



# XcitePI

## CHIP POWER INTEGRITY ANALYSIS

Use XcitePI to:

- Q Assess system effects on chip operation in the frequency and time domain
- Q Evaluate various bump, pad and power grid configurations
- Q Explore on- and off-chip decoupling capacitor options
- Q Conduct what-if experiments to improve chip and package performance
- Q Select the package that meets IC objectives
- Q Perform simultaneous switching noise simulations
- Q Generate SPICE or multi-port S-parameter chip models
- Q Examine chip performance with different off-chip models
- Q Prevent costly re-spins by addressing power integrity challenges before tape-out

XcitePI™ performs dynamic noise simulation of the full-chip power grid structure utilizing an approach that supports co-design for complete chip-package-board power integrity assessment. XcitePI performs frequency based impedance analysis as well as time domain simulations of voltage noise. Extractions can be performed on either selected structures or of the entire chip. With XcitePI, design teams can increase confidence in chip reliability by identifying chip power integrity issues including those that can only be observed when the system is part of the simulation.

### Q Chip and Package Interactions

High-speed ICs (particularly those in flip-chip packages) are sensitive to noise which begins on-chip and propagates through package plane structures to create noise in another region of the chip. This phenomenon can only be simulated by taking into account the distributed chip and package interactions as well as the wave propagation inside both the chip and package. Sigurity's approach ensures these elements are accurately simulated. In contrast, simulations utilizing off chip models which lump all or a large number of power and ground bumps fail to accurately compute on-chip voltage noise distributions.

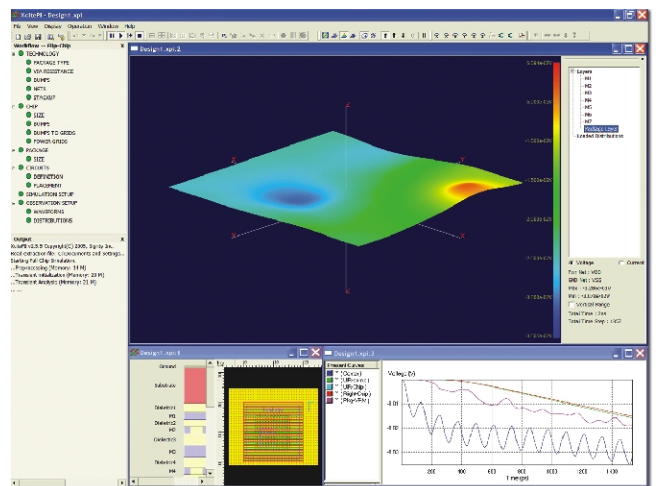


FIGURE 1. Transient analysis of the full-chip power grid taking into account the package effects.

### Q Simultaneous Analysis

Sigurity provides a flexible and accurate approach for chip-package-board assessment. XcitePI chip-level simulations can be run with distributed package models such as those created with Sigurity's XtractIM. For ultimate accuracy, complete multi-level system designs can be simultaneously simulated in Sigurity's CoDesign Studio environment. This simultaneous analysis provides the most detailed modeling of the distributed interactions between the chip, the package and the board to enable effective assessment of overall power delivery performance. This enables users to determine the impact of possible design improvement options.

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### Accurate Parasitic Extraction and Fast Simulation

XcitePI includes an extremely fast parasitic extraction engine to enable efficient simulation of the full-chip power grid. Resistance, capacitance and inductive parasitics are fully considered between all conductors of the IC power grid including mutual inductance and capacitance. This assures greater accuracy than approaches that only consider resistance or self-capacitance. XcitePI offers fast simulation throughput even for the entire chip power grid incorporating package data as well as for multi-die SiP projects.

### Time and Frequency Domain Simulations

XcitePI incorporates both time domain and frequency domain analysis capabilities. Transient simulations show dynamic spatial variation of voltage noise in the system and enables direct observation of waveforms. Frequency domain analysis enables assessment of impedance profiles across broadband frequencies and is well suited to looking at power delivery challenges. Combining the two enables users to work in ways that are both familiar and well suited to the issues they are investigating. Flexible viewing and dynamic replay options are included to support rapid what-if consideration of various design scenarios.

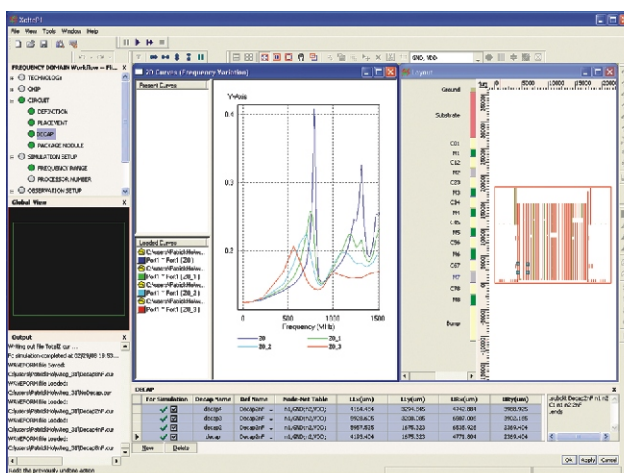


FIGURE 2. Analysis of frequency domain impedance values for various decoupling capacitor implementations.

### Interfaces

- Available for use with Windows and Linux.
- Links to Sigridy's CoDesign Studio for simultaneous chip-package-board analysis.
- Access to chip physical data in GDSII and LEF/DEF formats.
- With XtractIM, SPEED2000 or PowerSI, interfaces to IC Package, SiP and PCB physical design systems from Sigridy, Cadence, Mentor Graphics, Zuken, etc.
- Supports Circuit models in SPICE format.