

CoDesign Studio

OPTIMIZE CHIP & PACKAGE POWER PERFORMANCE

Use CoDesign Studio to:

- ❖ Analyze the performance of the complete chip and package power delivery system
- ❖ Perform fast and accurate analysis of the complete IC power grid, including the critical effects of the package
- ❖ Evaluate different on-chip and on-package decoupling capacitor schemes
- ❖ Perform transient simulation of the entire package, while considering the on-chip power grid structure
- ❖ Design and analyze interdependent chip and package designs in a single, unified, co-design environment
- ❖ Optimize the electrical and physical chip and package design through intuitive and easy-to-use "what-if" design exploration
- ❖ Ensure that your chips are operational when they are placed into the package

CoDesign Studio™, part of Sigrity's highly acclaimed set of power and signal integrity solutions, is a comprehensive chip and package co-design environment for analyzing and optimizing the performance of the entire power delivery system. It simultaneously co-simulates the complete package and the complete chip, in an integrated design environment, considering the critical package effects that impact the correct operation of the chip. CoDesign Studio ensures that chips shown to be functional during simulation and testing are also fully operational when placed into the actual package.

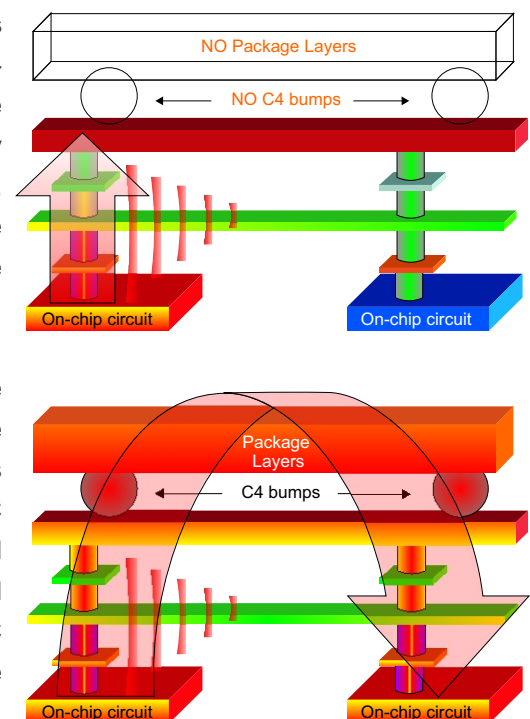
The CoDesign Studio solution analyzes the power integrity of the entire chip and package power delivery system by using an integrated combination of Sigrity's industry-standard SPEED2000™ solution for electrical analysis of the package, with the company's XcitePI™ solution for complete IC power grid analysis. This unique co-design methodology identifies power performance issues early in the design cycle, and provides design optimization techniques that can prevent costly re-spins and iterations, helping deliver your product to market on time.

Chip Power Analysis Must Include the Complete Package

❖ Realistic Chip Operation is Package Interdependent

Today's large and complex IC designs have an increasing number of high-speed clocks, decreasing voltage margins, and stringent power integrity requirements. Without the package, simulation tools show that voltage noise is likely to locally dissipate through the high-loss IC power grid.

However, by including the complete package, the same voltage noise is more likely to propagate through the low-loss package power planes to far-away IC circuits, affecting the operational integrity of the chip. Therefore, the full package must be included during IC power integrity analysis for accurate power noise representation.



CoDesign Studio

OPTIMIZE CHIP & PACKAGE POWER PERFORMANCE

Advanced Power Integrity Analysis

❖ Fast and Accurate Extraction and Simulation

Unlike typical EDA power integrity tools that often generate incomplete parasitics for today's very large and complex designs, CoDesign Studio utilizes proprietary computational techniques to consider the complete set of self and mutual RLC chip parasitics, along with all electromagnetic interactions of the package. CoDesign Studio replaces the simplistic off-chip models and lumped connections found in other EDA tools with the actual package structure and a fully distributed connection model. CoDesign Studio performs full-chip extraction a simultaneous simulation of the entire chip and package power delivery system, overcoming the speed, capacity, and complexity limitations of other EDA tools.

True Chip-Package Co-Design

❖ Integrated and Unified Design Environment

CoDesign Studio provides the first comprehensive link between the critically interdependent chip design and package design, in a single unified co-design environment. The intelligent "what-if" design feasibility enables fast and accurate electrical and physical power structure exploration and optimization, including chip and package decoupling capacitor placement, multiple package selection, floorplan optimization, and IC bump/pad and power grid reconfiguration.

Sigrity's Proven Technology

❖ Power and Signal Integrity Solutions

CoDesign Studio provides an integrated SPEED2000 and XcitePI co-design environment for the analysis and optimization of the entire power delivery system. SPEED2000 is the first and only commercial time-domain simulator for performing transient electromagnetic analysis of entire PCBs and packages. XcitePI is the industry's first IC power integrity solution to provide complete transient simulation of the entire IC power grid, including the distributed electromagnetic effects of the package. PowerSI™ provides complex frequency-domain electrical analysis of complete PCBs and packages. PowerDC™ provides fast and accurate IR drop analysis of PCBs and packages. Broadband SPICE™ is the industry-standard solution for N-port network parameter conversion to SPICE circuits.

Sigrity provides comprehensive chip, package, and PCB simulation and optimization solutions for power and signal integrity analysis. Visit our website at www.sigrity.com for industry and academic articles, and for success stories from our customers who have used Sigrity's proven technology to "Achieve What Others Can't".