Proceeding of 1995 IEEE 4th Topical Meeting on Electrical Performance of Electronic Packaging, p. 235-238
0-7803-3034-X/95/$4.00© 1995 IEEE

A New Approach to Signal Integrity Analysis of High-Speed Packaging

Yuzhe Chen, Zhaoqing Chen, Zhonghua Wu, Danwei Xue and Jiayuan Fang
Department of Electrical Engineering, State University of New York at Binghamton
Binghamton, NY 13902 (607)777-4412

Abstract

A signal integrity analysis program that simultaneously performs the electromagnetic field simulation and the circuit simulation is introduced in this paper. The electromagnetic field simulation algorithms are based on special geometric features of packaging structures and can run two to four orders of magnitude faster than general-purpose electromagnetic tools. The use of the distributed circuit simulation technique drastically reduces the simulation time for lumped circuit components. This program can promptly simulate practical packages of tens of power/ground planes and thousands of vias and signal traces, while considering signal integrity problems such as signal delay, distortion, reflection, coupling, and power/ground noise. The accuracy of the simulated results is verified by measurements.

This work is supported in part by the National Science Foundation under contract MIP-9357561, and the Integrated Electronics Engineering Center (IEEC) at the State University of New York at Binghamton.

The authors are with the Department of Electrical Engineering, State University of New York at Binghamton, Binghamton, NY 13902

Proceeding of 1995 IEEE 4th Topical Meeting on Electrical Performance of Electronic Packaging, p. 235-238
0-7803-3034-X/95/$4.00© 1995 IEEE

A New Approach to Signal Integrity Analysis of High-Speed Packaging

Yuzhe Chen, Zhaoqing Chen, Zhonghua Wu, Danwei Xue and Jiayuan Fang
Department of Electrical Engineering, State University of New York at Binghamton
Binghamton, NY 13902 (607) 777-4412

Introduction

The trend of electronic packaging is toward faster transition speed and more I/O count due to the advances in fabrication technology. As a consequence, many signal integrity problems become increasingly challenging to design engineers [1]. In the high speed and high density regime, a circuit board built without post-layout signal integrity verifications is unlikely to work. Accurate and efficient signal integrity analysis tools are necessary to cut down the design/prototyping cycle [2].

Complex electromagnetic wave propagation and interaction occur in high-speed electronic packages. Most signal integrity tools are based on SPICE types of circuit simulators which are mainly for linear and nonlinear lumped circuits. Some of these tools can handle transmission lines, and compute crosstalk between parallel metal conductors. Most of them treat power and ground planes as ideal power and ground supplies. A small number of these tools model the power and ground planes by effective inductors (L_{eff}) and model the interaction between vias by mutual inductors. The effective inductor model has been found unsuitable for the modeling of high-speed packaging structures because it cannot account for electromagnetic effects due to wave propagation and resonance in packaging. These simulators generally fail to accurately simulate voltage fluctuations on power and ground planes, and also fail to accurately simulate noise in signal lines caused by the interaction between the power and the signal distribution systems.

Equivalent circuit models or network parameter (such as S, Z, or Y matrices) representations of electronic packages can be extracted through intensive electromagnetic computations. To fully take into account package resonances and electromagnetic interactions in packages of a large number of vias, the number of these frequency-dependent and via-hole location dependent network parameter elements can become formidably large, resulting in long computation times for circuit simulations. The general-purpose electromagnetic tools that are based on the finite element, the boundary element, and the finite-difference time-domain methods are suitable for extracting transmission line parameters and equivalent circuit models of individual interconnect discontinuities. However, they are too time consuming to be applied for the simulation of wave propagation in entire packaging structures.

Our electromagnetic field simulation algorithms are derived on special geometric features of packaging structures. The electromagnetic field inside a typical multi-layered package is a three dimensional field in nature. However, it is not an arbitrary three dimensional field and can be decomposed into several modes each of which can be simulated with special techniques that are orders of magnitude faster than those for general 3-D fields. The package simulator introduced in this presentation mainly consists of three solvers: the circuit, the transmission line, and the plane solvers as shown in Figure 1. The circuit solver computes all the lumped circuit components, such as resistors, capacitors, inductors,

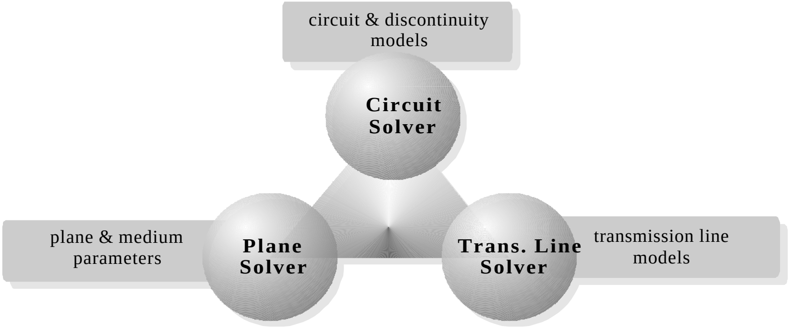


Figure 1 Components of the proposed packaging simulator.

drivers, and receivers. The transmission line solver computes signal propagation along transmission lines such as strip and microstrip lines [3]. The plane solver computes transient voltage and current distributions on metal planes [4]. The circuit, the transmission line and the plane solvers are run simultaneously, and properly linked together to take into account interactions between circuits, metal planes and signal vias/traces. On the aspect of circuit analysis, we use the distributed circuit solver that may include many individual circuit solvers instead of the traditional approach that computes all the lumped circuit components associated with a package with one circuit solver. Circuit networks that are connected by package interconnects have their own circuit equations and are each solved by a designated circuit solver that is linked to the plane and the transmission line solvers. With the distributed circuit solver approach, each circuit solver deals with a relatively small size of circuit network, resulting in more efficient and stable circuit analysis.

Examples

1. This example compares our simulation results with measurement data. The measurement setup is shown in Figure 2, where a via passes through two metal planes on both sides of a printed circuit board of 469 mm by 573.5 mm in size. The relative dielectric constant of the 1.46 mm thick dielectric medium is 4. Potential differences between the two metal planes were measured at the edges of the planes. The source waveform is shown in Figure 3. The waveform of the actual measurement appears to have significant edge reflections and resonance of electromagnetic fields, which are accurately represented by simulated results obtained by our method as shown in Figure 4.

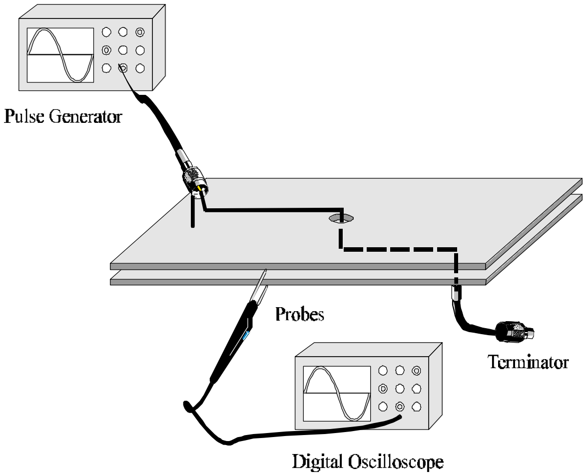


Figure 2 Experimental setup for measuring voltage fluctuations on metal planes.

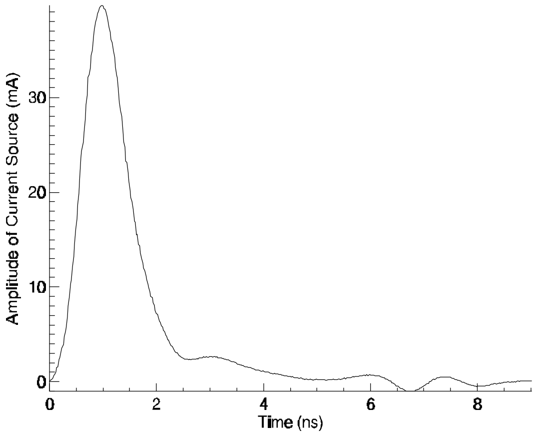


Figure 3 Source waveform.

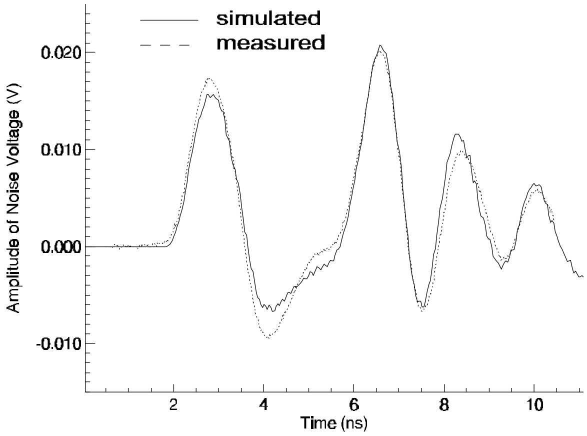
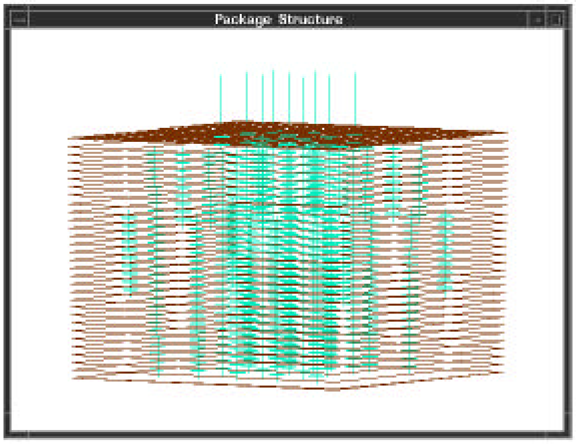


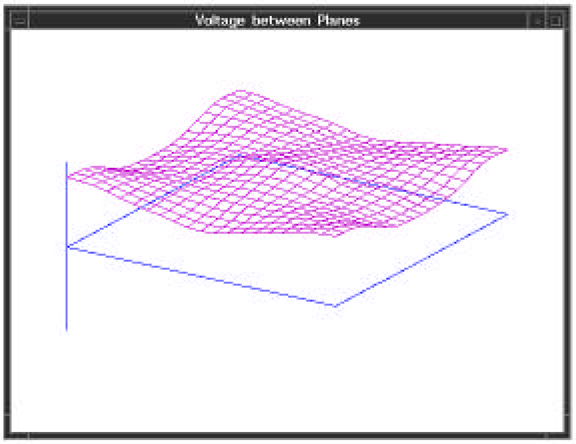
Figure 4 Comparison between measured and simulated voltage fluctuations on metal planes.

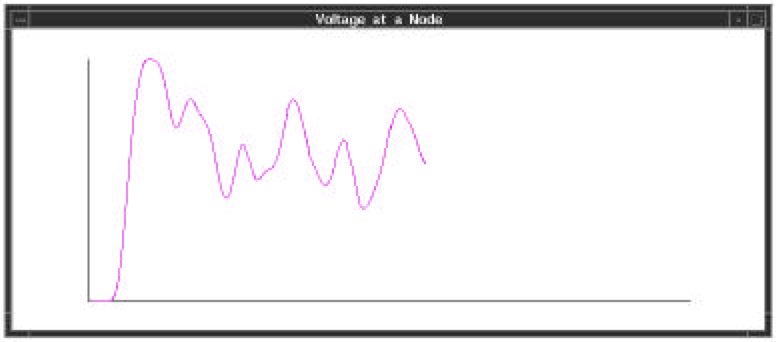
2. Figure 5 is the appearance of our signal integrity analysis program in the process of evaluating a 31-layer package with hundreds of vias (shown in window A). Window B displays the real time simulation results of spatial voltage distributions between two adjacent metal planes. Window C is the transient response of a node voltage in the lumped circuit, which is not drawn in Window A, connected to the package. For this example, which may take hours of CPU time of a super-computer with the general-purpose 3-D FDTD method, it only takes tens of seconds for the transient waveform simulation with an IBM R/6000 notebook workstation model N40.

Acknowledgment

Measurement results presented in this paper are provided by Dr. Chi-Shih Chang and Mr. Steven Rosser at IBM Microelectronics Division at Endicott, New York.







References

[1] Tai-Yu Chou, "Signal Integrity Analysis in ASIC Design," *ASIC & EDA*, pp.70-81, May 1994.
[2] Dan Strassberg, "Signal-integrity tools," *EDN*, pp. 61-68, Jan. 1995.
[3] J. Fang, Y. Chen, Z. Wu, and D. Xue, "Model of Interaction Between Signal Vias and Metal Planes in Electronics Packaging," *IEEE 3rd EPEP Conference Proc.*, pp. 211-214, Nov. 1994.
[4] Y. Chen, Z. Wu, A. Agrawal, Y. Liu, and J. Fang, "Modeling of Delta-I Noise in Digital Electronics Packaging," *1994 IEEE MCM Conference Proc.*, pp. 126-131, Mar. 15-17,1994.