



# **Impact and Modeling of Anti-Pad Array on Power Delivery System**

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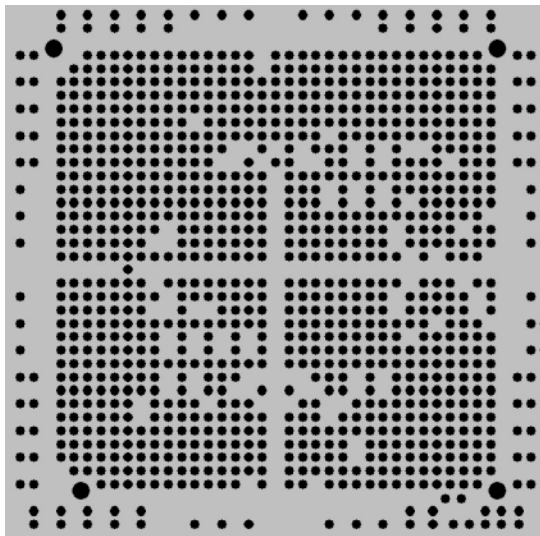
**Princeton, New Jersey**

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- **Test card structure and lab measurement setting and results**
- **3D EM model extraction**
- **Board level modeling and simulation**
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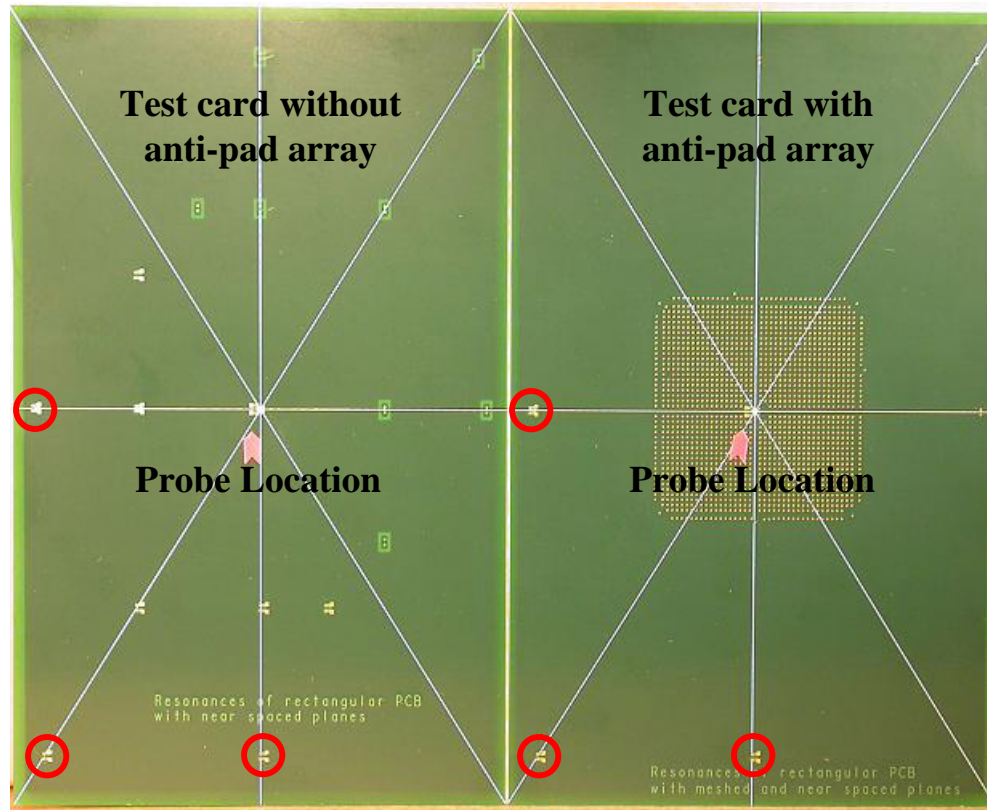
## Anti-pad Array and Its Effects

- Several thousands passing through vias on a typical CISCO board
- Most of the vias are located right under the BGA ASICs with regular pattern
- No commercial EDA software available for studying the effects of anti-pad array at system/board level
- Anti-pad array will impact signal transmitted and power supply system performance

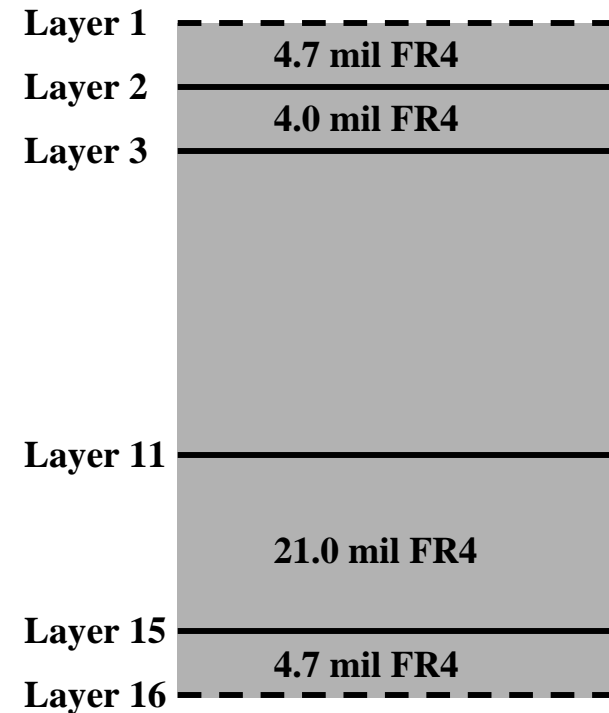


Our intuition suggests that the plane inductance and resistance will increase because of the reduction of the current flowing capacity; and that cell capacitance will vary due to the change in effective area and also due to the via structures that are passing through the anti-pad array.


# Test Card Structure



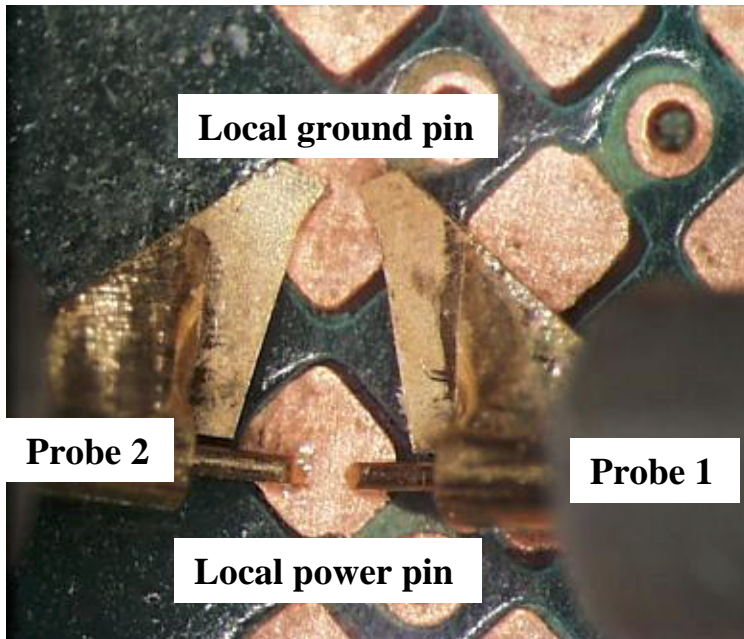
## Test Card Stackup



Total thickness=93 mils

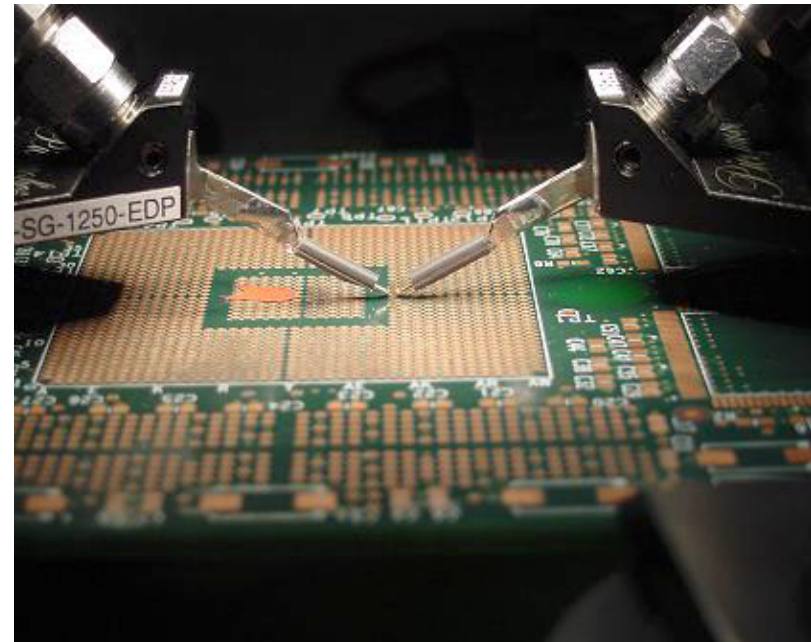
Two cases: open case  
short case (shorting at  locations)

# Lab Measurement

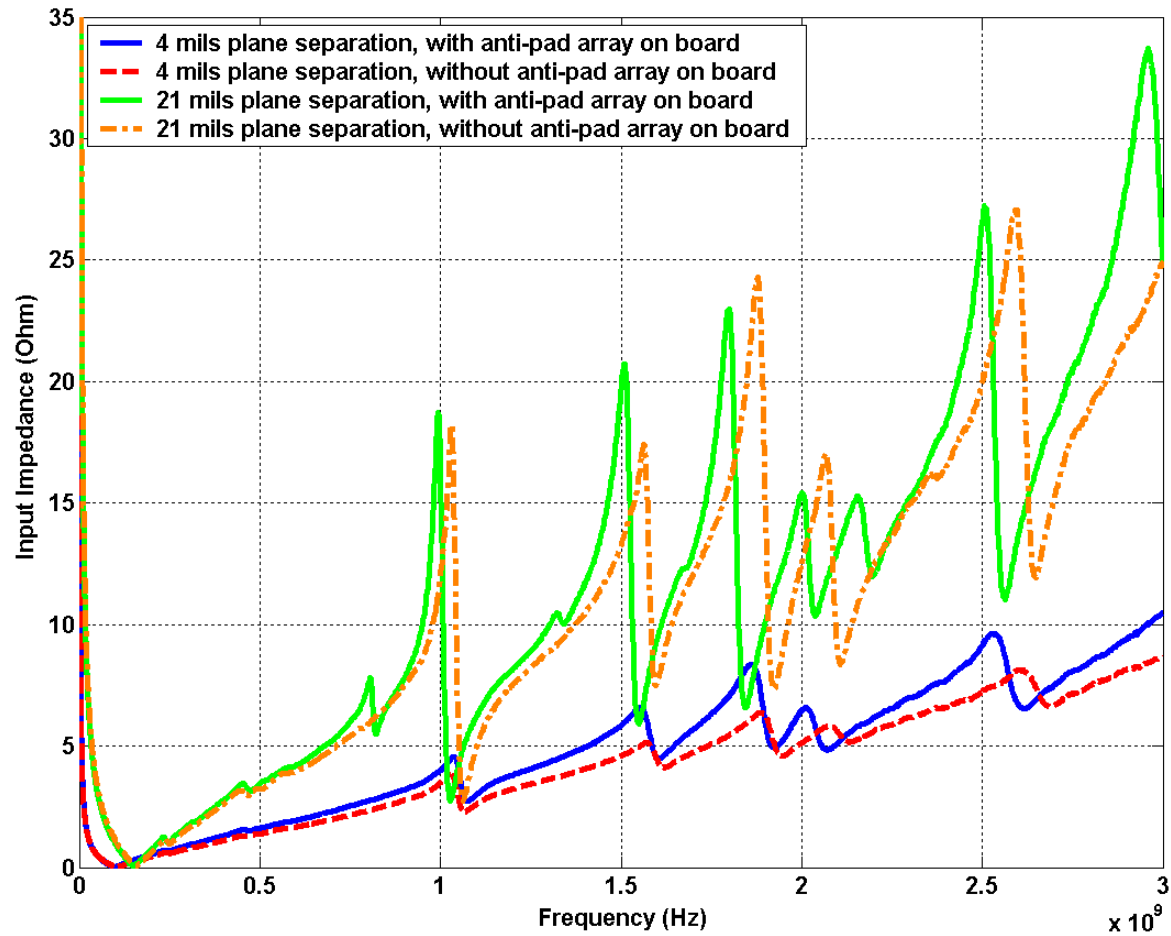


Probe setting detail

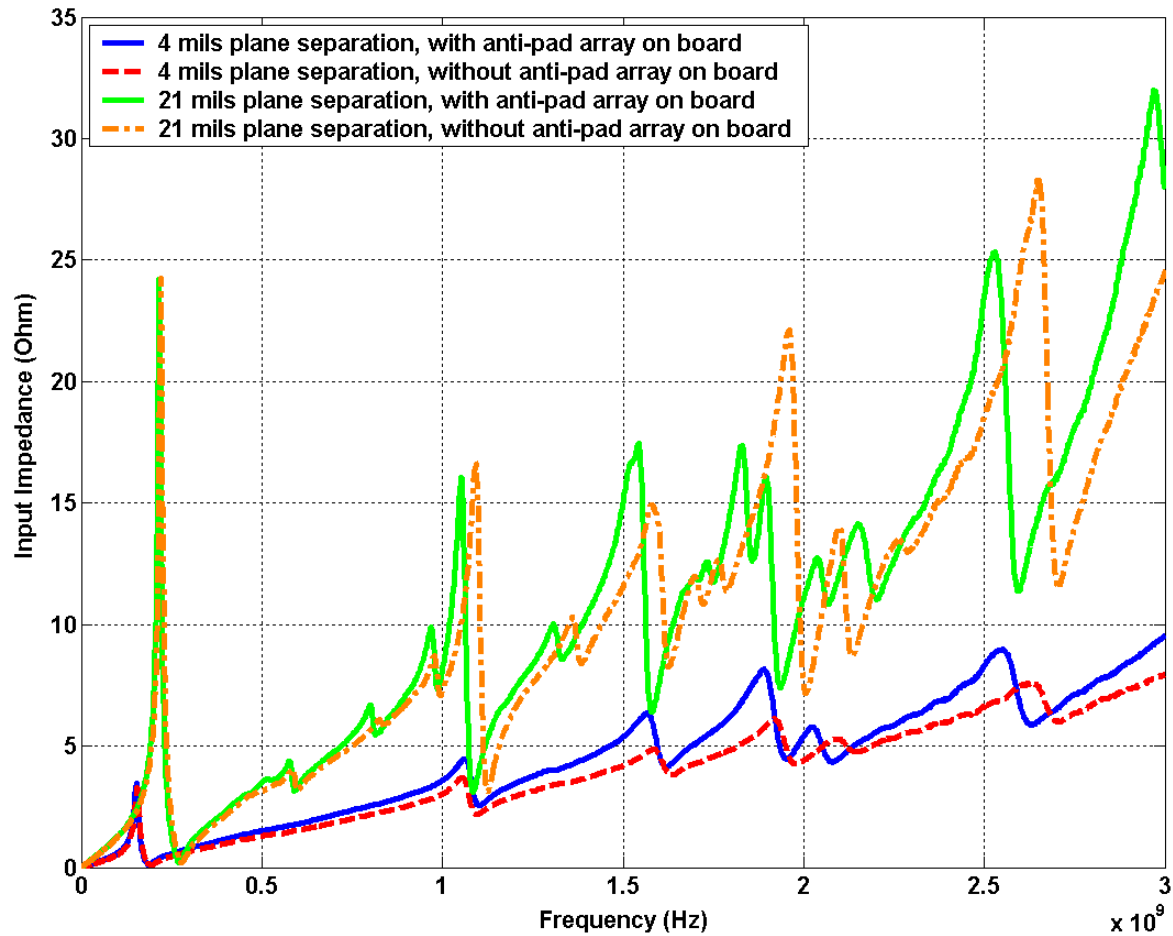
Probe setting



## Lab Measurement Results (Open Case)



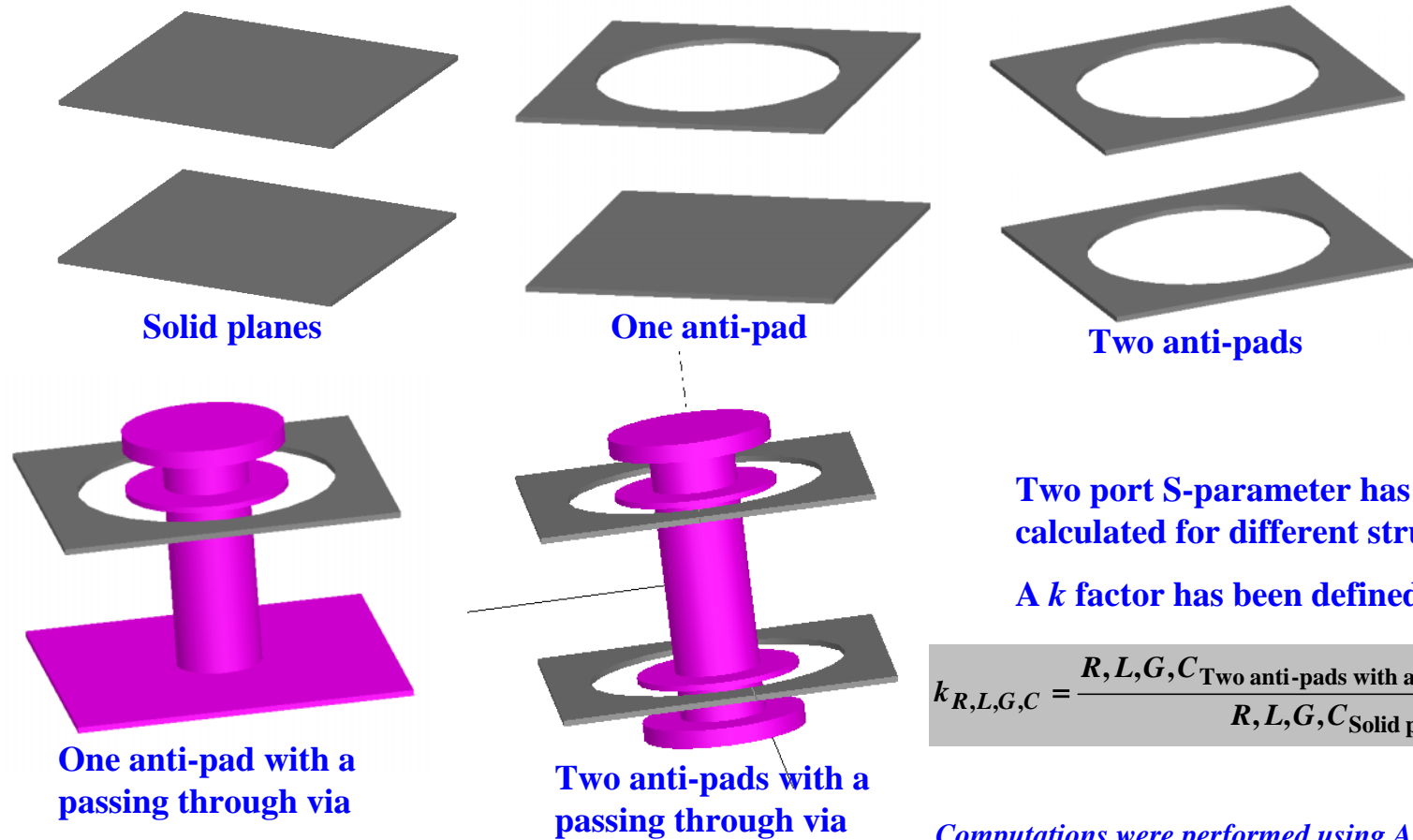
## Lab Measurement Results (Short Case)



## Observations from Lab Measurement Results

- From the measurement results, it is obvious that the anti-pad array exhibits different impedance and resonance impact on 4 mils and 21 mils structures.
- For the structure with 4 mils plane separation, the impedance has been raised by 10% to 30%.
- For the structure with 21 mils plane separation, the resonant frequency has been shifted downward several tenths of MHz to 100MHz.
- According to the measurement results, ignoring the impact of anti-pad array at the design stage could lead to a weakened power delivery system.

# 3D EM Field Solver Model Extraction



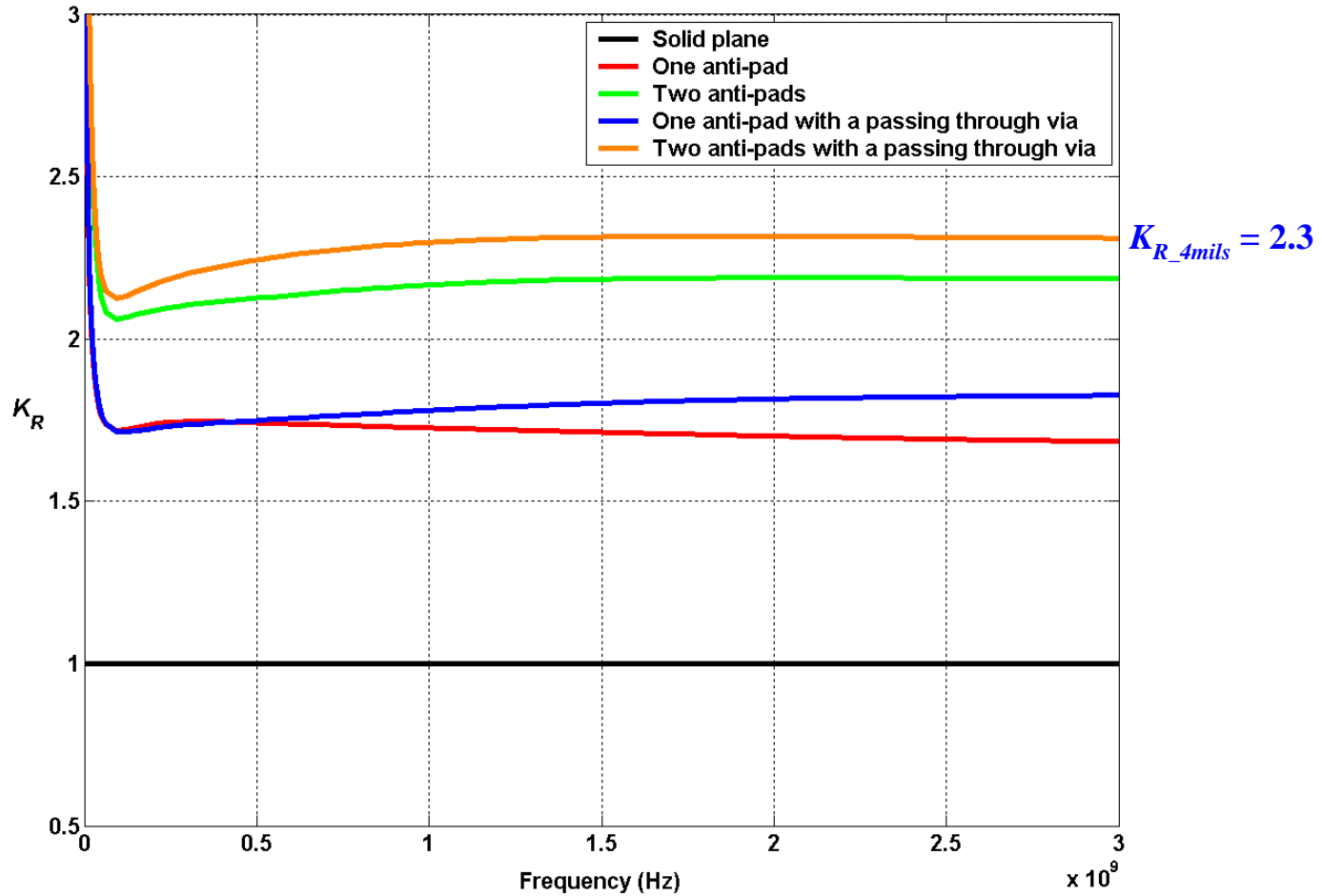
Two port S-parameter has been calculated for different structures.

A *k* factor has been defined as

$$k_{R,L,G,C} = \frac{R,L,G,C_{\text{Two anti-pads with a passing through via}}}{R,L,G,C_{\text{Solid planes}}}$$

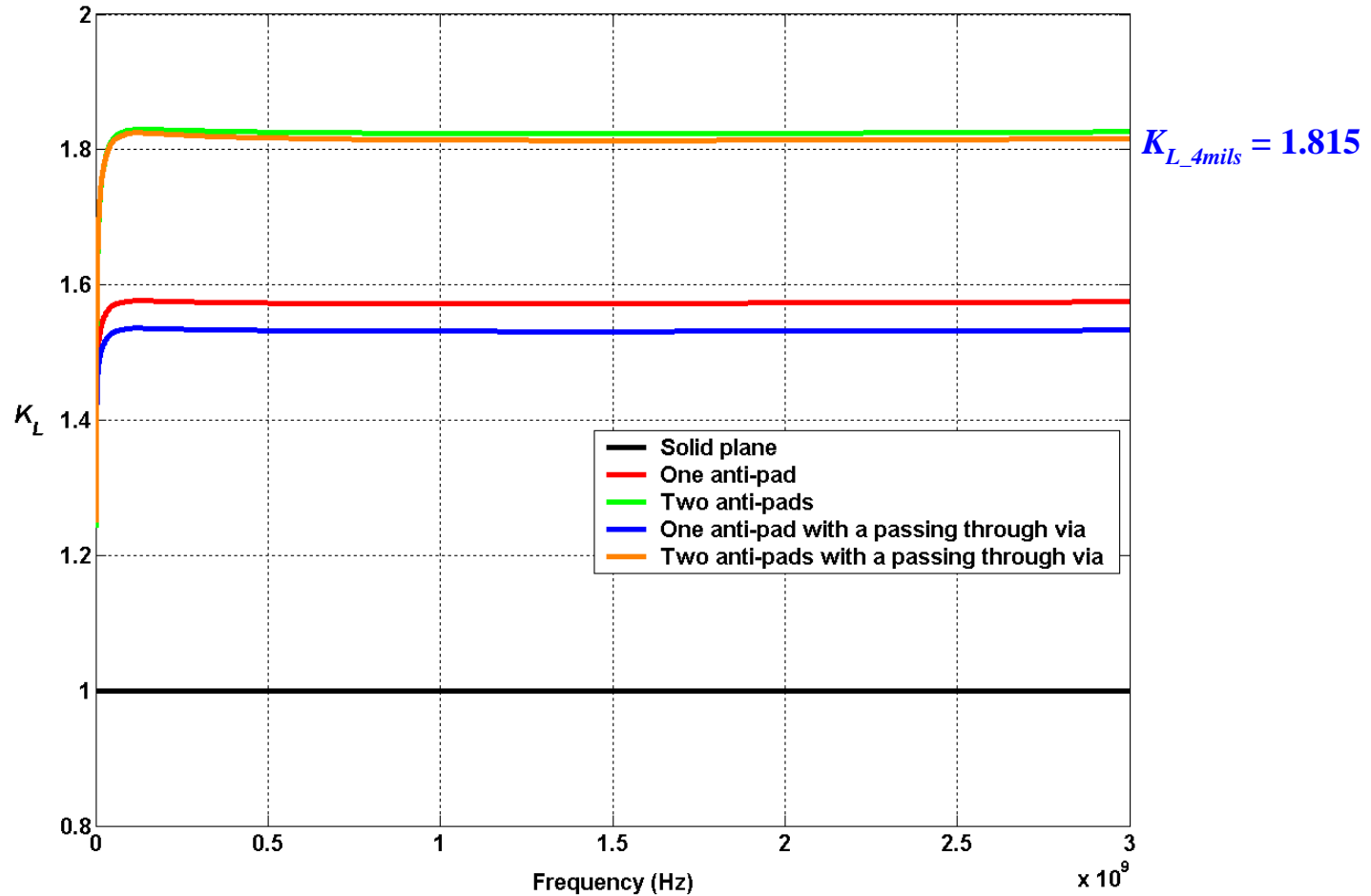
*Computations were performed using Ansoft HFSS™*

# Computed $K_R$ Factor



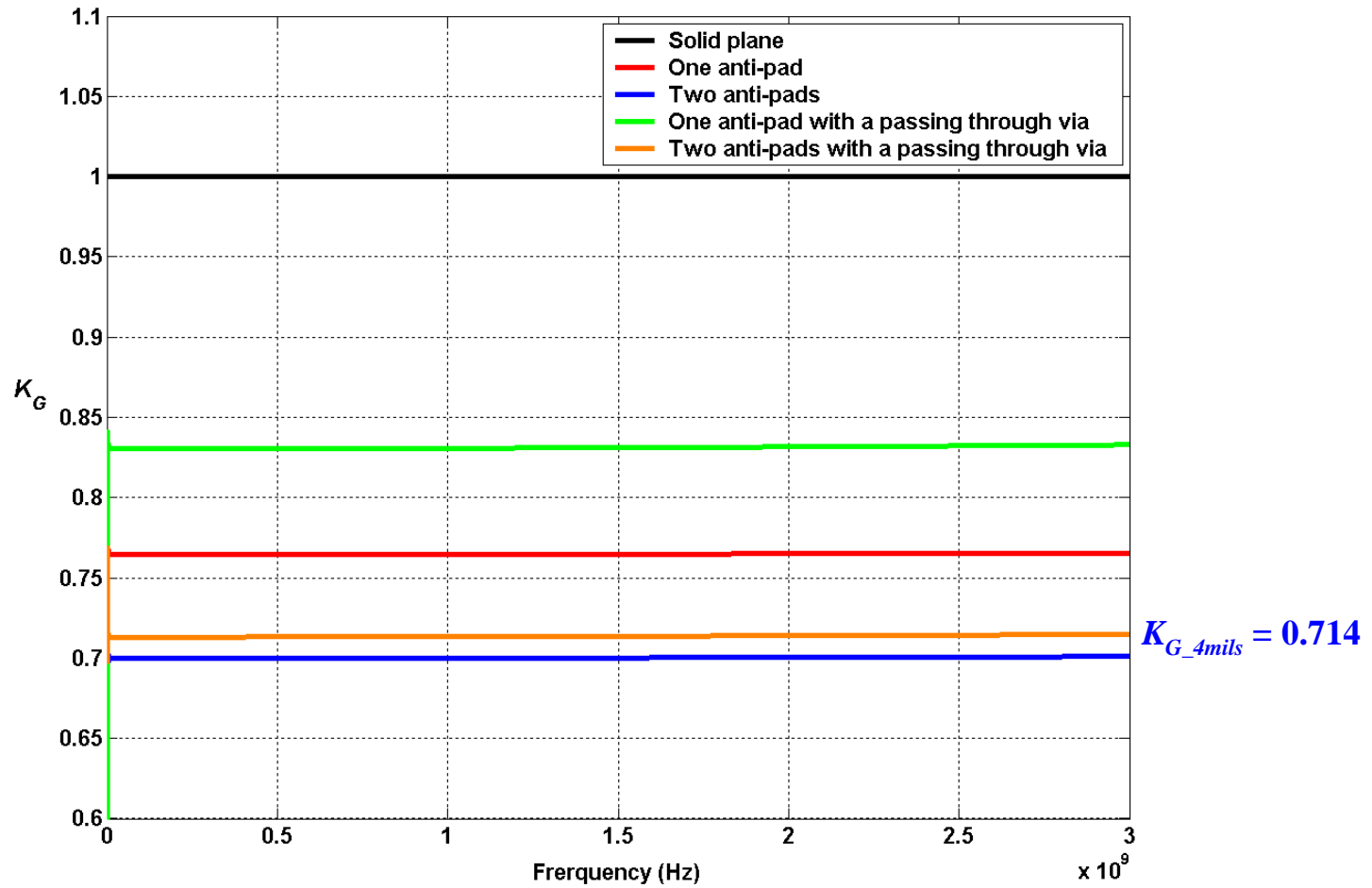
4 mils plane separation

# Computed $K_L$ Factor



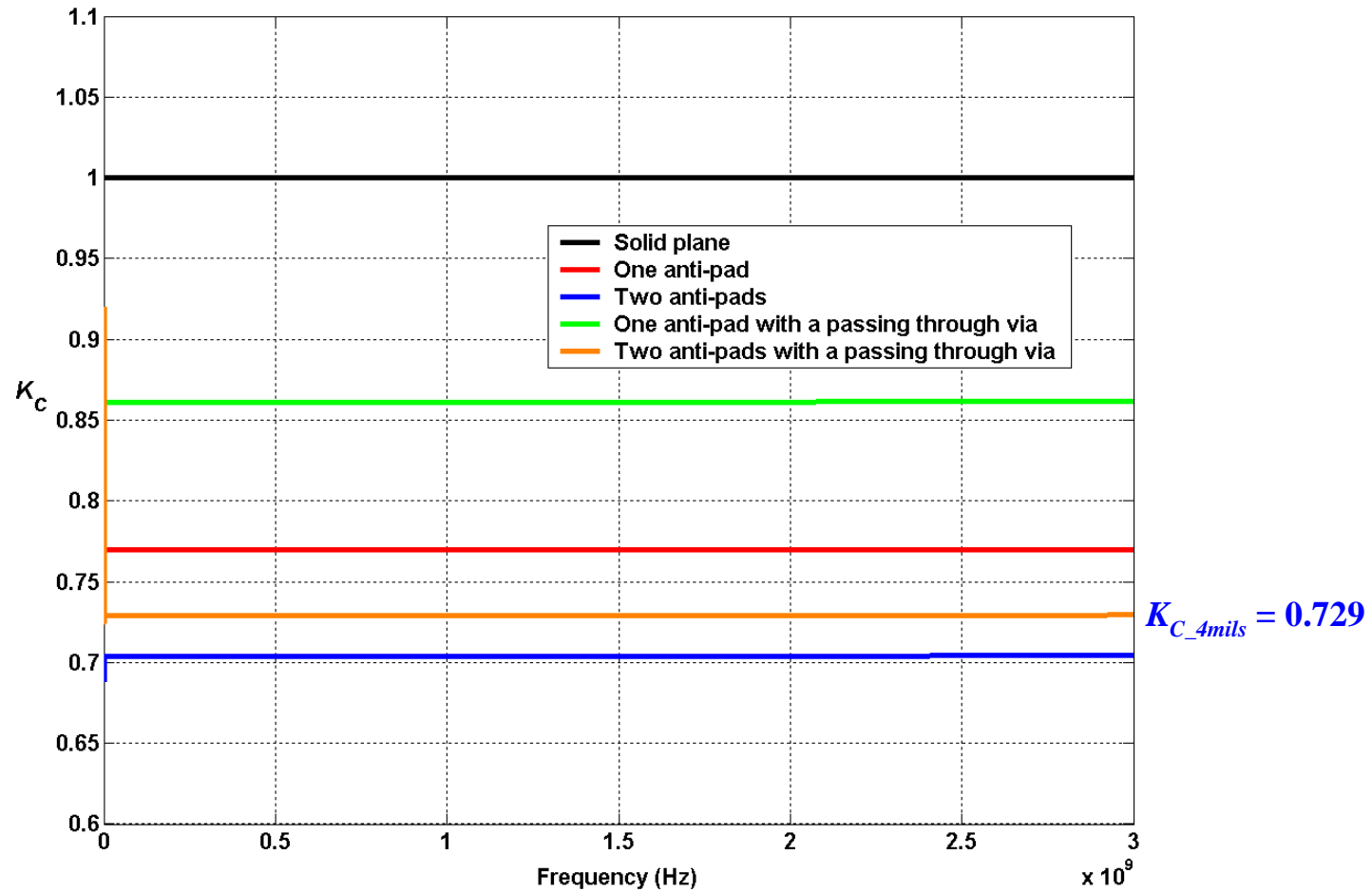
4 mils plane separation

# Computed $K_G$ Factor



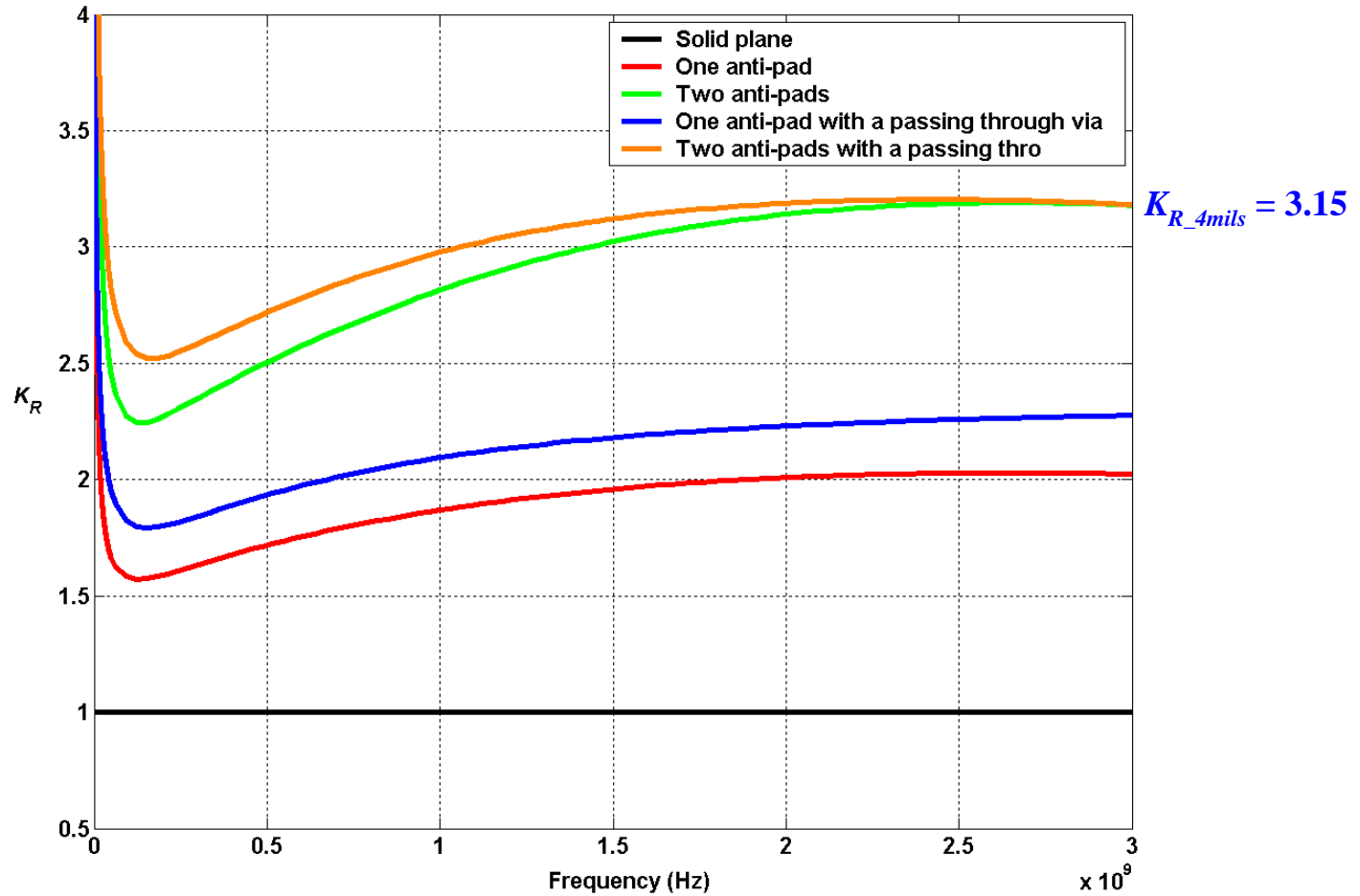
4 mils plane separation

# Computed $K_C$ Factor



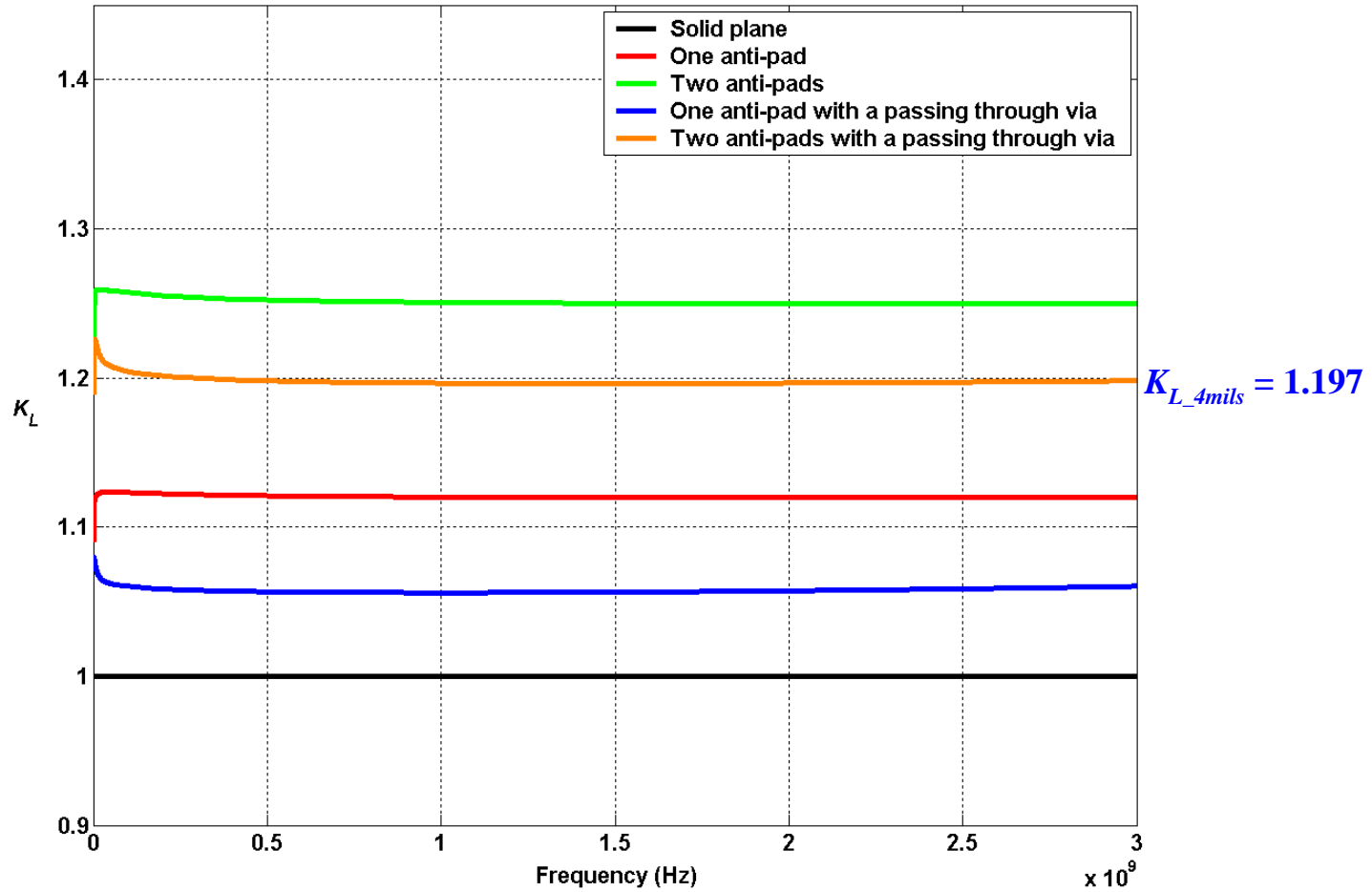
4 mils plane separation

# Computed $K_R$ Factor



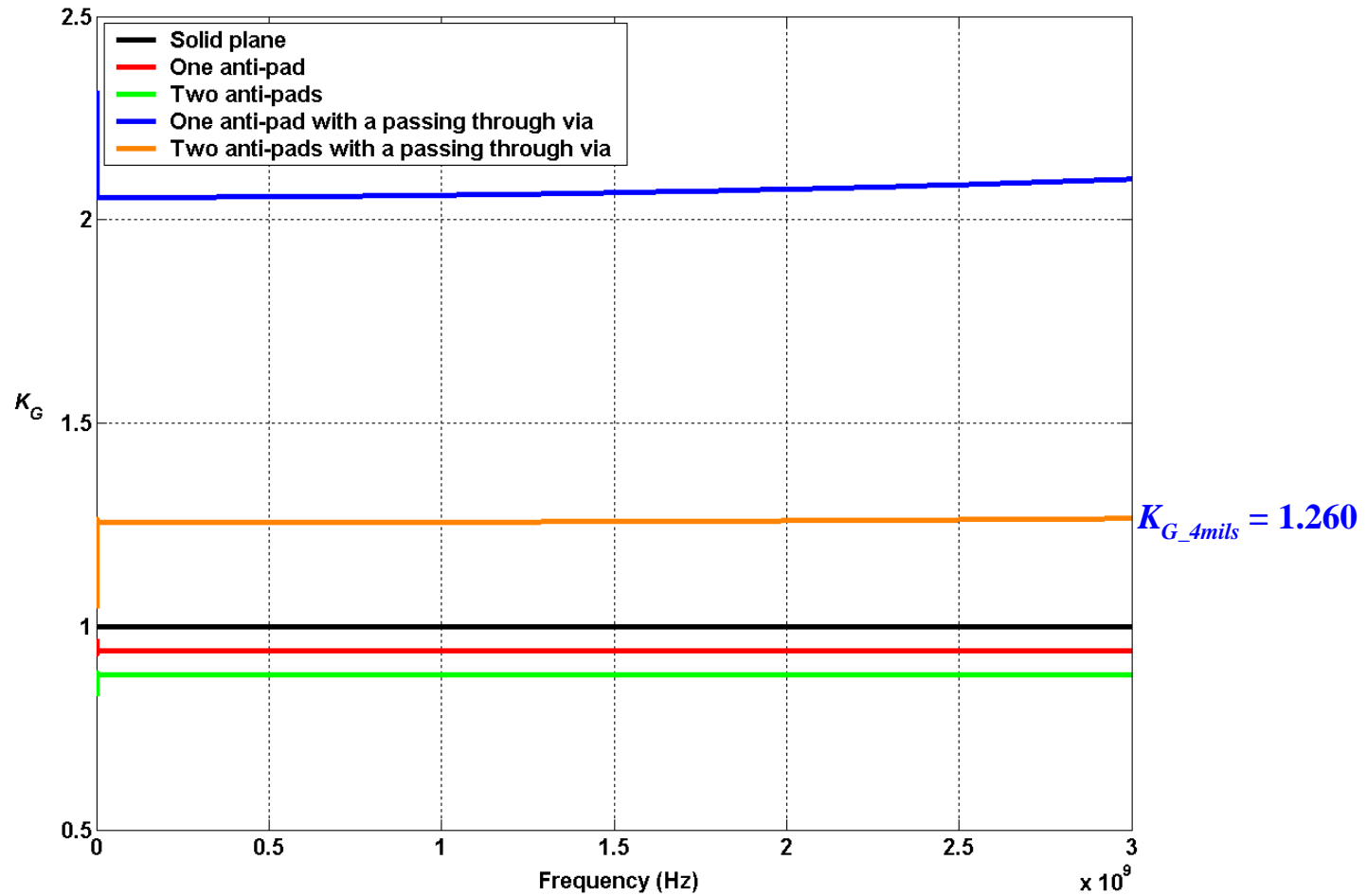
21 mils plane separation

# Computed $K_L$ Factor



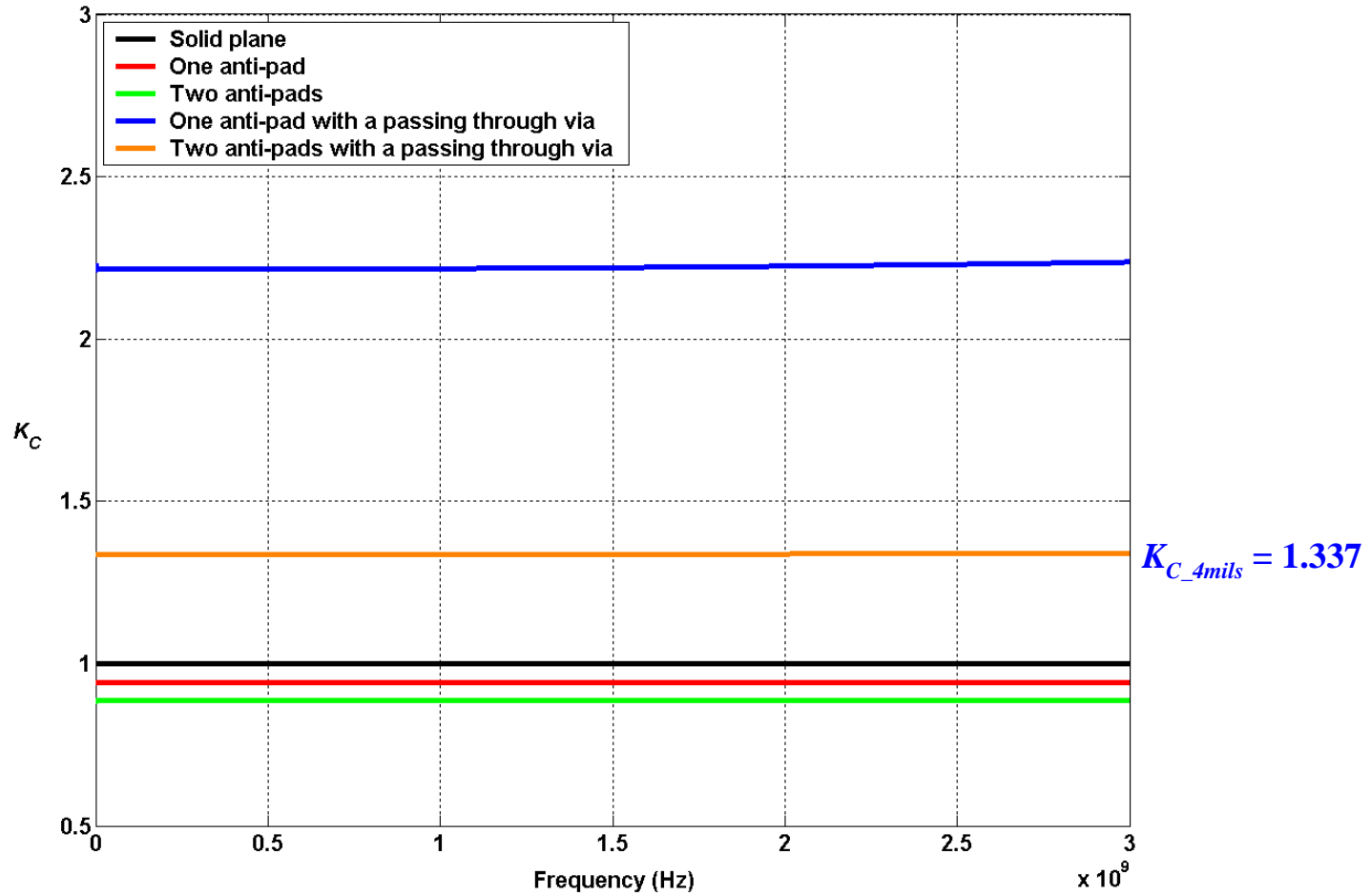
21 mils plane separation

# Computed $K_G$ Factor



21 mils plane separation

# Computed $K_C$ Factor



21 mils plane separation

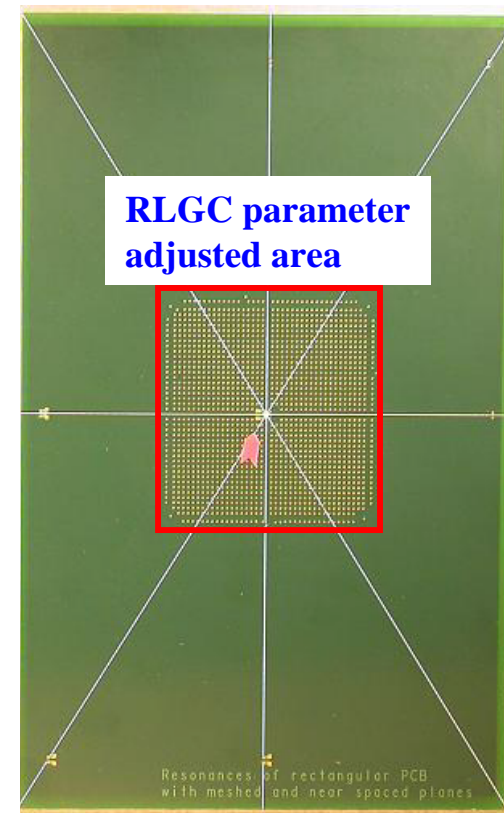
## K Factor Summary

	$K_R$	$K_L$	$K_G$	$K_C$
<b>4 mils plane separation</b>	<b>2.30</b>	<b>1.850</b>	<b>0.714</b>	<b>0.729</b>
<b>21 mils plane separation</b>	<b>3.15</b>	<b>1.197</b>	<b>1.260</b>	<b>1.337</b>

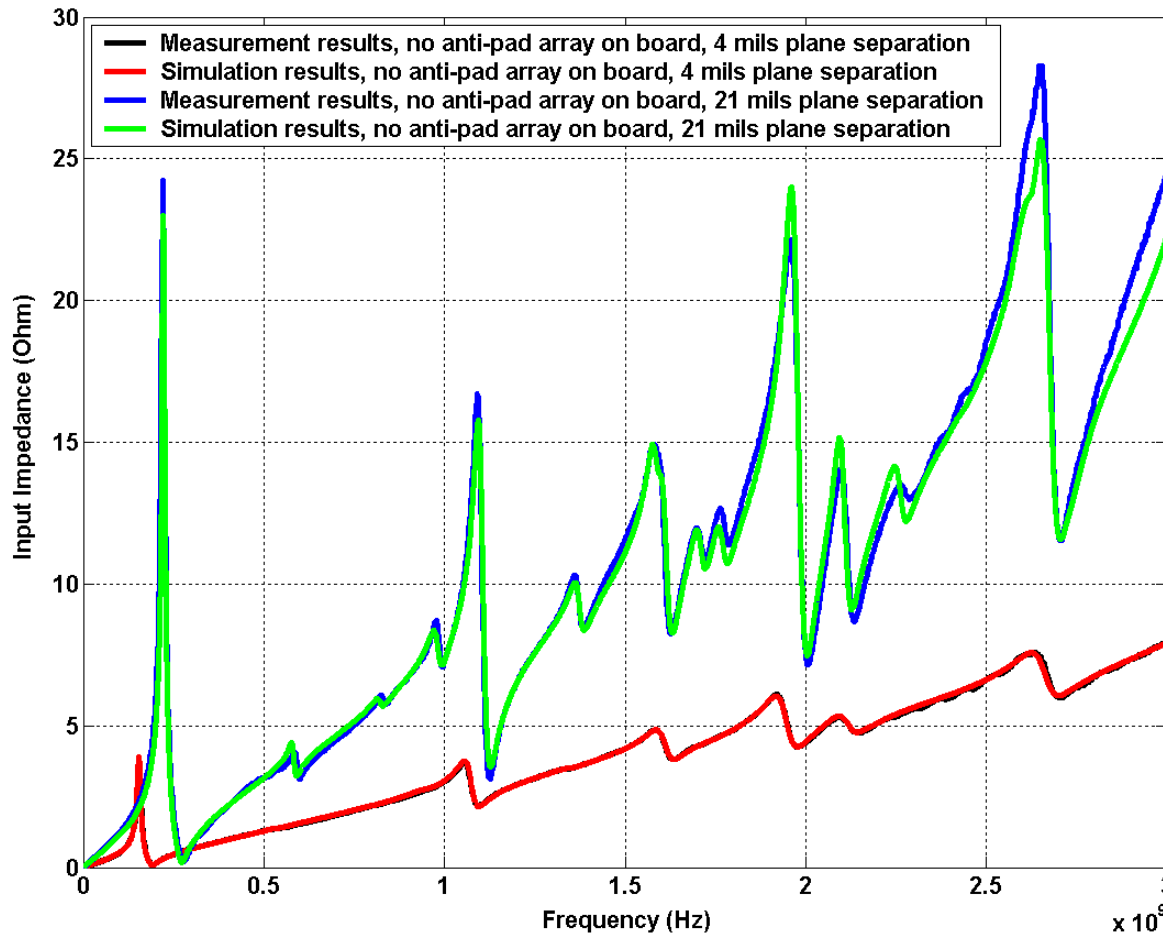
- **The table above lists the  $k$  factors that were used in simulation for both structures with 4 mils and 21 mils plane separations.**
- **The inductance and resistance always increase with the anti-pad array existing on the plane for both 4 mils and 21 mils structures.**
- **The capacitance and admittance will be reduced for the 4 mils structure, but will increase for the 21 mils structure.**
- **The  $k$  factor remains constant for a reasonably broad frequency range.**

## Board Level Simulation Setting

- $k$  factors are calculated by using Ansoft HFSS™ 3D EM field solver.
- The *RLGC* parameters adjustment is only for the area where the anti-pad array is located on the PCB.
- This approach was successfully applied into Sigrity SPEED2000™.
- Simulation results were compared with measurement results.

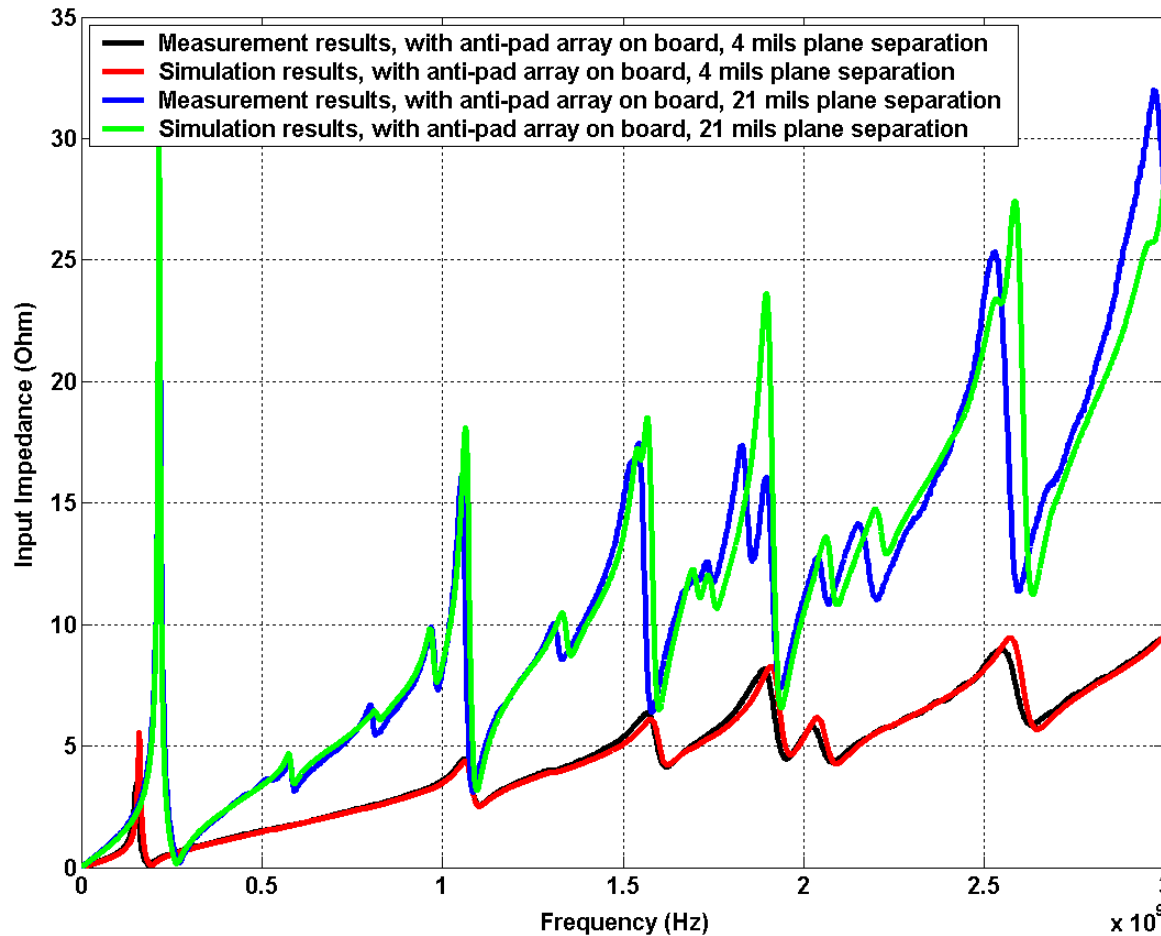


# Simulation Results vs. Measurement Results



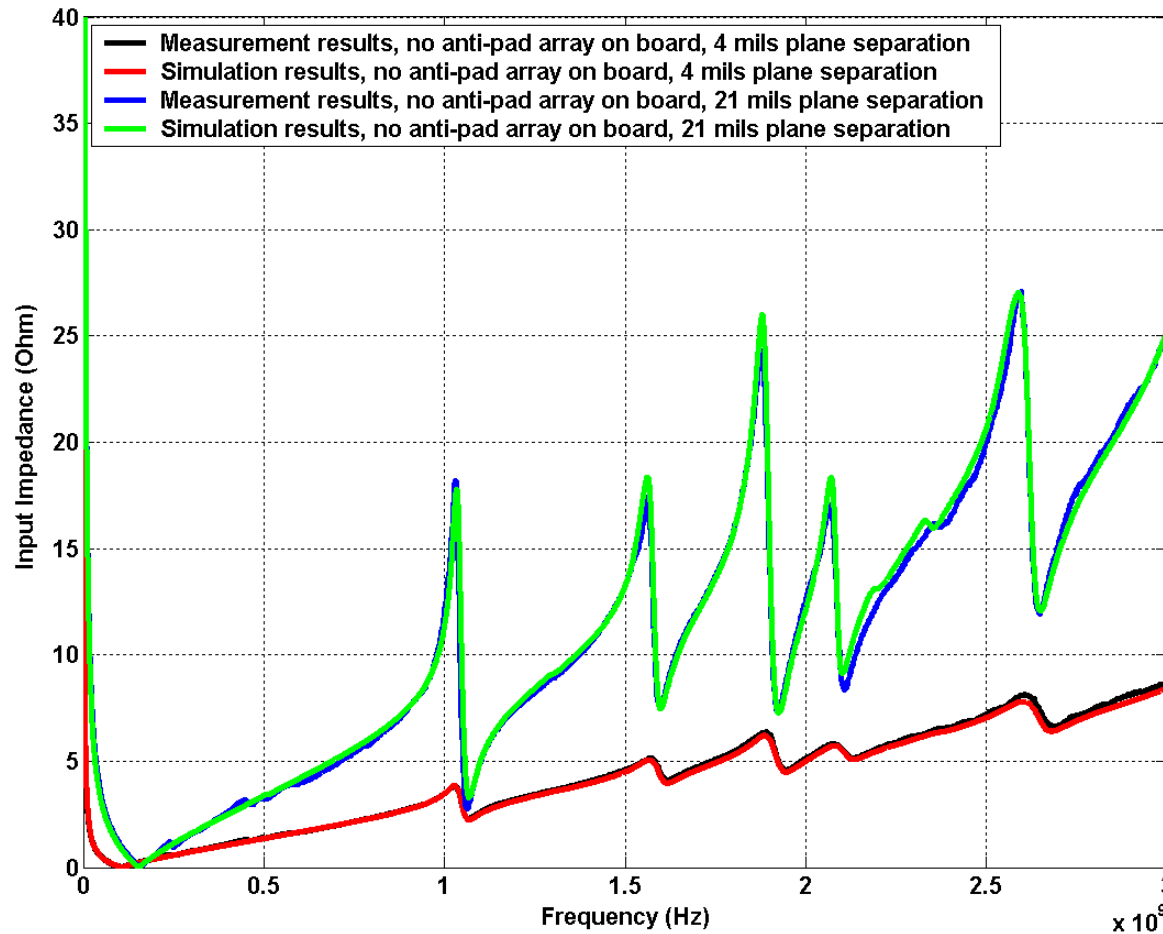
Short Case  
without Anti-pad  
array

# Simulation Results vs. Measurement Results



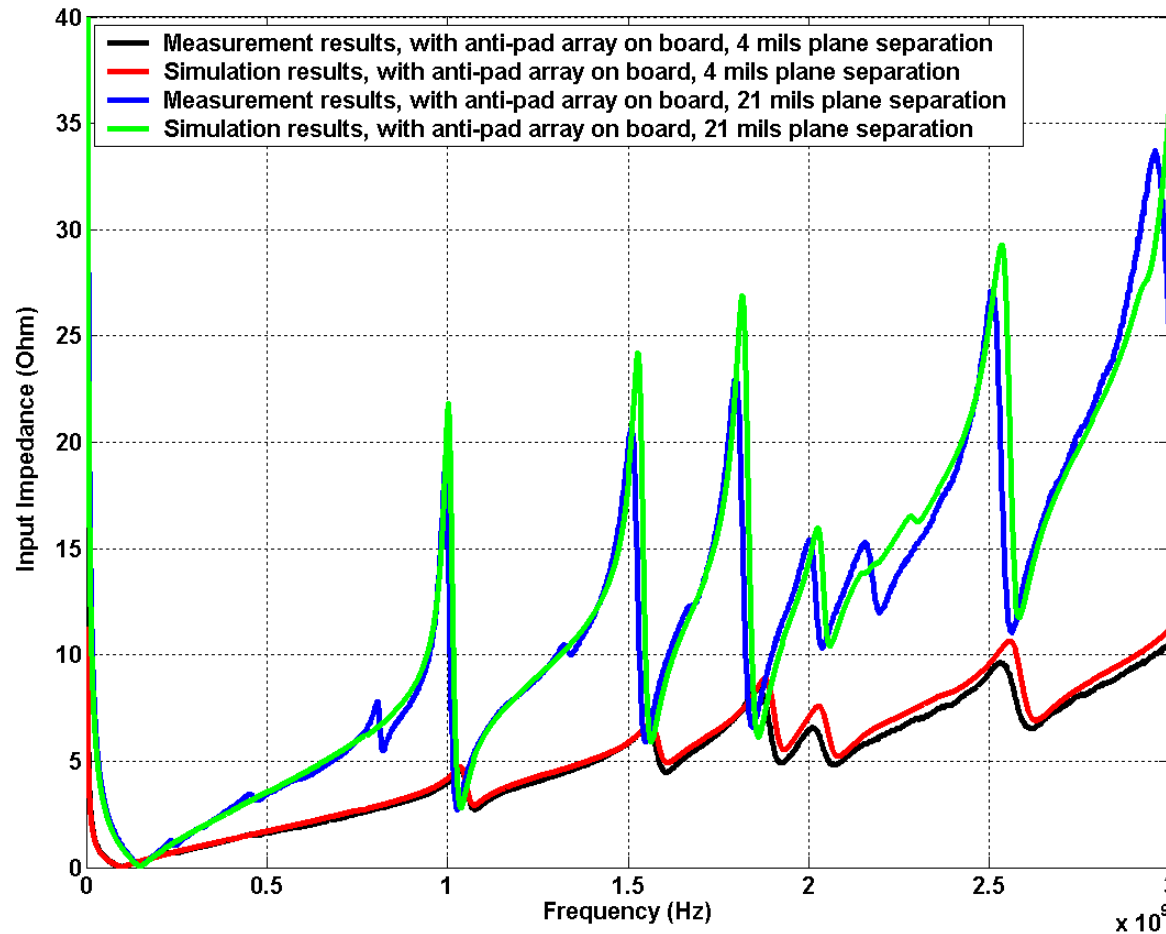
Short Case with Anti-pad array

# Simulation Results vs. Measurement Results



Open Case  
without Anti-pad  
array

# Simulation Results vs. Measurement Results



Open Case with Anti-pad array

## Conclusions and Future Work

- An effective approach for accurate consideration of anti-pad array impact on the power and ground planes is presented.
- Simulation and measurement comparison indicates that this approach is valid and the impact of the anti-pad array on the power delivery system has been captured up to several GHz.
- A frequency dependent  $k$  factor may improve the model accuracy for high frequency applications.