Impact and Modeling of Anti-Pad Array on Power Delivery System

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Abstract: The impact of anti-pad array on power and ground planes, especially at the area right under the BGA package, has been studied in this paper. An effective modeling and simulation approach based on 3D field computation has been used to take into account the anti-pad array effect. The simulation results match the measurement results. It has been found that the effect of anti-pad array on power delivery system is considerable; therefore it cannot be ignored in the power delivery system analysis and design for high-speed applications.

Introduction

The Internet is rapidly becoming an electronic agent for commerce, entertainment, communication, and information retrieval. The need for high-speed dedicated access to the Internet is increasing. As a result, the performance of network hardware, such as a line card system, is the key issue for realizing those needs. A good power delivery system is one essential enabler for the performance of such high-speed system. Especially the whole electronic industry is pursuing higher clock frequency, lower supply voltage, and larger surge current, an accurate power delivery model is necessary in order to design a high quality and cost effective power delivery system.

Parallel plate transmission line model [1, 2], represented by an LC grid depicted in figure 1, has been extensively used in the power delivery system analysis for printed circuit board (PCB) and even for IC package analysis. The inductance and capacitance in each cell of the LC grid is calculated as

$$L = \mu d, \quad C = \frac{\varepsilon A}{d} \tag{1}$$

where μ, ε, A, and d are the permittivity and permeability of the dielectric medium, the area of the cell, and the separation between two metal planes.

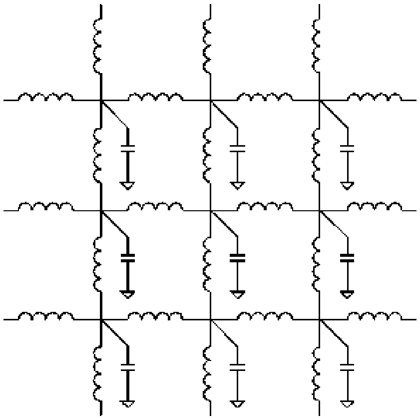


Figure 1, LC grid model for power delivery system analysis

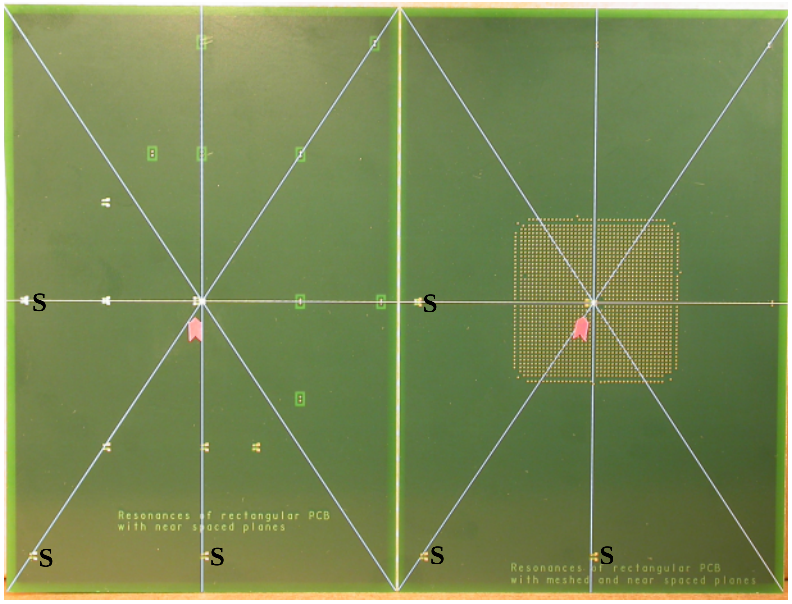
Usually, those sparse via holes on the power and ground planes have been ignored during the analysis of a power delivery system. It is questionable that how much an anti-pad array on the power and ground planes, especially at the place where a ball grid array (BGA) package is mounted, will degrade the performance of the power delivery system on a printed circuit board. For example, on a typical line card utilized in network hardware, there are more than ten ASICs directly mounted on the board and the pin number of each ASIC package could be well in excess of one thousand. With other BGA packages mounted on the board, the total number of plated through hole (PTH) vias is well beyond forty thousands. Therefore the number of the anti-pads on the power and ground planes is huge. Most of them are in an array pattern.

Generally speaking, for a single small anti-pad or the anti-pad pattern with a coarse density, the inductance and the capacitance obtained from a solid parallel plane transmission line model, calculated by equation (1), may still be valid for the power delivery system analysis; but for a dense anti-pad array right underneath an ASIC/BGA package, definitely a more accurate model should be used for that particular area on the power and ground planes to represent the effect of anti-pad array. An intuitive conclusion is that the cell inductance and resistance will increase because of the reduction of the current flowing capacity; and the cell capacitance will vary because of the variation of the effective area and the existence of the via structures that passing through the anti-pad array.

Now the question is what the impact of such variation on the power delivery system is; how much degrade will be posed to the power delivery system performance. This paper studies the anti-pad array impact and presents an approach to quantify the effect in simulation. This approach is verified by plugging the model into a commercial signal integrity software [4] for power delivery system analysis. Simulation results match measurement results up to several GHz frequency range. As a conclusion, this approach can effectively model the anti-pad array impact on the power delivery system and it can be easily adopted by available commercial software tools for power delivery system analysis and design.

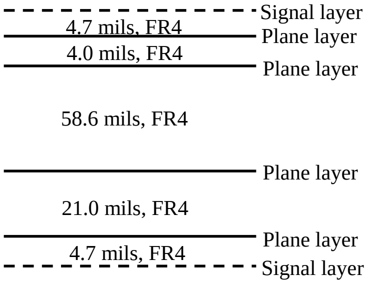
Measurement

Figure 2a shows two test structures. The only difference is that the right one has anti-pad array. The mark "**S**" indicates the shorting locations on the card for short case. Figure 2b illustrates the stackup. Two power/group separations of 4 mils and 21 mils have been studied. Figure 2c is a photograph of the impedance measurement lab setting [3].

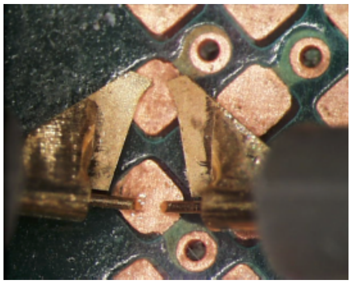


Without anti-pad array With anti-pad array

(a) Two test cards



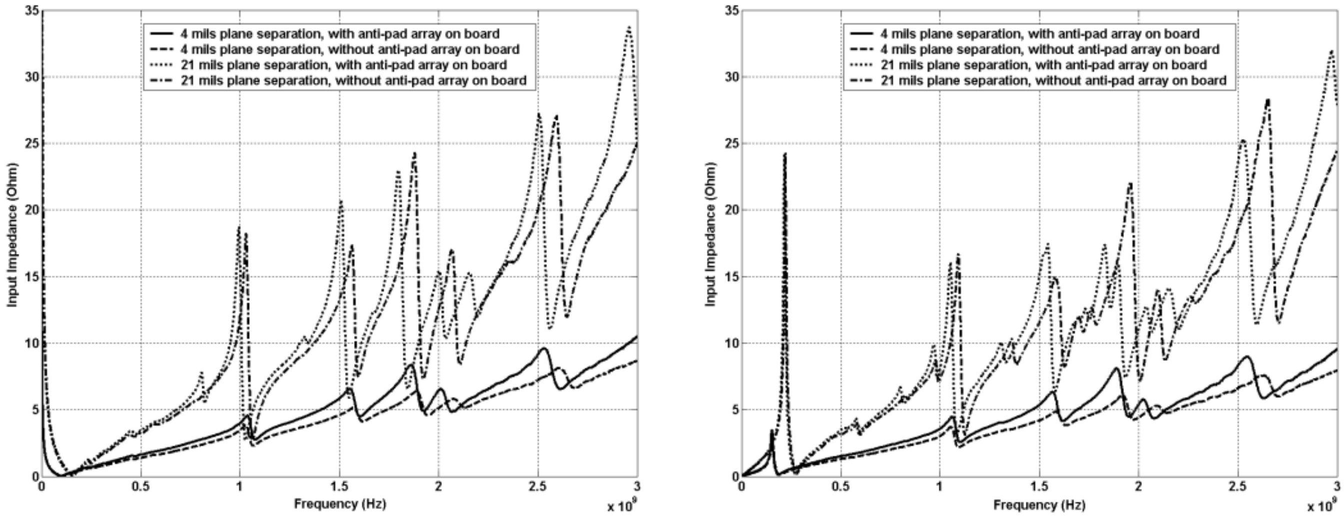
(b) Stackup



(c) Impedance measurement lab setting

Figure 2, test card used for measurement

For each structure, two measurements with open and short at those "S" locations are made. Figure 3 shows the measurement results with open and short on board respectively.



Open **Short**

Figure 3, measurement results for open and short on board

From the measurement results, it is obviuos that the anti-pad array exhibits different impact on 4 mils and 21 mils structures. For the structure with 4 mils plane separation, the impedance has been raised by 10% to 30%; for 21 mils structure, the resonant frequency has been shifted downward several tenths of MHz to 100MHz. According to the measurement results, ignoring the impact of anti-pad array at the design stage could lead to a weakened power delivery system.

3D Field Computation and Simulation Results

A straight and effective way to incorporate the anti-pad array impact is to change the cell R, L, G, and C for the area where the anti-pad array is located on the PCB. Five different structures in Figure 4 are computed by HFSS, a 3D full-wave electromagnetic field solver. A two-port S-parameter is first calculated, and the equivalent *R*, *L*, *G*, *C* parameters are extracted. A *k* factor is introduced to represent the anti-pad array impact. The *k* factor is defined as the ratio of the *R*, *L*, *G*, *C* parameter calculated from the structure with two anti-pad and a passing through via to the corresponding parameter calculated from the structure with solid planes. That is,

$$k_{R,L,G,C} = \frac{R,L,G,C_{\text{Two anti-pads with a passing through via}}}{R,L,G,C_{\text{Solid planes}}} \tag{2}$$

Figure 5 shows the *k* factors as a function of frequency for the structure with 4 mils plane separation.

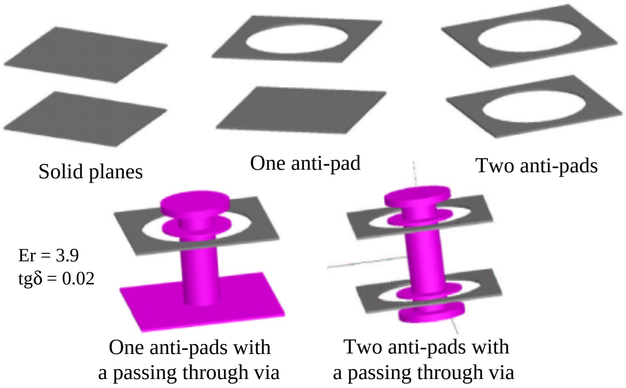


Figure 4, calculated structures

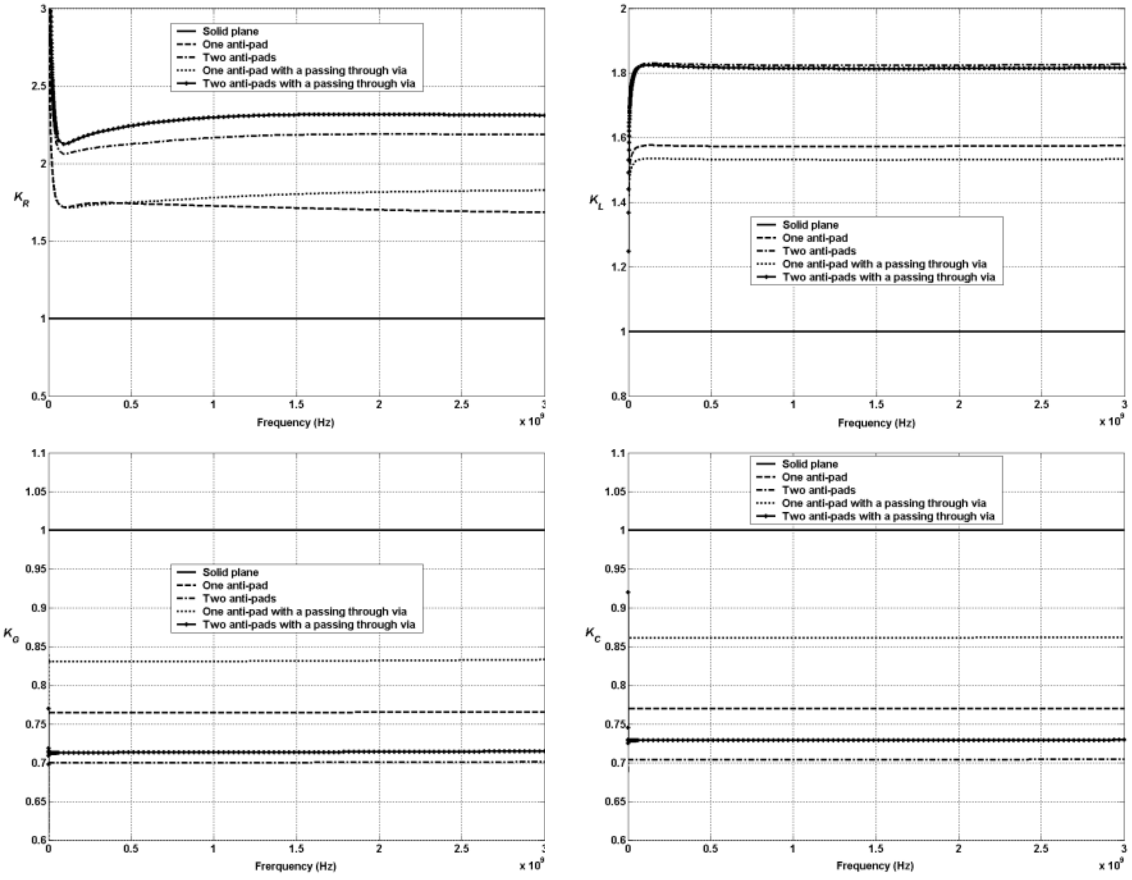


Figure 5, *k* factors for *R*, *L*, *G*, *C* parameters of the structure with 4 mils plane separation

	k_R	k_L	k_G	k_C
4 mils plane separation	2.30	1.850	0.714	0.729
21 mils plane separation	3.15	1.197	1.260	1.337

The table on the right lists the *k* factors that were used in simulation for both structures with 4 mils and 21 mils plane separations. It is worth to point out that the inductance and resistance always increase with the anti-pad array existing on the plane for both 4 mils and 21 mils structures. However the capacitance and admittance will be reduced for the 4 mils structure, but will increase for the 21 mils structure. This can be explained as the via capacitance could compensate the reduction of plane capacitance more for the 21 mils structure. Another phenomenon is the *k* factor remains constant for a reasonable broad frequency range.

Once the *k* factors are calculated, it is fairly straightforward to incorporate them into a spice circuit solver. The *RLGC* parameters adjustment is only for the area where anti-pad array is located on the PCB. This approach was successfully applied into SPEED2000 and the simulation results were compared with measurement results in Figure 6. It can be seen that this approach can effectively capture the characteristics of the real physical structures up to 1.5GHz frequency range. A frequency dependent *k* factor may improve the model accuracy beyond 1.5GHz.

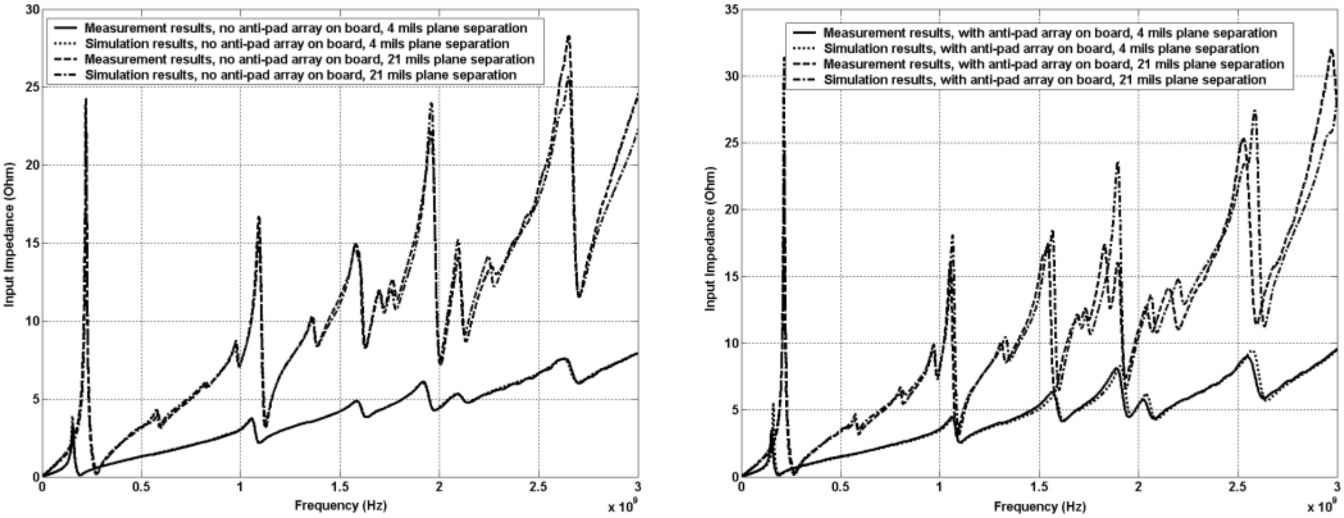


Figure 6, simulation results comparing with measurement results for the short case with or without anti-pad array

Conclusion

An effective approach for accurate consideration of anti-pad array impact on the power and ground planes is presented. Simulation and measurement comparison indicates that this approach is valid and the impact of the anti-pad array on the power delivery system has been captured up to several GHz.

Acknowledgement

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[3] I. Novak, “Probes and Setup for Measuring Power-Plane Impedances with Vector-Network Analyzer,” Proceedings of the 1999 DesignCon High-Performance System Design Conference, Feb. 1-4, 1999, Santa Clara, CA, pp. 201-215.
[4] See SPEED2000 User’s Guide and SPD file format on how to use area adjusted RLGC parameters.