

Impact of High Impedance Mid-Frequency Noise on Power Delivery

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ABSTRACT

In this paper, we present the core switching noise analysis of the power distribution system (PDS) for a signal processor on a card. The SPEED2000 [1], a spice and full-wave based simulation tool is used to study the frequency and transient responses of the core switching noise. The correlation between the result in frequency domain and time domain is discussed in detail. The frequency responses of the on-chip switching current and package current are introduced to illustrate that the noise level caused by the high impedance of the PDS is also frequency dependent.

I. INTRODUCTION

It is of increasing importance to design low impedance power delivery of microprocessors over a wide frequency band. Generally, the impedances of power distribution system (PDS) on packages and motherboards monotonically increase in frequency domain due to inductive effects with several resonant peaks caused by capacitive loops. On-chip decoupling capacitance with negligible parasitic inductance provides low power supply impedance at high frequency (above hundreds of MHz). Highest impedance peaks in frequency range of a few MHz to tens of MHz, called mid-frequency noise, are reduced by placing discrete de-coupling capacitors across the power rail in motherboards. How low the maximum impedance has to be is a very difficult question to answer. The formula of the target impedance described in [2] is a simple guideline for designers to follow, but becomes a very difficult goal to achieve due to decreasing operating voltage and faster and larger current transients. For example, assuming 10% tolerance or 120 mV maximum allowable noise on a 1.2 V supply with 100 A average current demand, the target impedance for the PDS is

$$\text{Target impedance} = (1.2 \text{ V}) \times 10\% / (100 \text{ A}) = 1.2 \text{ m}\Omega \quad (1)$$

To meet this target impedance over the mid-frequency range, a huge amount of decoupling capacitors need to be placed. This paper demonstrates that the target impedance is not necessary to be met at mid-frequency range. The impact of the mid-frequency noise is frequency dependant. In this paper, we demonstrate the correlation between the impedance of PDS over frequency and the voltage variation in time domain, and define an appropriate design approach for power delivery.

II. SIMULATION METHODOLOGY

The simulations were carried out using a commercial software tool from Sigrity, SPEED2000. This solver performs Spice-based and full-wave-electrodynamic analysis of complex high-speed PC boards and planar-chip packages as complete 3-D entities. Based on finite difference time domain (FDTD) method, the tool is able to characterize ground bounce and power droop, and determine the choice of distributed decoupling capacitors. The simulation methodology and validation using SPEED2000 are described in detail in [3]. The layout shown in Fig. 1 is the evaluation verification measurement (EVM) board for the core power distribution noise analysis. The blocks of interest include a signal processor unit on a BGA (Ball Grid Array) package and a voltage regulator module (VRM). The board is 330 mm by 90 mm, consisting of five signal layers, two voltage planes, and five ground planes. The system was powered by connecting an ideal voltage supply, 1.2 V, at the location of the VRM. The on-board decoupling capacitors are located in the backside of the board under the BGA package.

The core on-chip switching has been modeled as a current source, which is connected to all power/ground vias at the top of the package. From the SPICE simulation and the measurement, the current source can be represented approximately as a periodic triangular pulse. The current source is in parallel with one RC element (6.25 m Ω , 40 nF), representing on-chip decoupling capacitors. The current source switches at 2 ns cycle and each cycle has 400 ns rise time and 1.2 ns fall time. There are two operation cycles to be considered: non-operation cycle and full-operation cycle. The nominal average current demands during non-operation and full-operation cycles are experimentally determined to be 0.5 A and 2 A, respectively. Fig. 2 shows the current waveform flowing from the source on chip into the PDS through the package vias.

III. RESULTS

The two cases to be discussed are the same power distribution systems with two different sets of on-board decoupling capacitors listed in Table I. The impedances of the PDS in these two cases are shown in 3(a) and (b). The magnitude of the impedance is seen from the current source on the device into the power distribution system including on-chip decoupling capacitance, the BGA package, the EVM board, on-board decoupling capacitors and the short circuit at the location of the VRM. The impedance in the case I has two impedance peaks with the magnitude over 200 mΩ at 68 MHz and 2.75 MHz. In the case II, there is a high impedance peak with the magnitude of 723 mΩ at 68 MHz. If the maximum allowable noise, 120 mV, is assumed, those impedance peaks are far higher than the target impedance, 60 mΩ, from (1).

In the transient simulation, the current starts continuously switching at time zero in non-operation cycles and switches to the full-operation cycle after 800 ns in case I and after 600 ns in case II. The voltage variations at the current source and at the solder balls of the package are shown in Fig. 4. Three oscillations are found in the voltage curves. First, high-frequency noise oscillates at the switching frequency of the current source, 500 MHz. The magnitude of this noise is linearly proportional to the magnitude of the current source. Second, the mid-frequency noise oscillates at 68 MHz right after the transition, but the ringing vanishes within 80 ns. The third noise, oscillating at 2.75 MHz and causing severe overshoot and long ringing, is the one we have to pay more attention to reduce. In the case II, all tantalum capacitors are replaced by ceramic capacitors with low equivalent series resistance and one half of the ceramic capacitors are changed from 0.01 uF to 0.1 uF. Thus, the resulting impedance in the case II is decreased at several MHz range, but increased to 723 mΩ at 68 MHz as shown in Fig 3(b). However, from the transient simulation result shown in Fig. 5, the noise at 68 MHz does not cause bigger ringing and the overall voltage variation in the case II is less than the case I. Although the maximum impedance is more than 100 times higher than the target impedance, the overshoot is below 60 mV. This ringing in case II can be further reduced by placing a few more of 0.01 uF capacitors, but the impedance at 68 MHz does not have to be as small as required at a few MHz range.

We should consider the current demand in frequency domain. Fig. 6 shows the currents from the source, into the on-chip decoupling capacitor, and into the package in the non-operation cycle of the case I. The on-chip capacitors rapidly source and sink the high-speed switching current and only the amount of its current envelope waveform containing low- and mid frequency components flows into the package and the board. Since the package and the PCB have relatively high impedance at 2.75 MHz and 68 MHz, the energy at these two frequencies reflects back and forth between the chip and the rest of the PDS. Those reflected current flows into and out from the on-chip decoupling capacitance and causes the voltage variation on the chip at those frequencies. Since the current flowing into the package oscillates at much slower frequency than the source current does, the maximum current magnitudes, in both cases, seen at the package are only 0.43 A and 1.59 A in non-operation cycles and full-operation cycles, respectively. Fig 7 shows the dB magnitude spectrum of the currents from the source, into the on-chip decoupling capacitors, and into the package in both cases. The current source is a periodic triangular pulse with 2 ns period. The Fourier transform of this waveform shown in Fig 7(a) is a sinc square function at DC and harmonics of 500 MHz. The “energy windows”, where the source spectrum in significant magnitude appears, are at near DC to several MHz and at the harmonics. A well-designed PDS should be low impedance at those windows. The impedance outside these windows can be tolerably higher. Fig 7(c) ~ (e) show the on-chip decoupling capacitance in an amount of 40 nF sources and sinks most of the harmonic currents above hundreds of MHz, but also resonates at 2.75 MHz and 68 MHz where the high impedances of PDS are. We can further reduce the impedance at 68 MHz by placing more 0.1 uF capacitors, but the target impedance at this frequency does not have to be as small as what is needed in a few MHz range.

Table I Number and Parameters of On-Board Decoupling Capacitors

| | |
|---------|--|
| Case I | 28 x 0.01uF: ERL= 0.9 nH, ESR = 0.3 Ω, ceramic X7R, 0603 4 x 10 uF : ESL = 1.5 nH ESR = 1 Ω, tantalum |
| Case II | 14 x 0.01uF, ERL= 0.9 nH, ESR = 0.3 Ω, ceramic X7R, 0603 14 x 0.1uF, ERL= 0.9 nH, ESR = 0.08 Ω, ceramic X7R, 0603 4 x 10 uF, ESL = 1.5 nH ESR = 0.03 Ω , ceramic Y5V, 1206 |

IV. CONCLUSION

Power distribution analysis in frequency domain is insightful to help identify the oscillation frequencies of the system and determine suitable decoupling capacitors. The current waveform of the on-chip switching can be approximated as a periodic triangular function and its frequency response is a sinc square function at DC and harmonics of the current switching frequency. On-chip capacitors in tens of nF range should be able to provide low impedance above several hundreds MHz range. The PDS in a package and a board should be designed as a low pass filter with a bandwidth over the frequency spectrum of a single current pulse. Faster switching circuits usually result in a narrower current pulse. The narrower the single current pulse is, the wider the bandwidth has to be. It is very difficult to quantify the noise and determine the target impedance through calculation of Ohm's law because of the complexity of the system and interaction of the many components. However, since the magnitude of the current spectrum reduces in frequency below the circuit switching frequency, the target impedance of PDS should also increase in frequency. That is the reason that the high impedance at tens of MHz has less impact on noise than the one at a few MHz. To avoid an over designed system, an appropriate transient simulation has been conducted to observe the impact of each oscillation at mid-frequency and to determine the number and the value of the decoupling capacitors.

ACKNOWLEDGMENT

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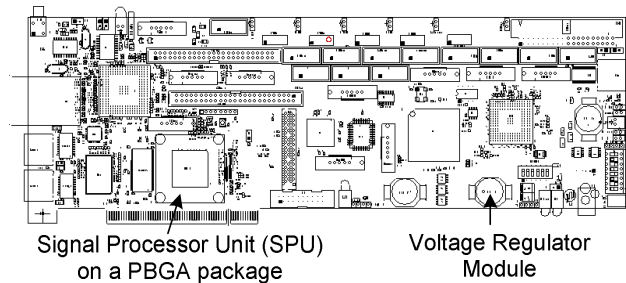


Fig. 1 The system board of the signal processor in size of 330 mm x 95 mm for delta-I noise analysis. The on-board decoupling capacitors listed in Table I are located in the backside of the board under the signal processor.

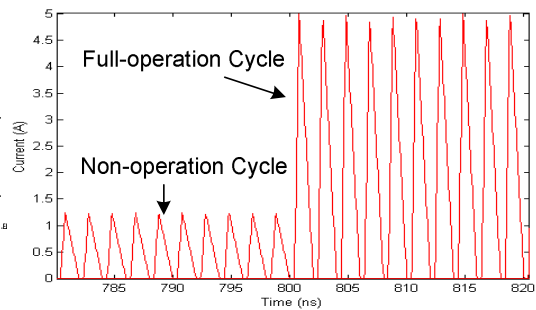


Fig. 2 Current source wave form with 2 ns period, 0.4 ns rise time and 1.2 ns fall time. The average currents are 0.5 A and 2 A in the non-operation cycle and the full-operation cycle, respectively.

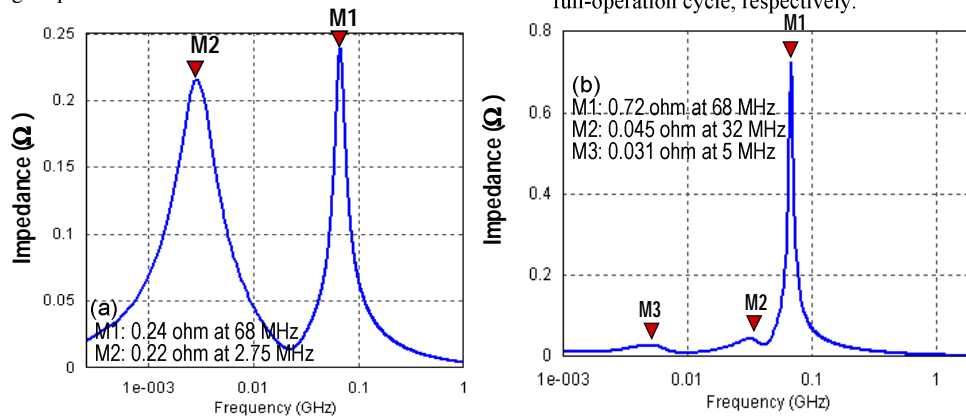


Fig. 3 The impedance of the power distribution system in (a) case I and (b) case II listed in Table I. The magnitude of the impedance looks from a circuit on the SPU processor into the package and the board.

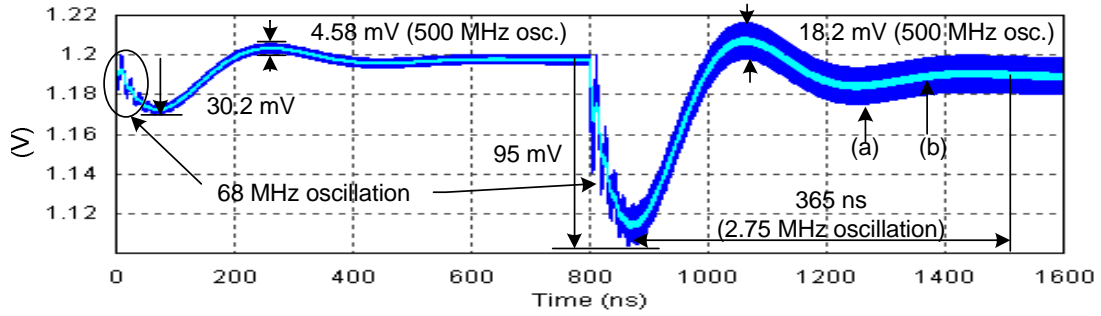


Fig. 4 Voltage variation (a) at current source and (b) at the solder balls of the PBGA package with the case I capacitors listed in Table I.

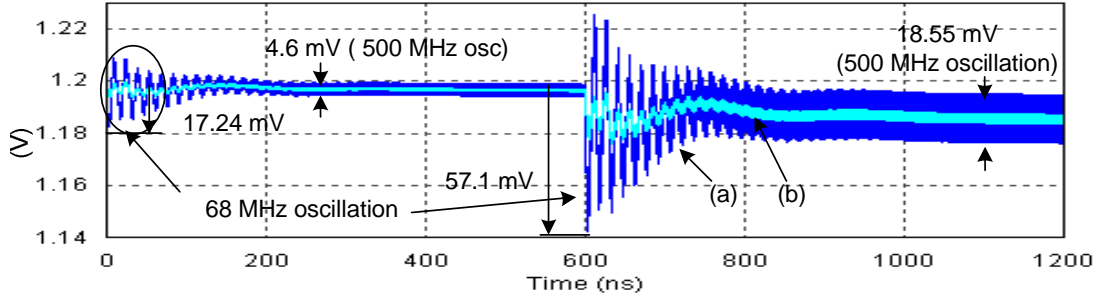


Fig. 5 Voltage variation (a) at current source and (b) at the solder balls of the PBGA package with the case II capacitors listed in Table I.

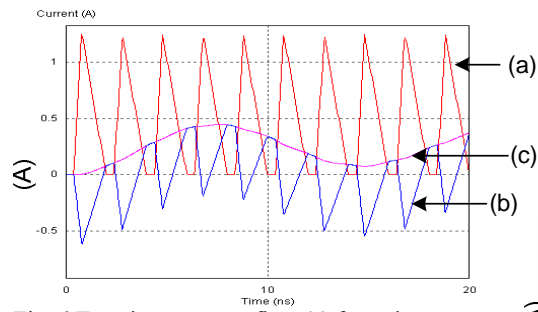


Fig. 6 Transient currents flow (a) from the source (b) into the on-chip capacitor (c) into the package in the non-operation cycle in case I.

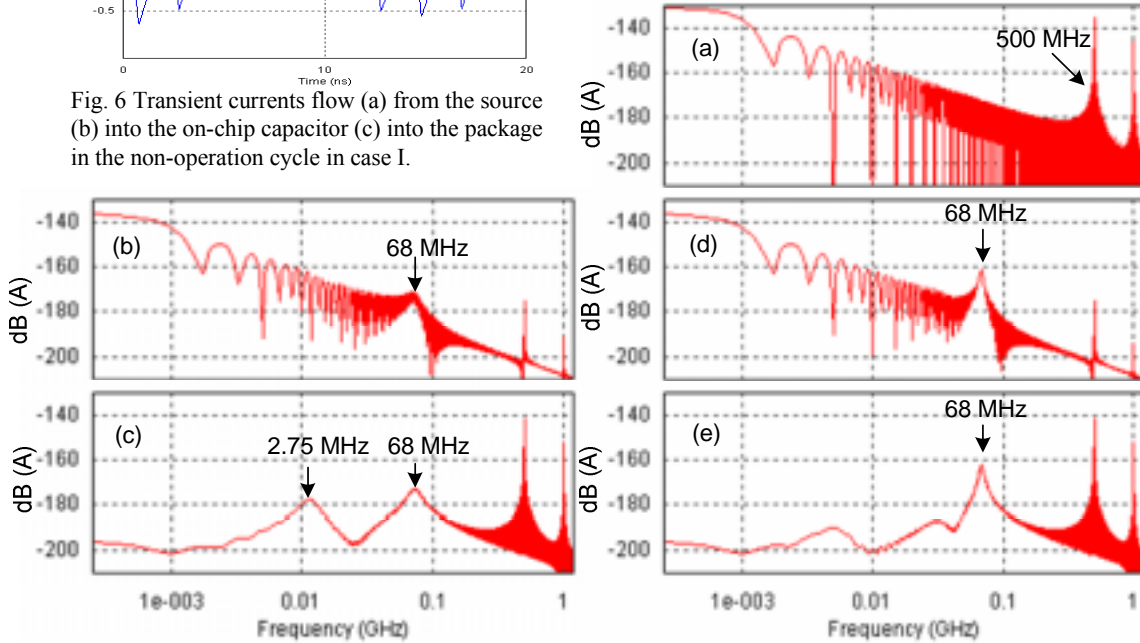


Fig. 7 The DB magnitude spectrum of the currents (a) from the source, (b) into the on-chip decoupling capacitor in case I, (c) into the package in case I, (d) into the on-chip decoupling capacitor in case II and (e) into the package in case II.