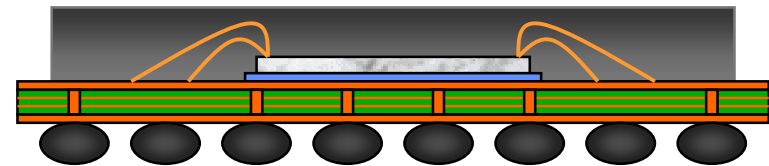
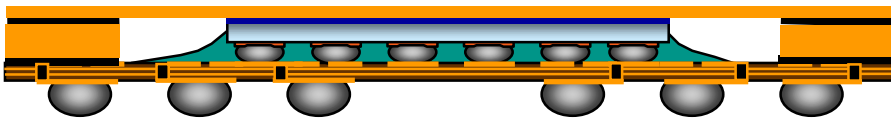


MINDSPEED™

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Impact of High Impedance Mid-Frequency Noise on Power Delivery

Jennifer Hsiao-Ping Tsai



- Generally, the impedances of power distribution system (PDS) on packages and motherboards monotonically increase in frequency domain due to inductive effects with several resonant peaks caused by capacitive loops.
- On-chip decoupling capacitance with negligible parasitic inductance provides low power supply impedance at high frequency (above hundreds of MHz).
- Highest impedance peaks in frequency range of a few MHz to tens of MHz are reduced by placing de-coupling capacitors across the power rail in motherboards.
- The formula of the target impedance introduced by Larry Smith is a very difficult goal to achieve due to decreasing operating voltage and faster and larger current transients. In our case,

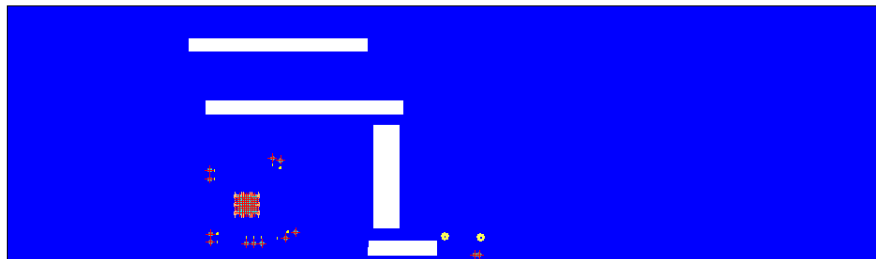
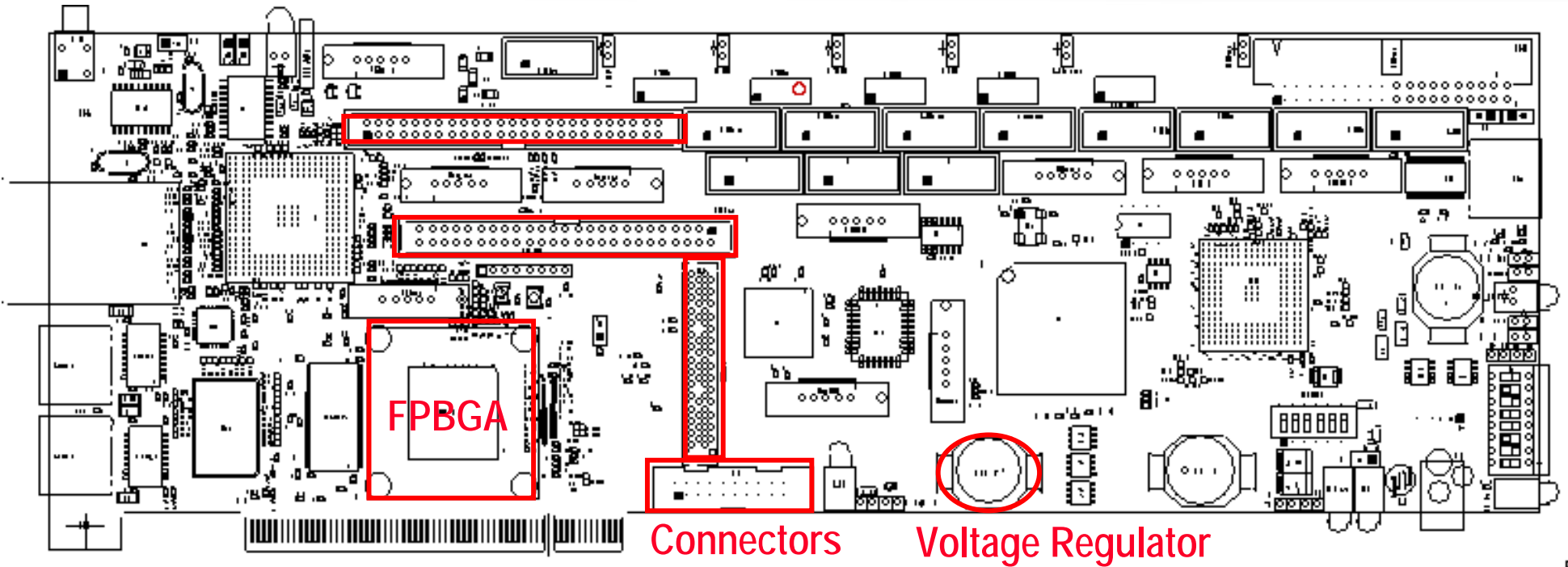
$$\text{Target impedance} = (1.2 \text{ V}) \times 10\% / (2 \text{ A}) = 60 \text{ m}\Omega$$

- A huge amount of decoupling capacitors need to be placed, to meet this target impedance over the mid-frequency range.
- This paper illustrates that the target impedance is frequency dependant.
- The correlation between the impedance of PDS over frequency and the voltage variation in time domain is demonstrated, and an helpful simulation methodology for power delivery is defined.
- The simulations were carried out using a commercial software tool from Sigrity, SPEED2000.



Power Distribution System of the EVM board

Dimension of the Board: $\Delta x = 330$ mm, $\Delta y = 95$ mm

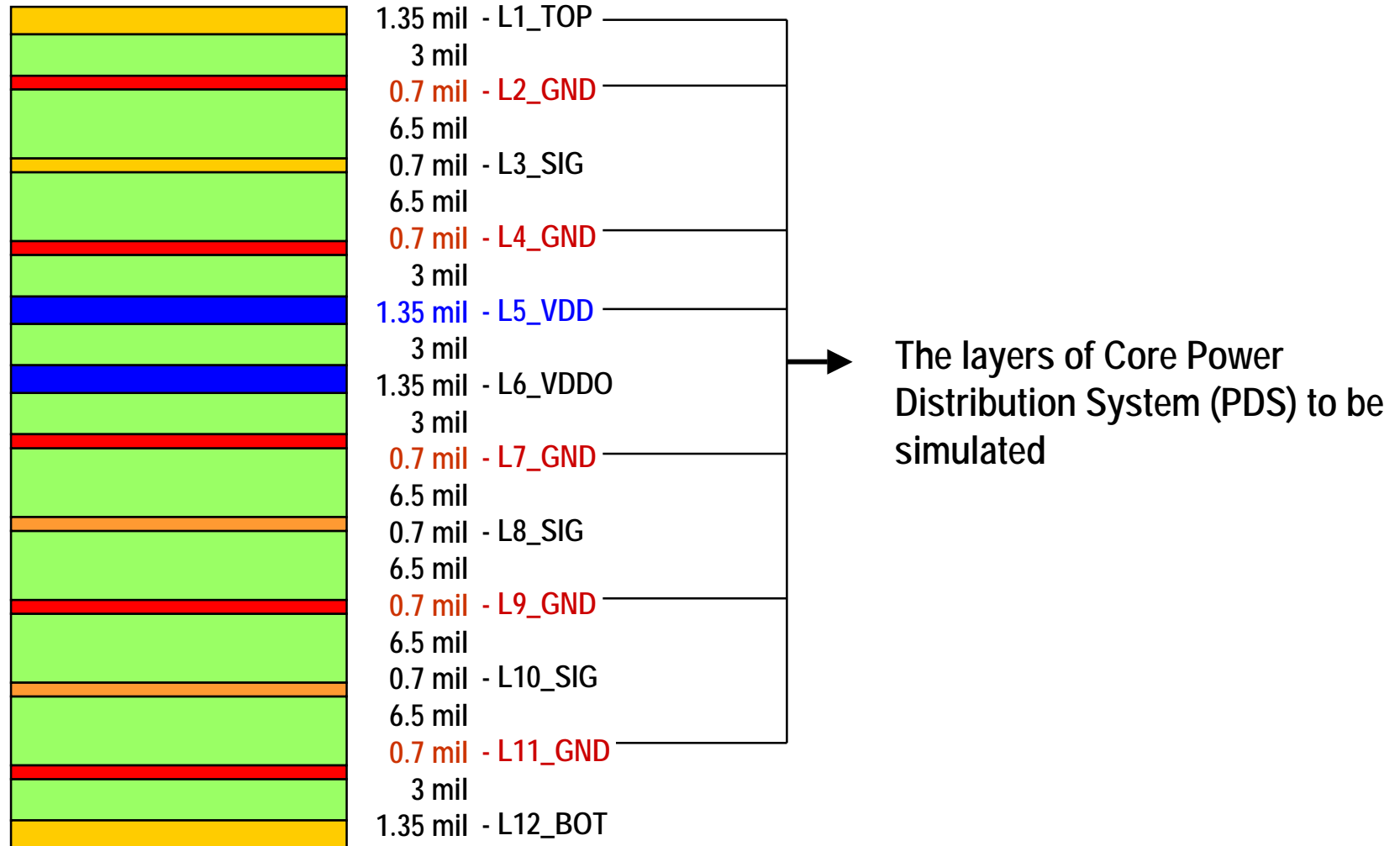


GND plane
Two empty slots represent vias of the connectors

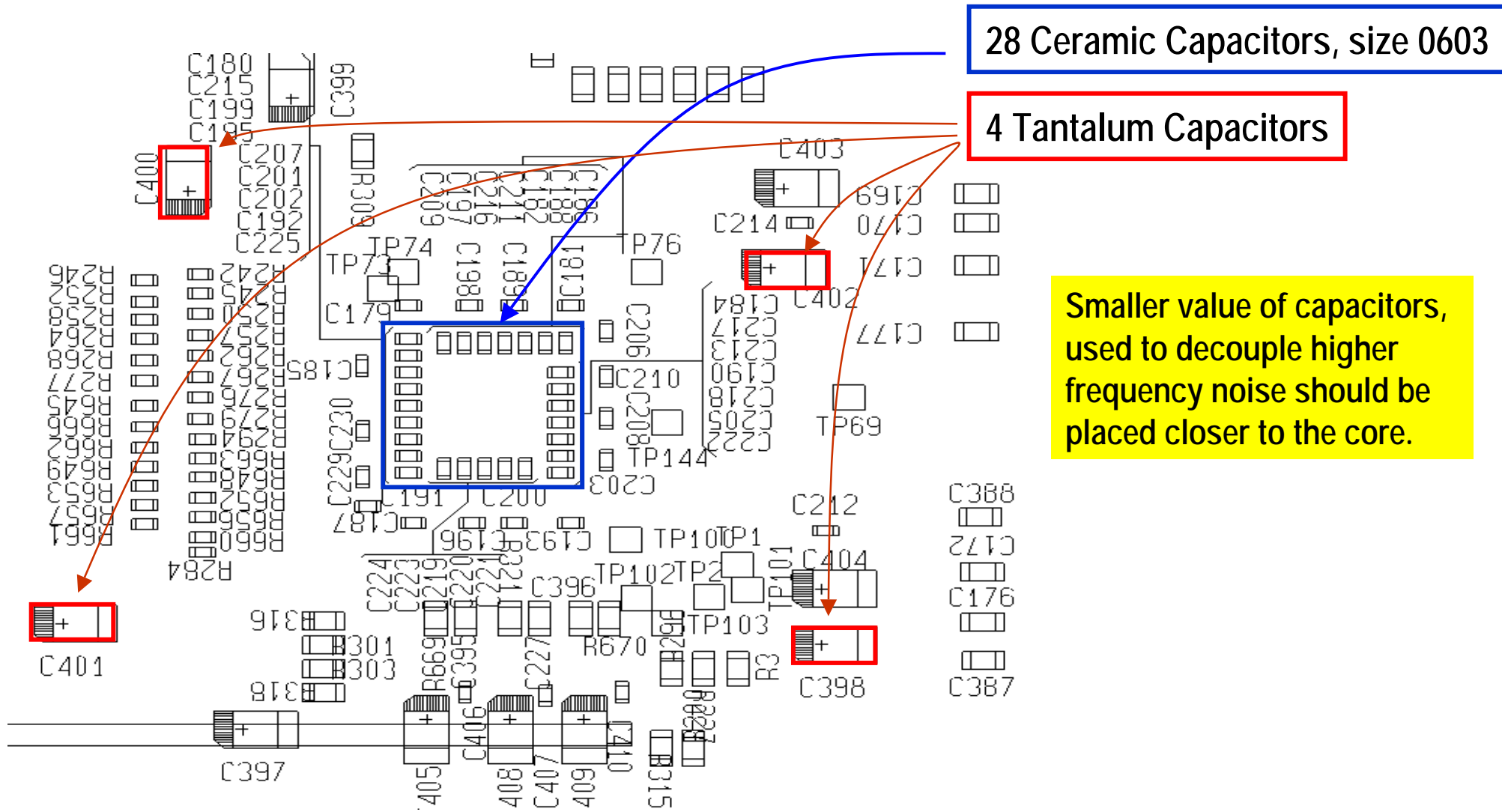


PWR plane
A jumper between two metal is modeled as a 8nH inductor.

The Stackup of the EVM Board



Decoupling Capacitors at the Bottom Side of the Board



28 Ceramic Capacitors, size 0603

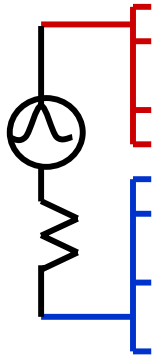
4 Tantalum Capacitors

Smaller value of capacitors, used to decouple higher frequency noise should be placed closer to the core.

Impedance Calculation of the EVM Board

3D full wave model of the board

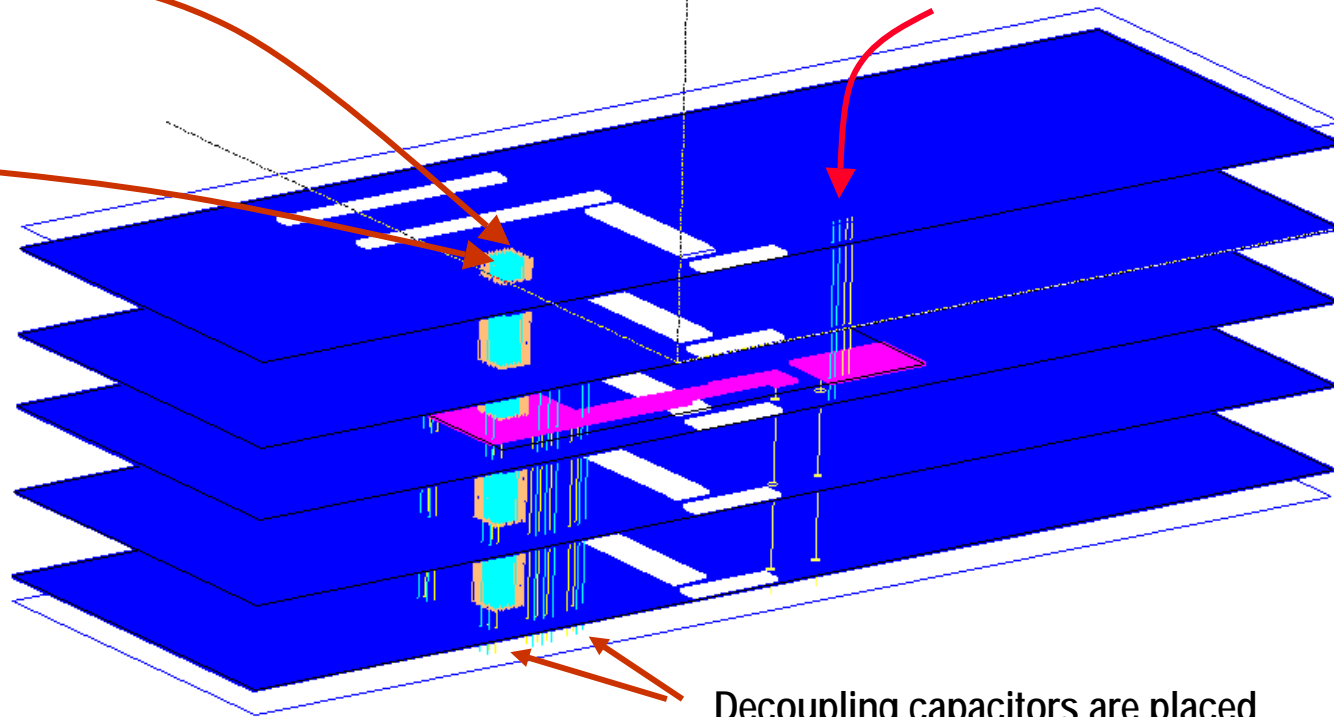
Gaussian source excitation
at the top of the board



Connect to
VDD vias

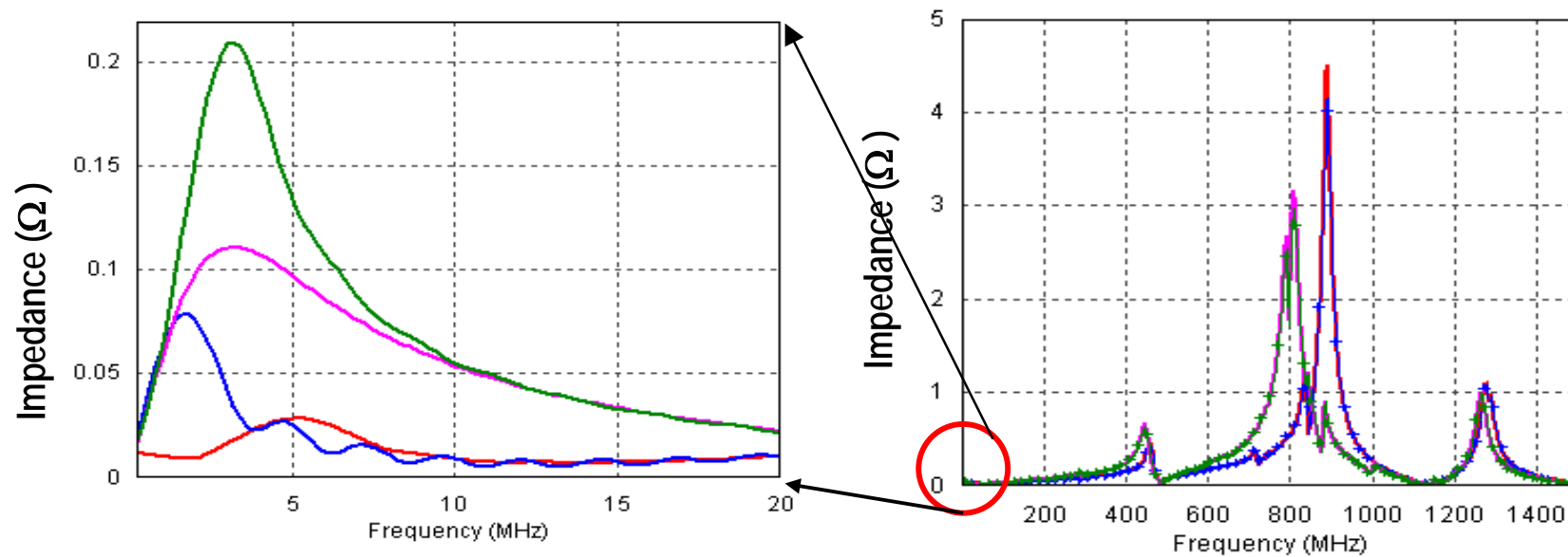
Connect to
VSS vias

VDD and VSS nets are shorted at
the location of the voltage
regulator Module



Decoupling capacitors are placed
at the bottom side of the board

Impedance of the Board vs. Decoupling Capacitors



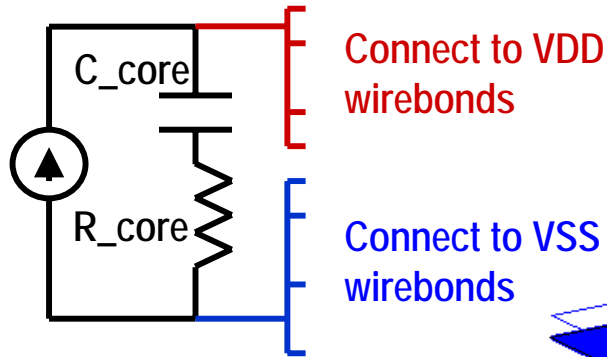
Curves	# of 0.01 uF (0.38 nH, 0.23 Ω)	# of 0.1 uF (0.69 nH, 0.12 Ω)	# of 10 uF (1nH)	ESR of 10 uF	Peak impedance
Green	28	0	4	1 Ω (tantalum)	210 mΩ at 3.2 MHz
Magenta	28	0	4	0.5 Ω (tantalum)	110 mΩ at 3 MHz
Blue	14	14	4	0.5 Ω (tantalum)	78.4 mΩ at 1.8 MHz
Red	14	14	4	0.03 Ω (ceramic Y5V 1206)	28.5 mΩ at 5.2 MHz

- The impedance peaks above operating frequency has less significant effect on power distribution system. However, a impedance bump below 10 MHz can cause big undershoot and long ringing.
- 10 uF capacitors with different ESR affect the impedance only below 10 MHz, which determines the magnitude of the voltage overshoot in this case.

Transient Simulation of the EVM Board

3D full wave model of the board

On-chip switching
circuit model

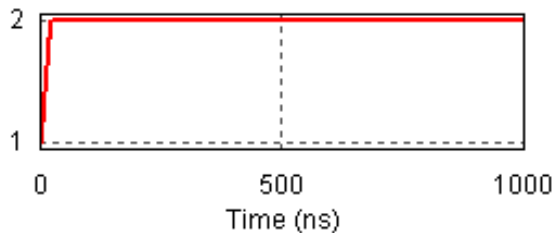


Current source in parallel with
On-chip decoupling capacitance

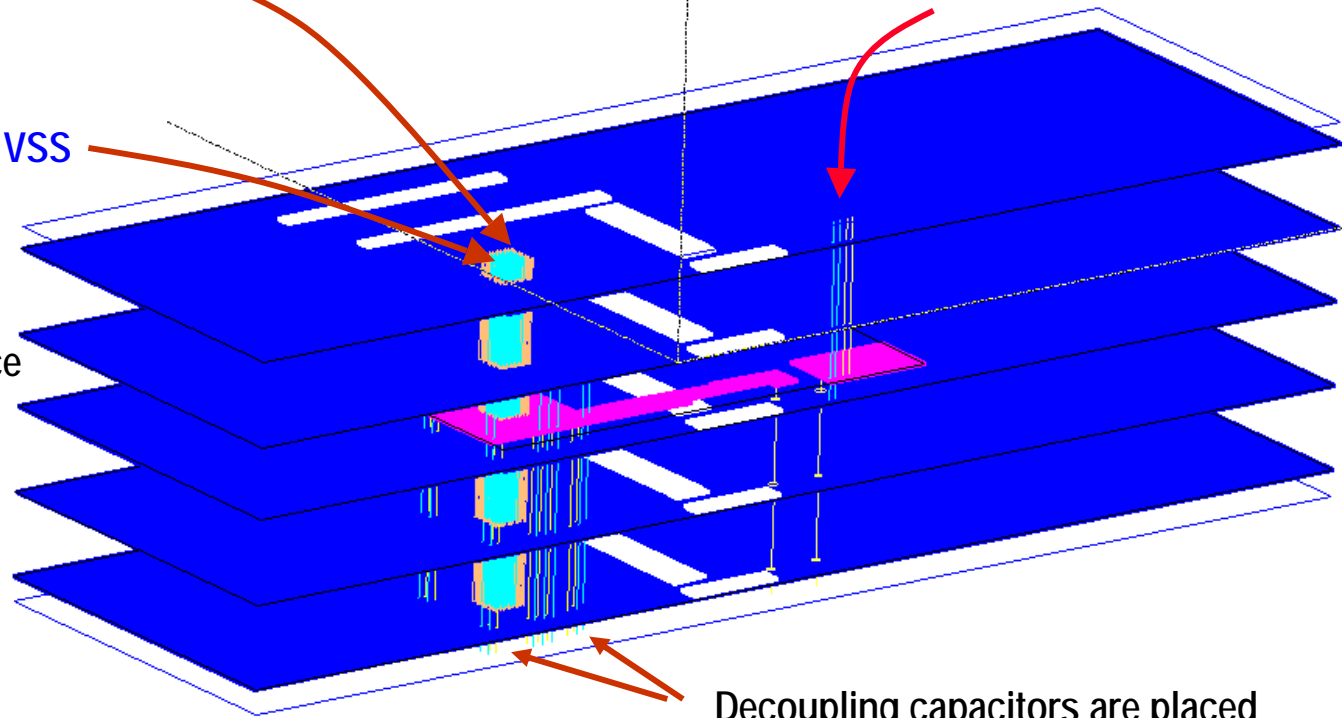
$C_{core} = 40 \text{ nF}$

$R_{core} = 0.625 \text{ m}\Omega$

Current source (A)



VDD and VSS nets are shorted at
the location of the voltage
regulator Module

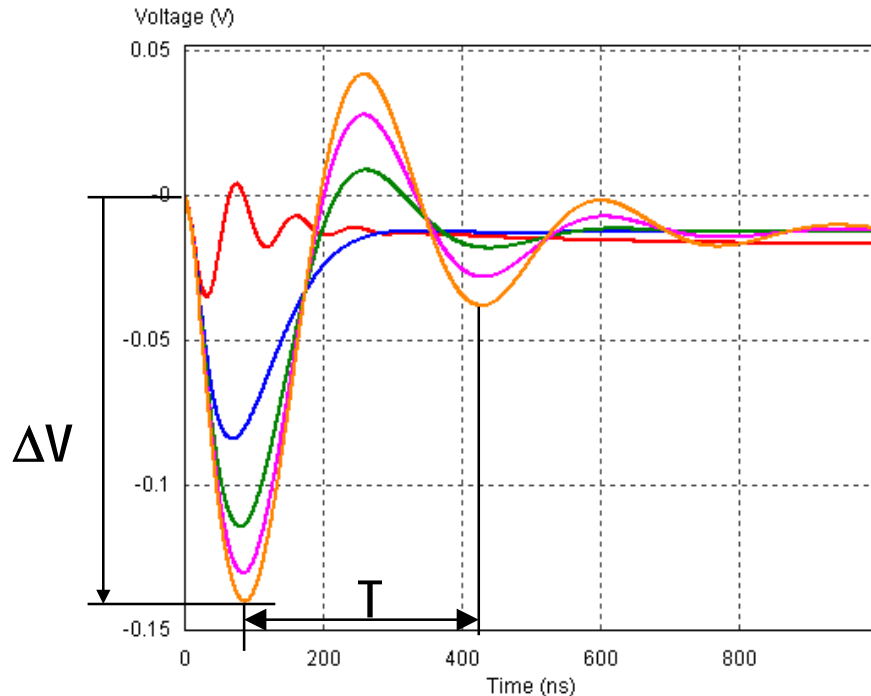


Decoupling capacitors are placed
at the bottom side of the board

Supply Voltage Droop vs. ESR of Decoupling Capacitors

A pulse current, switching from 1 A to 2 A at $t = 0$, is applied at the top of the board.

Capacitor	Number	ERL	ESR	Type	Size	Self Resonant Freq.
0.01 μF	28	0.9 nH	0.3 Ω	Ceramic X7R	0603	63 MHz
10 μF	4	1.5 nH	0.03 Ω for Ceramic Y5V 0.5 ~ 2 Ω for tantalum		1206	1.3 MHz



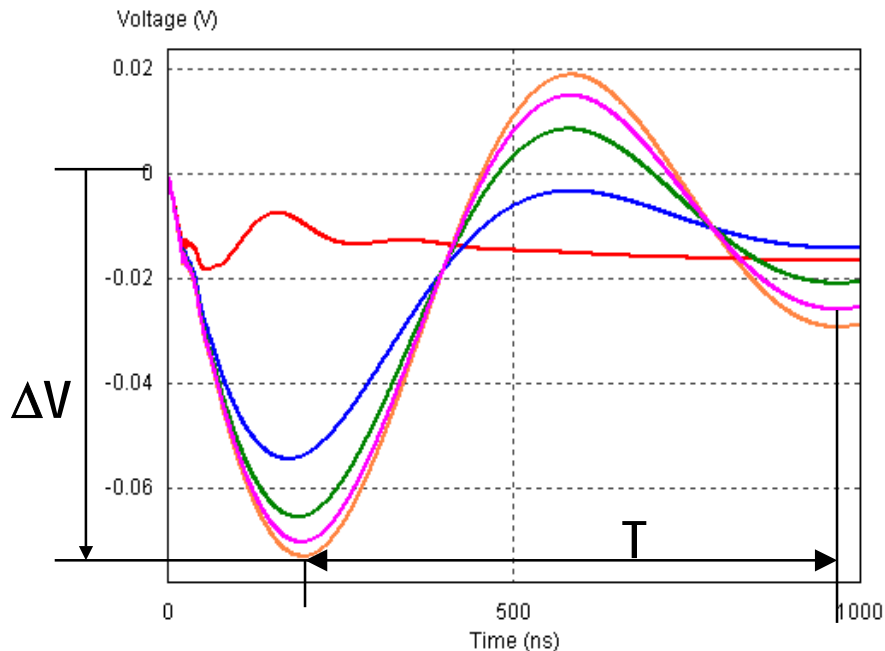
Curves	ESR of 10 μF	ΔV	Period, T	Frequency, 1/T
Red	0.03 Ω	35.2 mV	86 ns	11.6 MHz
Blue	0.5 Ω	83.8 mV	No ripple	No ripple
Green	1.0 Ω	114 mV	360.17 ns	2.78 MHz
Magenta	1.5 Ω	130 mV	347.88 ns	2.87 MHz
Orange	2.0 Ω	139.4 mV	345.77 ns	2.89 MHz

When the four tantalum capacitors are replaced by low ESR ceramic capacitors, the noise magnitude reduced at least 60%.

Supply Voltage Droop v.s. ESR of Decoupling Capacitors

A pulse current, switching from 1 A to 2 A at $t = 0$, is applied at the top of the board.

Capacitor	Number	ERL	ESR	Type	Size	Self Resonant Freq.
0.01 uF	14	0.9 nH	0.3 Ω	Ceramic X7R	0603	63 MHz
0.1 uF	14	0.9 nH	0.08 Ω	Ceramic X7R	0603	18 MHz
10 uF	4	1.5 nH	0.03 Ω for Ceramic Y5V 0.5 ~ 2 Ω for tantalum		1206	1.3 MHz



Curves	ESR of 10 uF	ΔV	Period, T	Frequency, 1/T
Red	0.03 Ω	18.2 mV	220.7 ns	4.5 MHz
Blue	0.5 Ω	54.3 mV	807.98 ns	1.2 MHz
Green	1 Ω	65.4 mV	772.17 ns	1.3 MHz
Magenta	1.5 Ω	70.1 mV	795.92 ns	1.3 MHz
Orange	2 Ω	72.9 mV	769.5 ns	1.3 MHz

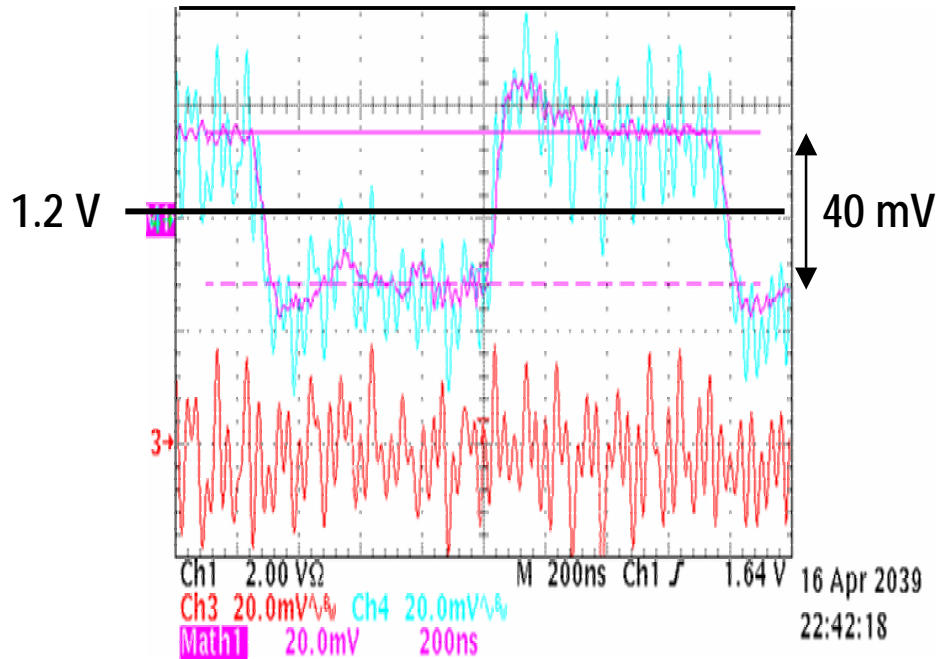
When the four tantalum capacitors are replaced with low ESR ceramic capacitors and a half of 0603 ceramic capacitors are replaced with 0.1uF values, the noise magnitude reduces.

Measurement of Power Droop on the Board

A pulse current, switching from 1 A to 2 A, is applied at the top of the board.

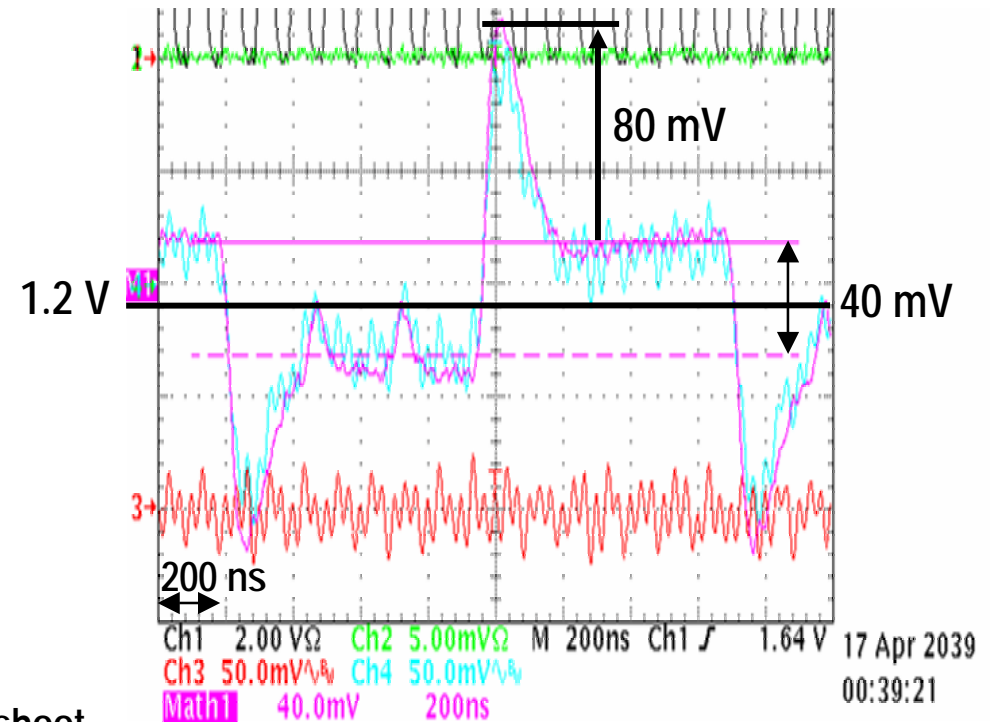
Decoupling capacitors: 28 x 0.01uF, TDK, size 0603
4 x 10 uF, TDK, tantalum

The Voltage Measured at Voltage Regulator Output



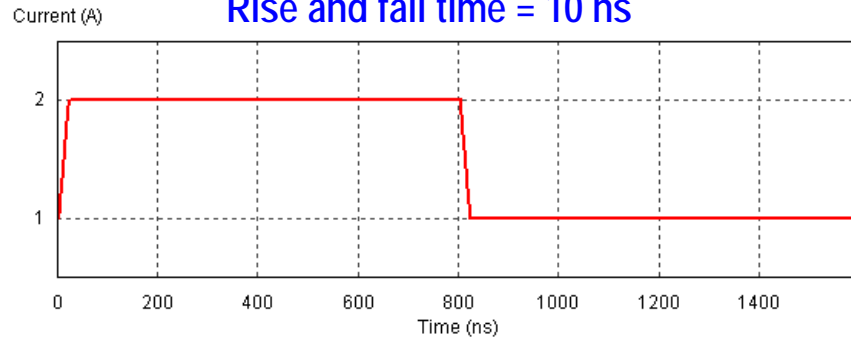
Supply voltage has 40 mV variation and 10 mV overshoot.

Voltage on the Bottom of the Board Across 10 uF Cap



Simulation to Be Correlated to Measurement

Current source on the top of the board
Rise and fall time = 10 ns



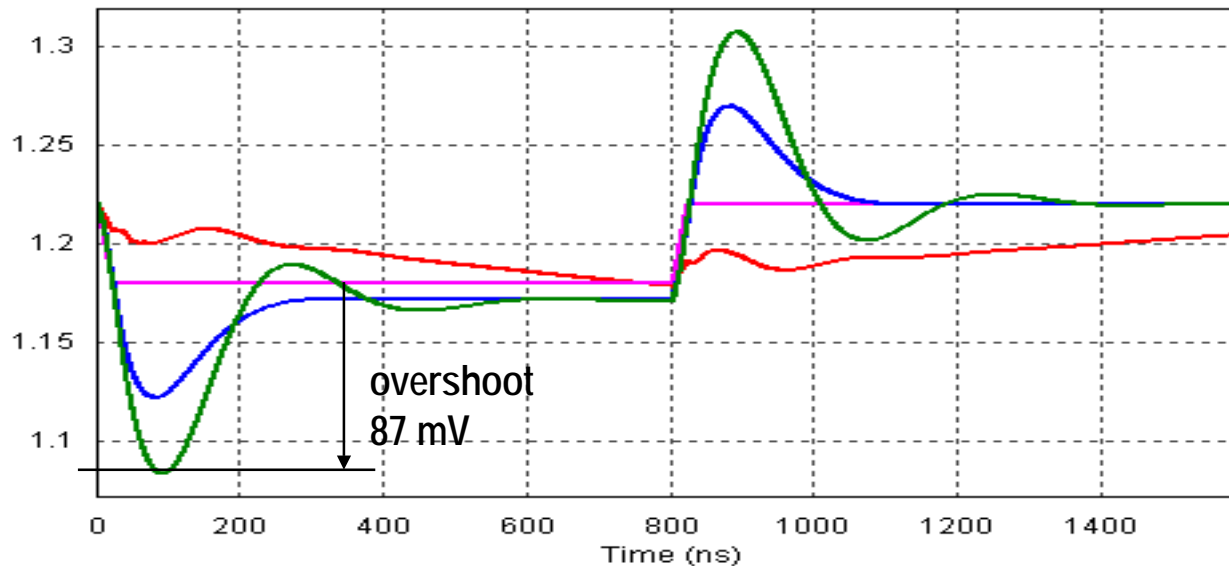
Curves	# of 0.01 uF	# of 0.1uF	# of 10 uF	ESR of 10uF	Overshoot
Red	14	14	4	0.03 Ω	None
Blue	28	0	4	0.5 Ω	49.7 mV
Green	28	0	4	1 Ω	87 mV

0.01uF, ERL= 0.9 nH, ESR = 0.3 Ω, Size 0603

0.1uF, ERL= 0.9 nH, ESR = 0.08 Ω, Size 0603

10 uF, ESL = 1.5 nH, Size 1206

Voltage (V)



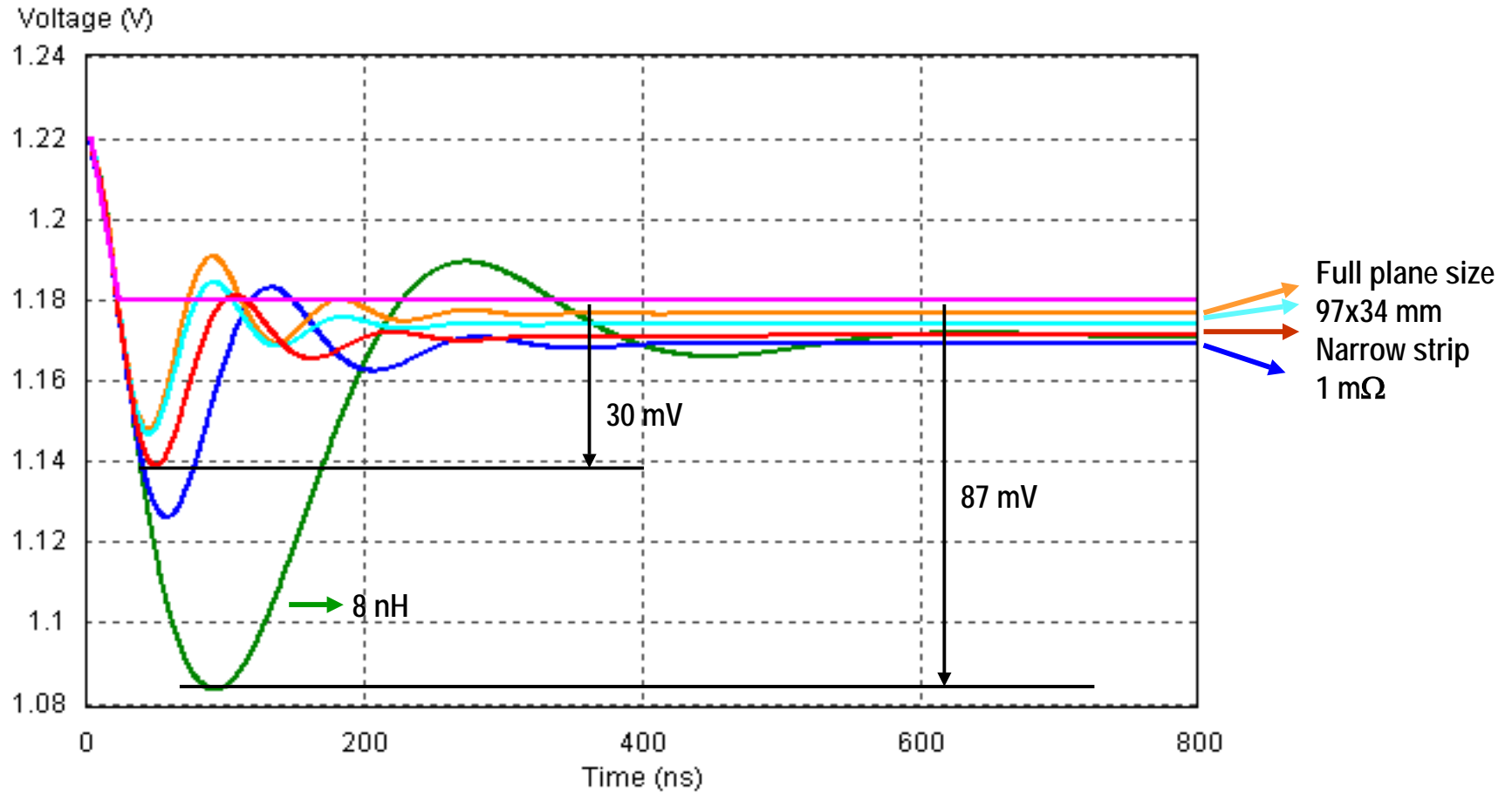
Magenta: Voltage source at VRM location
for comparison with measurement

The Effect of the Jumper Model on Supply Droop

Decoupling capacitors:

28 x 0.01uF: ERL= 0.9 nH, ESR = 0.3 Ω , Size 0603

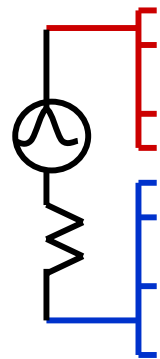
4 x 10 uF : ESL = 1.5 nH ESR = 1 Ω





Power Distribution System of the Package and the EVM Board

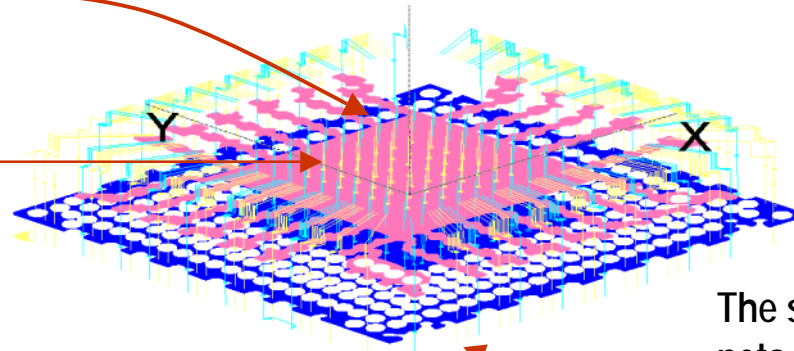
Impedance Simulation of the Package



Connect to
VDD wirebonds

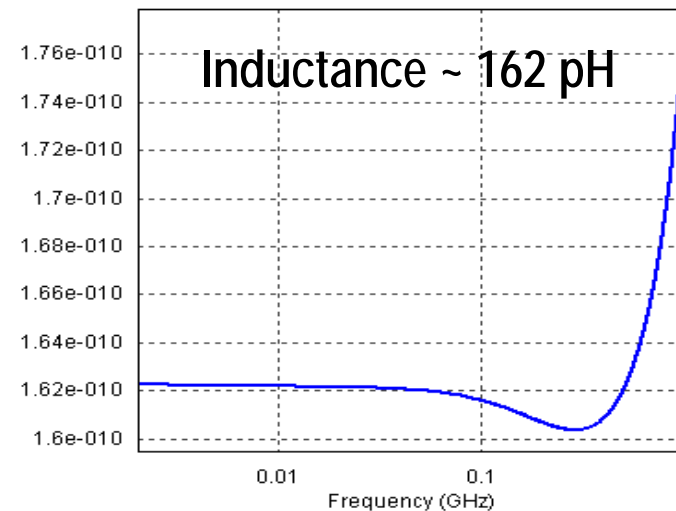
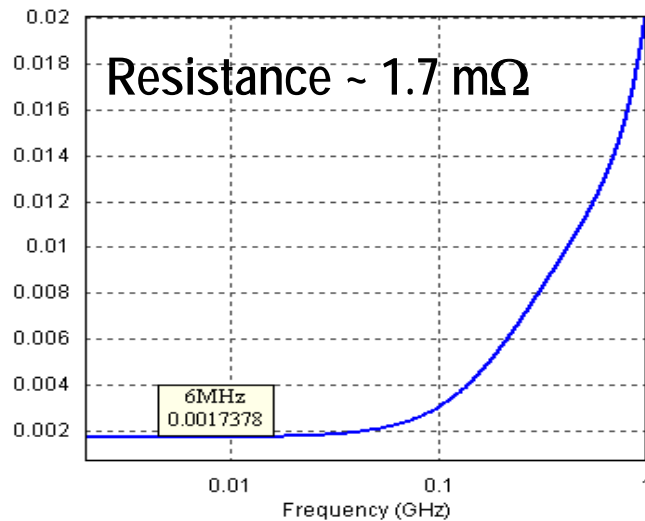
Connect to
VSS wirebonds

3D full wave model of the package



The solder balls of VDD and VSS nets at the bottom of the package are shorted

Gaussian source excitation
at the top of the package

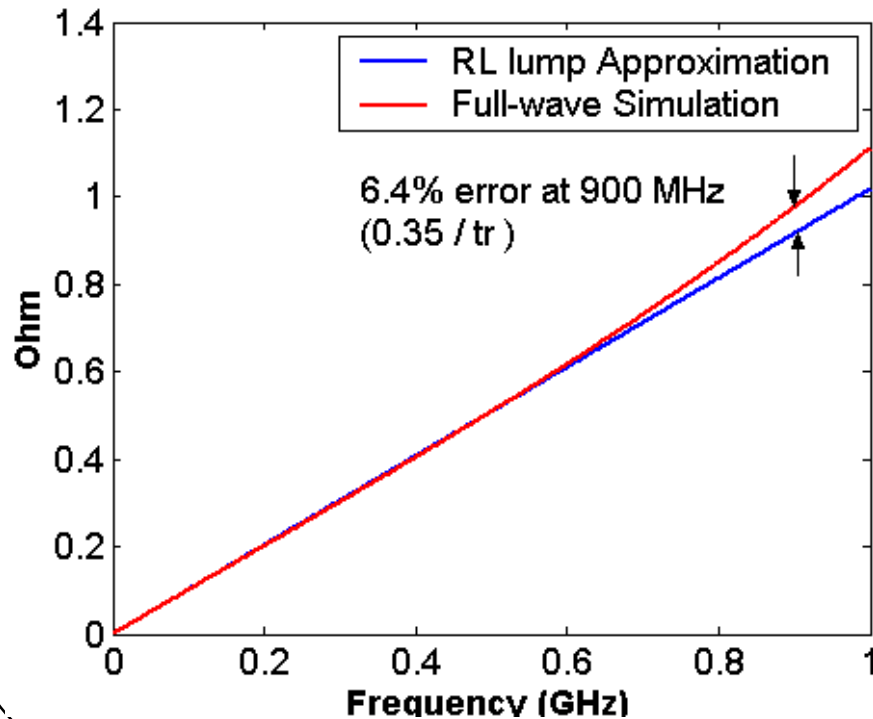


Models of Package and On-chip Switching

Through full wave simulation of the real package geometry and curve fitting, the equivalent RL model of the package is extracted.

$$Z_{pkg} = R_{pkg} + j\omega L_{pkg}$$

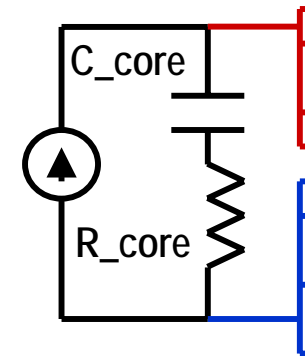
where $R_{pkg} = 1.7 \text{ m}\Omega$ and $L_{pkg} = 162 \text{ pH}$.



On-chip switching behavior is modeled by a current source in parallel with on-chip decoupling capacitors and parasitic resistance.

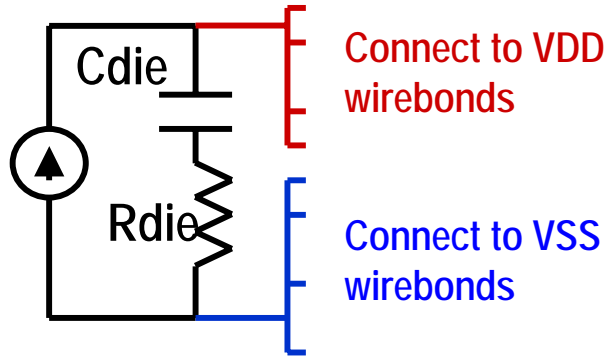
The on-chip decoupling capacitance is 40 nF in series with 0.625 m Ω .

On-chip switching circuit model

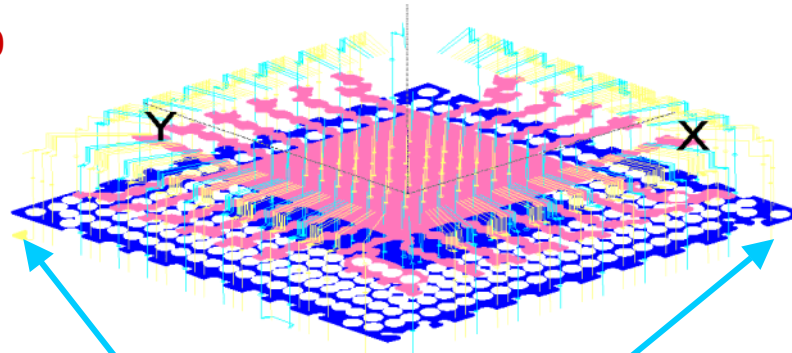


Expensive Full-Wave Modeling Methodology

On-chip switching
circuit model



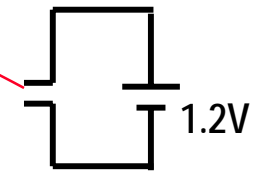
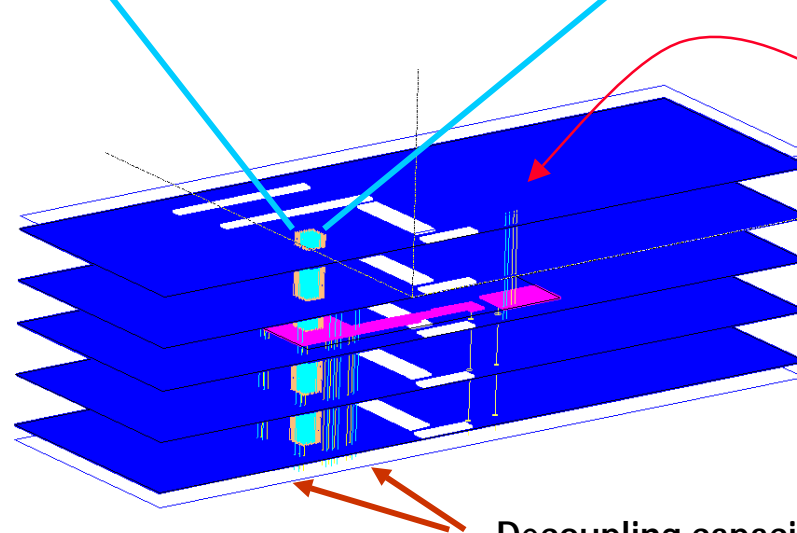
3D full wave model of the package



The mesh size is around the via pitch of the package. A big number of meshes on a multiple layer PCB is very expensive to be modeled together with the package.

3D full wave model of the board

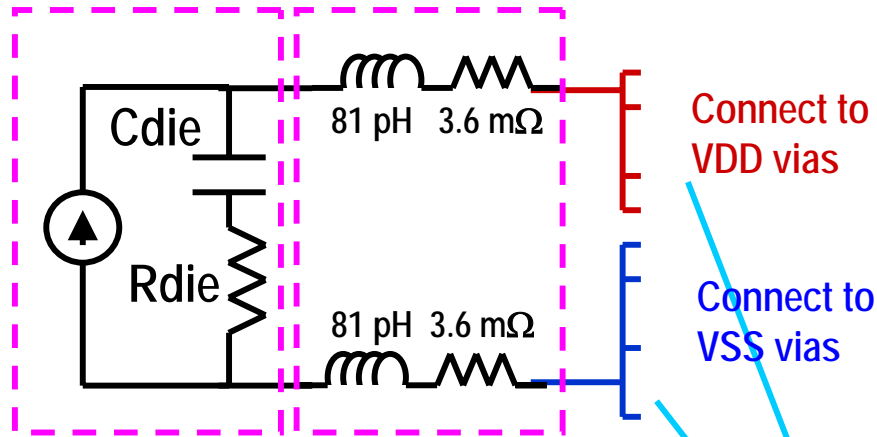
Computation cost is high in terms of memory and CPU time due to uniform meshes in FDTD scheme



An Ideal voltage supply is placed at the location of the voltage regulator Module.

Decoupling capacitors are placed at the bottom side of the board

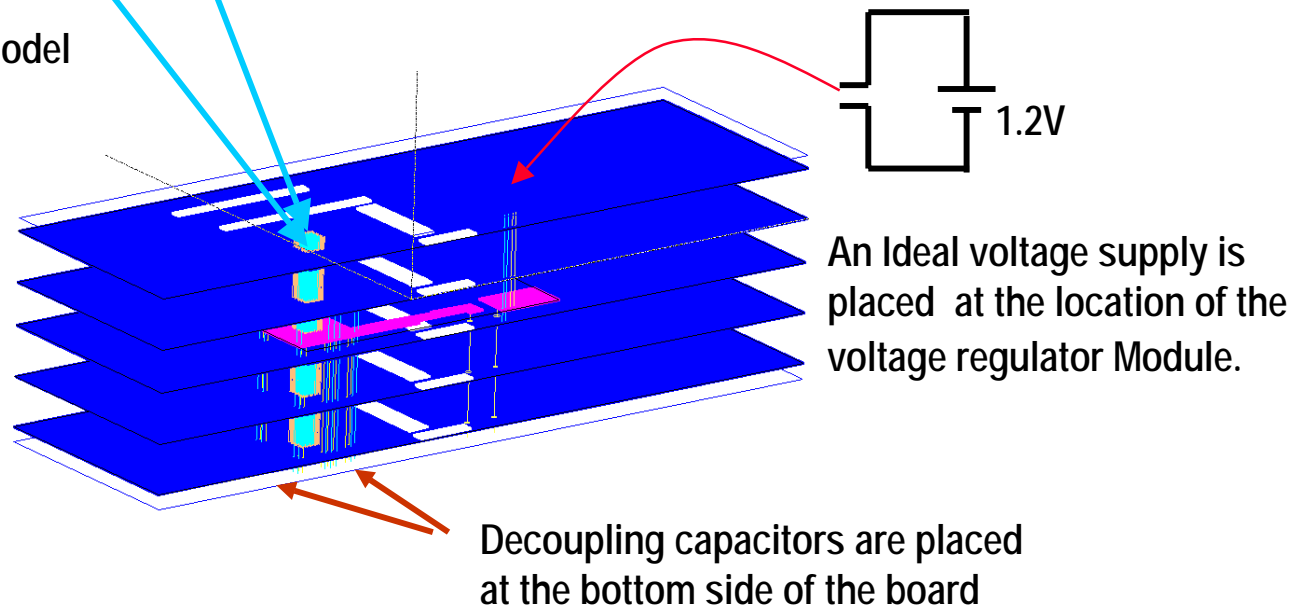
Efficient Simulation Methodology



On-chip switching circuit model Package lump model circuit model

The mesh size is around the via pitch of the board. A big, multiple layer PCB can be efficiently modeled.

3D full wave model of the board



Current Demand on the Core

The system is excited by periodic current demand on the die.

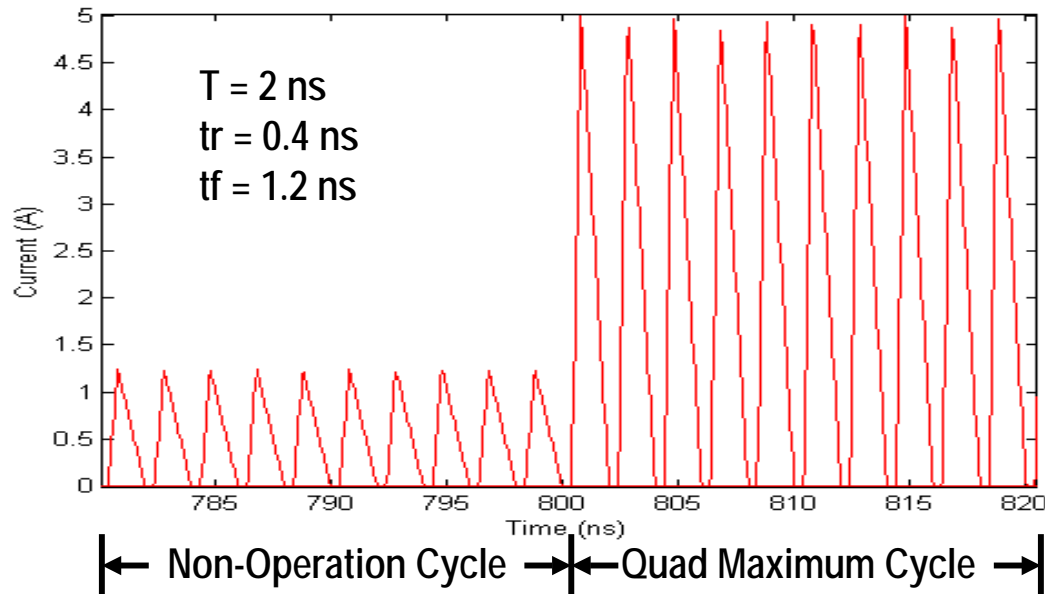
The current source starts continuously switching at time zero with 2 ns cycle.

1. Non-Operation Cycle

No logical operation on chip, but there is clock switching current demand. $I_{AVG} = 0.5 \text{ A}$ ($I_{MAX} = 1.25 \text{ A}$).

2. Maximum-Operation Cycle

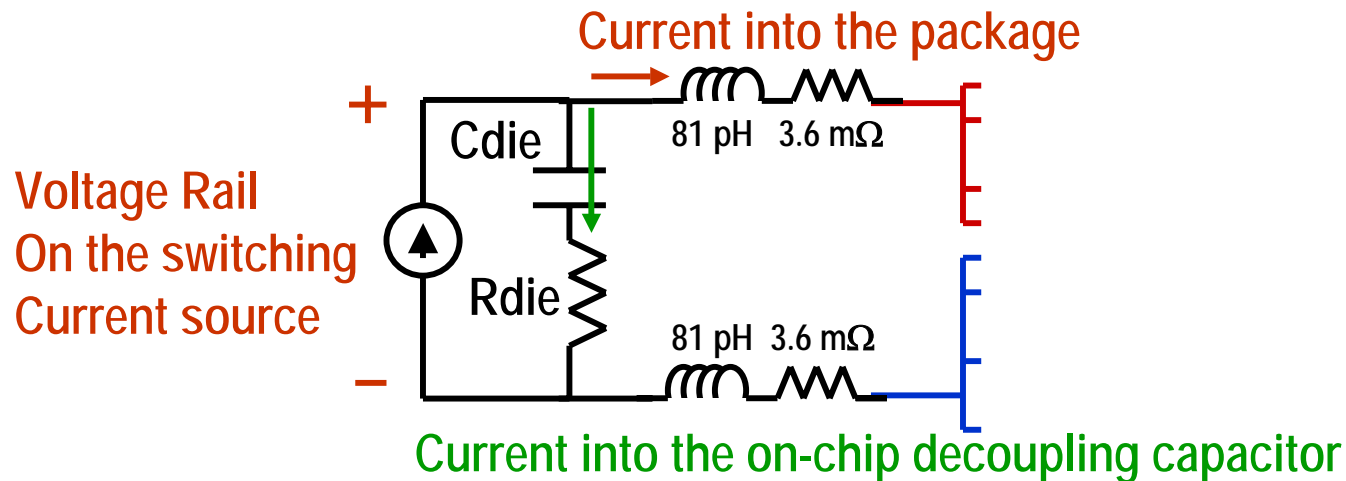
Logic gates switching at $I_{AVG} = 2 \text{ A}$. ($I_{MAX} = 5 \text{ A}$).



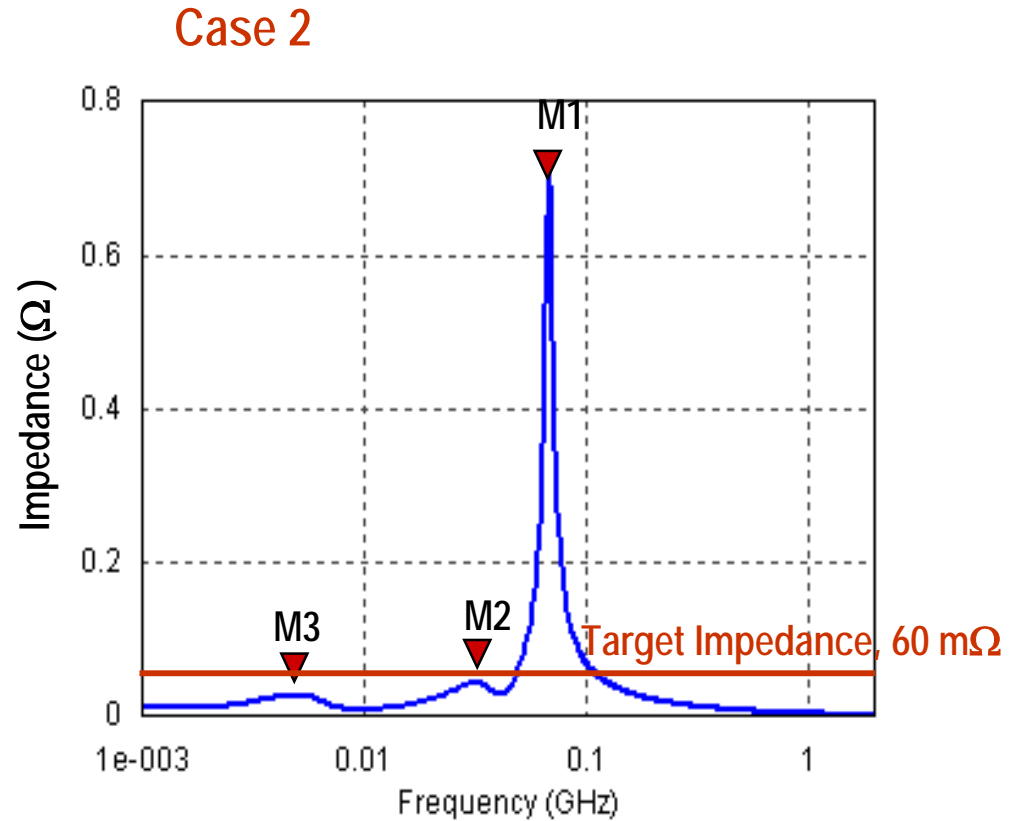
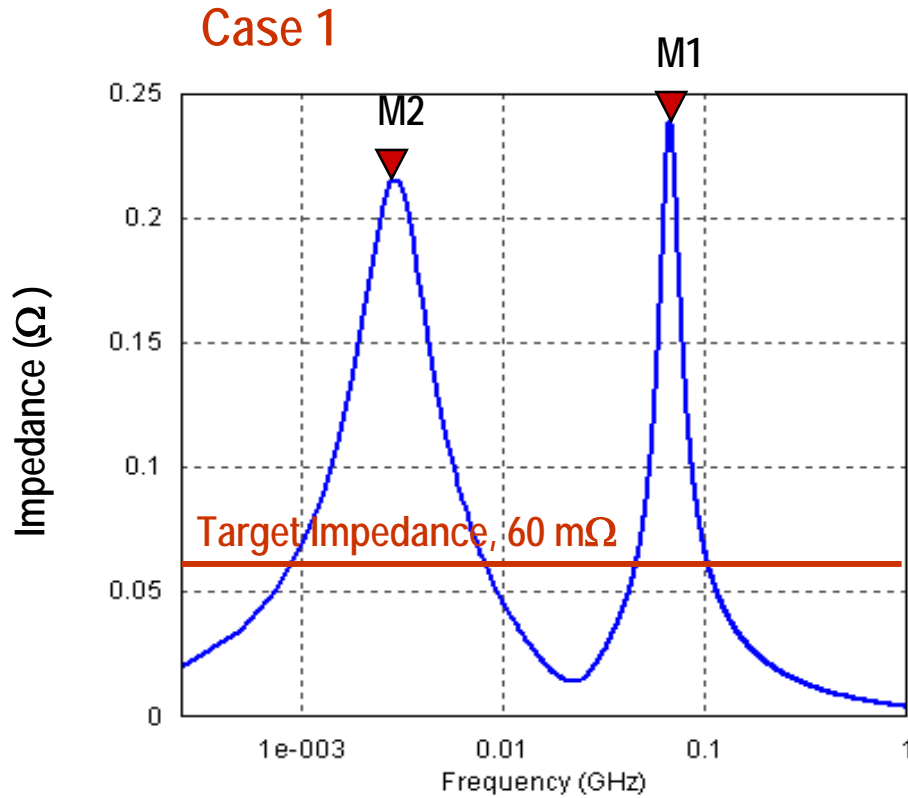
Two Sets of On-board Decoupling Capacitors

- Case 1
- 28 x 0.01uF: ERL= 0.9 nH, ESR = 0.3 Ω , ceramic, Size 0603
 - 4 x 10 uF : ESL = 1.5 nH ESR = 1 Ω , tantalum
- Case 2
- 14 x 0.01uF, ERL= 0.9 nH, ESR = 0.3 Ω , Size 0603
 - 14 x 0.1uF, ERL= 0.9 nH, ESR = 0.08 Ω , Size 0603
 - 4 x 10 uF, ESL = 1.5 nH ESR = 0.03 Ω for ceramic Y5V 1206

The voltage and currents to be observed



PDS Impedance in Two Cases



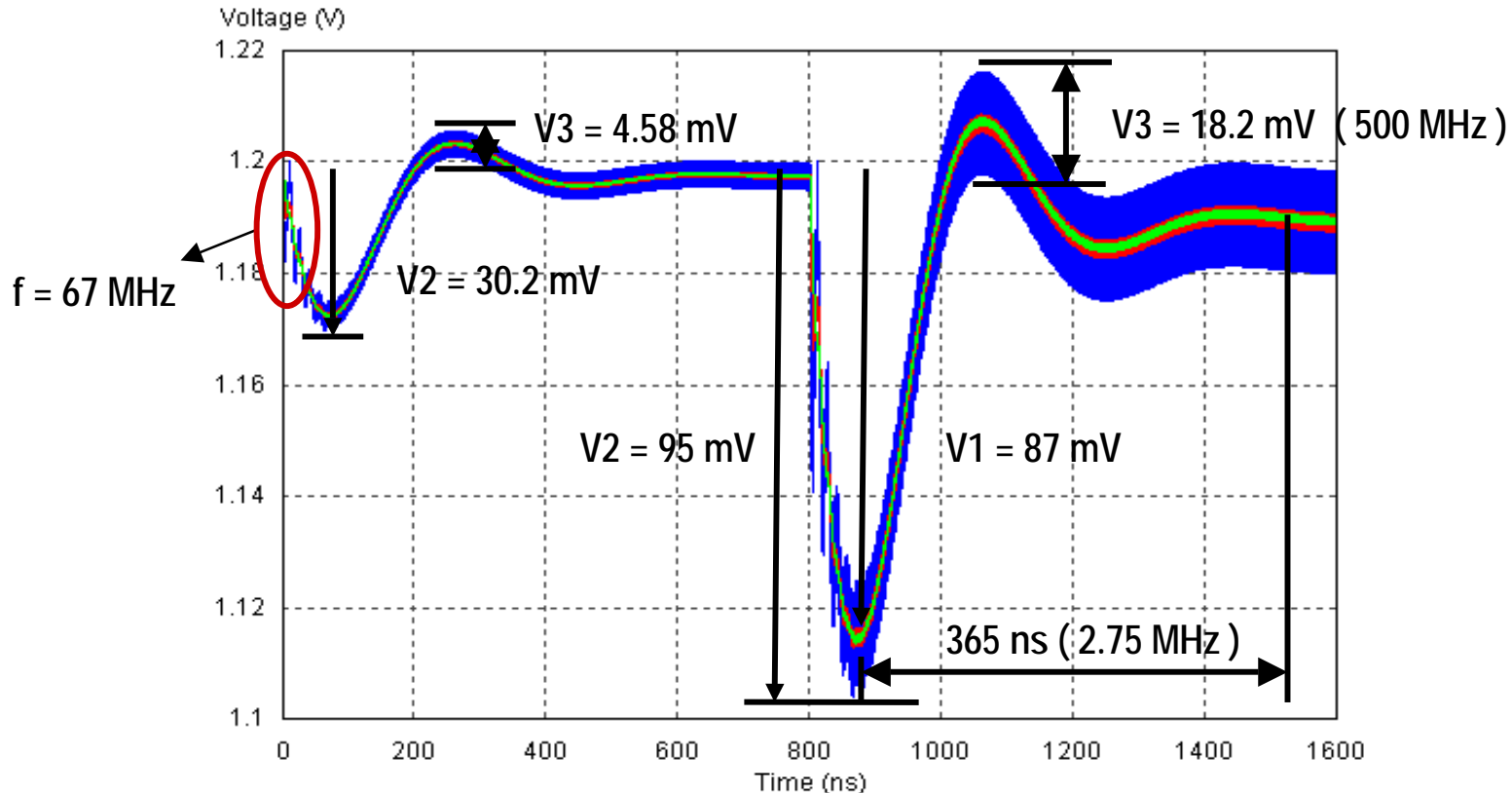
Impedance peaks

- M1: 239 m Ω at 66.75 MHz
- M2: 215 m Ω at 2.75 MHz

- M1: 723 m Ω at 68 MHz
- M2: 45 m Ω at 32 MHz
- M3: 31 m Ω at 5 MHz

Voltage Rail of PDS in Case 1

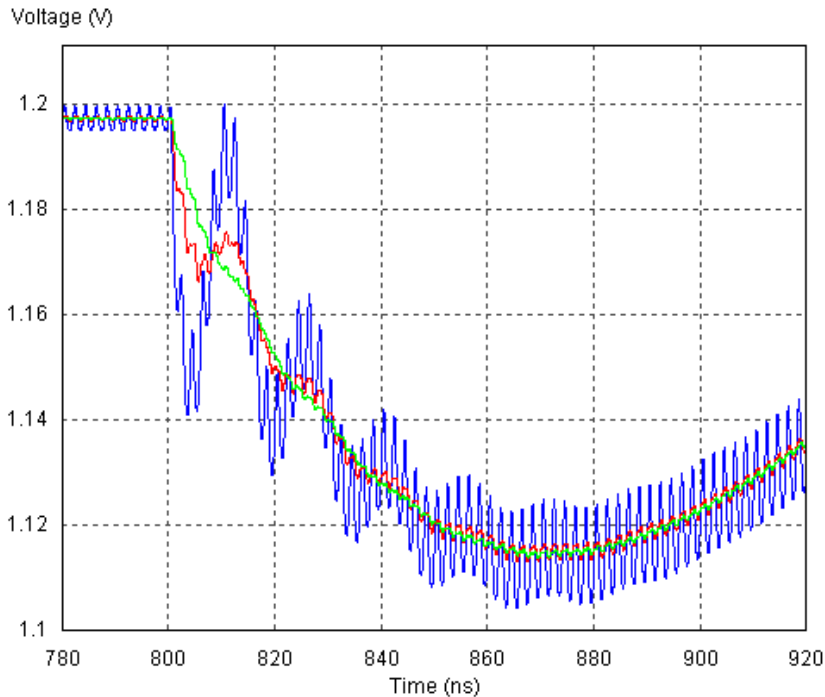
- (a) Voltage at the switching source on the die (Blue)
- (b) Voltage at the top of the EVM board (Red)
- (c) Voltage at the bottom of the EVM board (Green)



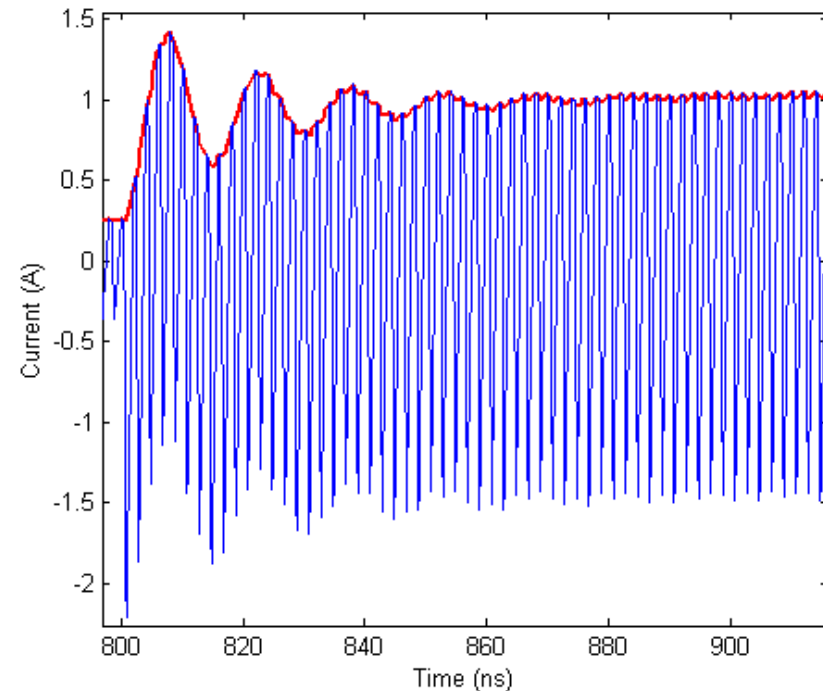
$18.2 / 4.58 = 3.97 \Rightarrow V3$ is linearly proportional to the current magnitude.

Maximum Operation Cycle in Case 1

- (a) Voltage at the switching source on the die (Blue)
- (b) Voltage at the top of the EVM board (Red)
- (c) Voltage at the bottom of the EVM board (Green)



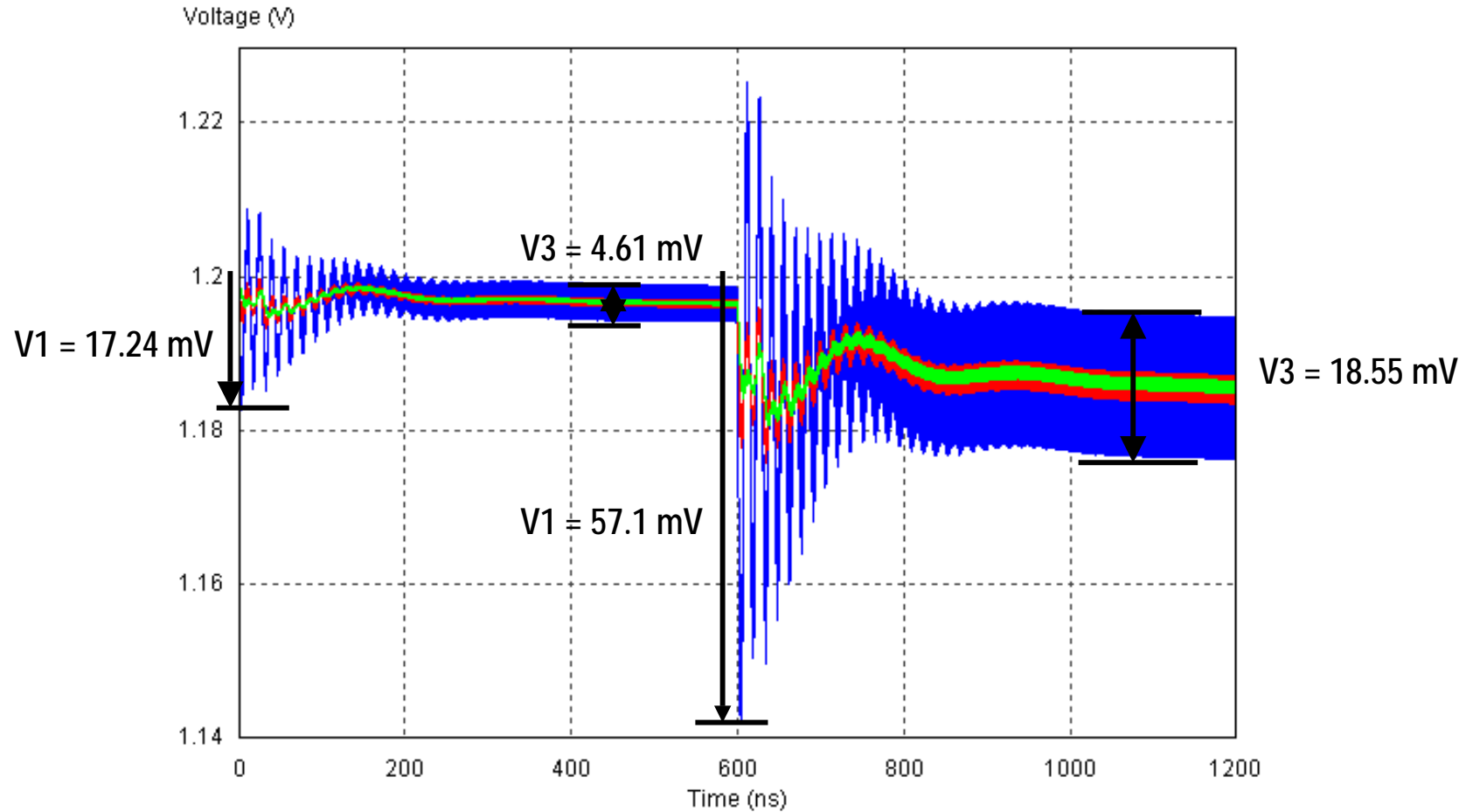
- (a) Current flowing from the source to the package (Red)
- (b) Current flowing from the source to the on-chip decoupling capacitor (Blue)



- The on-chip decoupling capacitor bypasses fast switching currents.
- The current flowing into the package oscillates at 67 MHz for 80 ns.
- The voltage rail on the die oscillates at 67 MHz and 500 MHz.

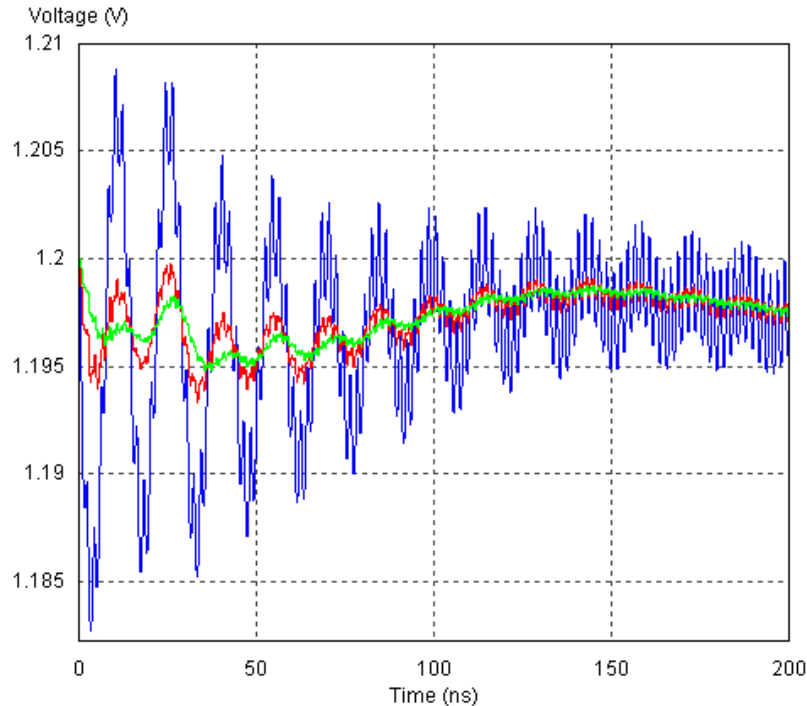
Voltage Rail of PDS in Case 2

- (a) Voltage at the switching source on the die (Blue)
- (b) Voltage at the top of the EVM board (Red)
- (c) Voltage at the bottom of the EVM board (Green)

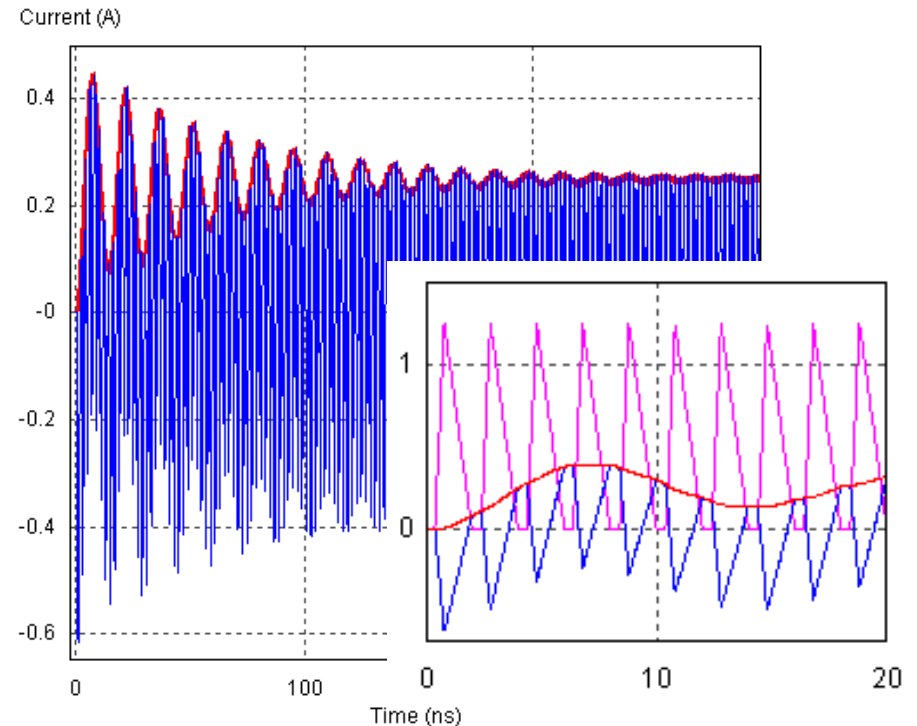


Non-Operation Cycle in Case 2

- (a) Voltage at the switching source on the die (Blue)
- (b) Voltage at the top of the EVM board (Red)
- (c) Voltage at the bottom of the EVM board (Green)



- (a) Current flowing from the source to the package (Red)
- (b) Current flowing from the source to the on-chip decoupling capacitor (Blue)

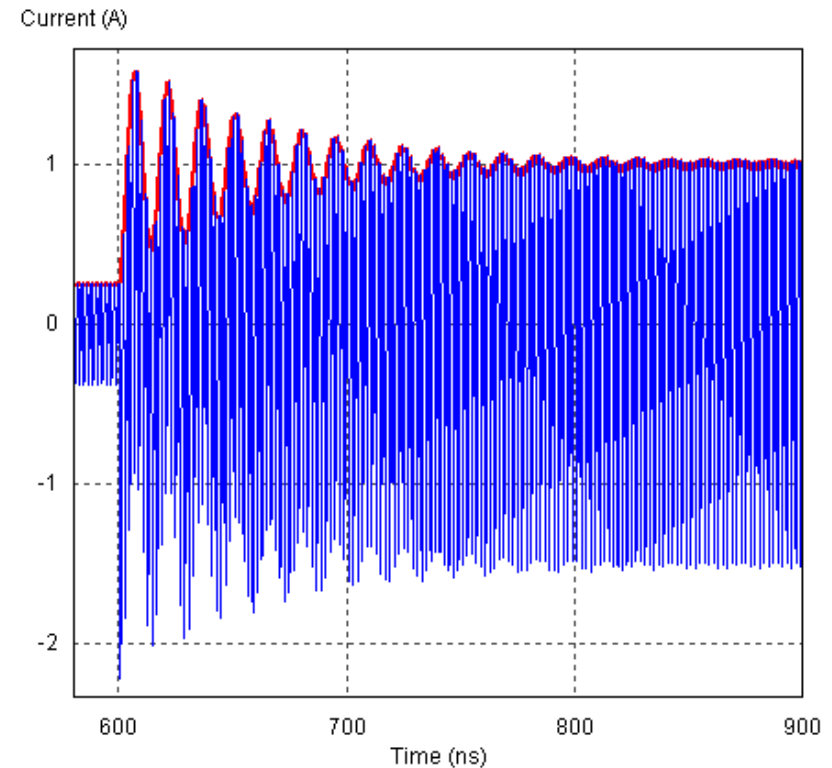
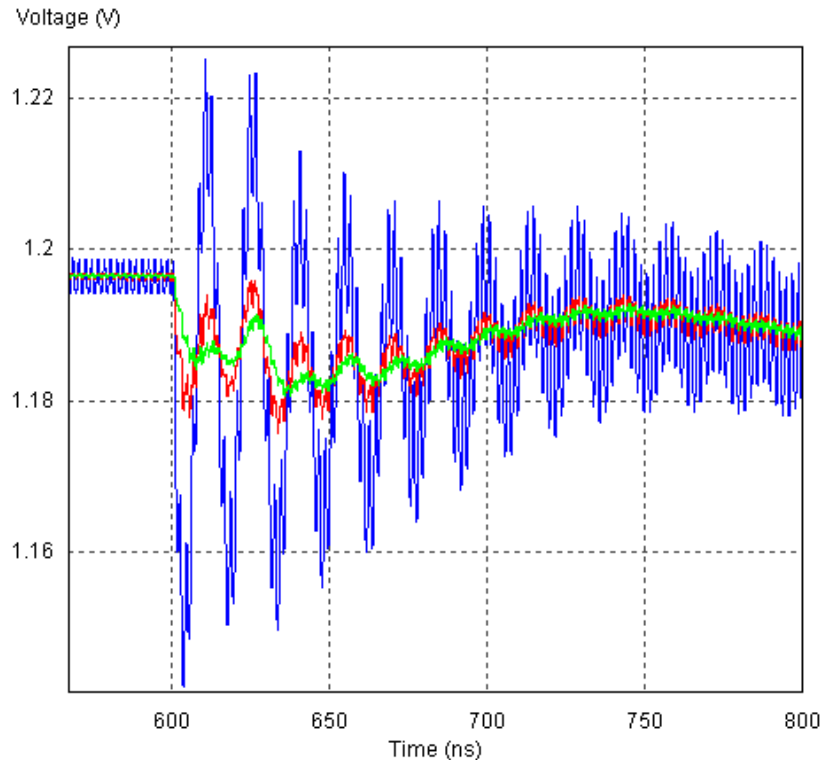


- The on-chip decoupling capacitor bypasses fast switching currents.
- The current flowing into the package oscillates at 67 MHz for 80 ns.
- The voltage rail on the die oscillates at 67 MHz and 500 MHz.

Maximum Operation Cycle in Case 2

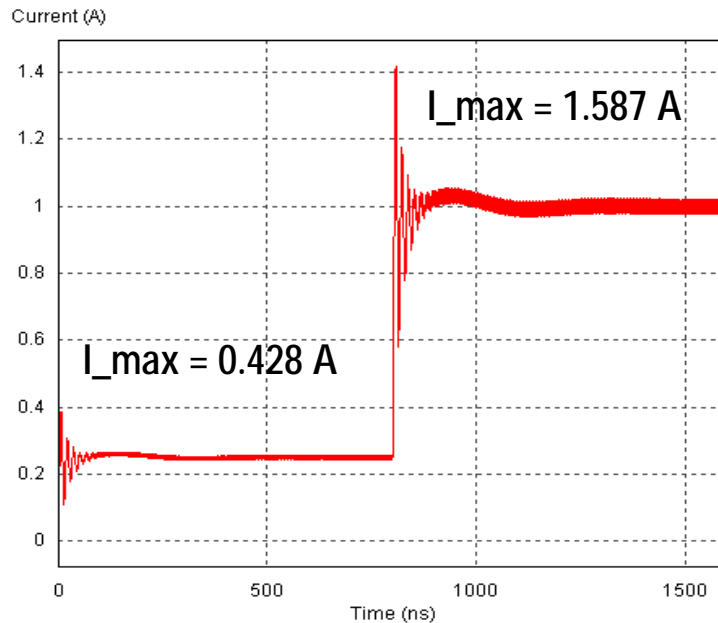
- (a) Voltage at the switching source on the die (Blue)
- (b) Voltage at the top of the EVM board (Red)
- (c) Voltage at the bottom of the EVM board (Green)

- (a) Current flowing from the source to the package (Red)
- (b) Current flowing from the source to the on-chip decoupling capacitor (Blue)

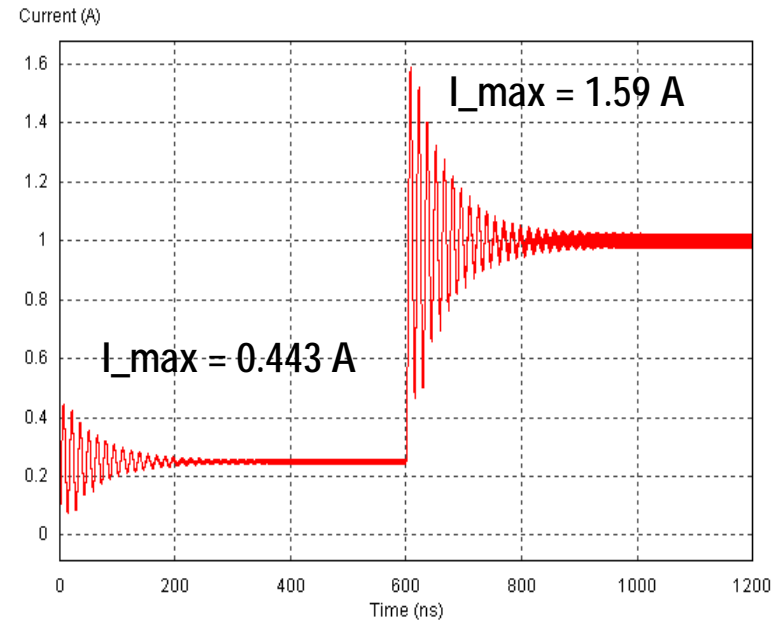


Comparison of the Currents Flowing into the Package

Case 1



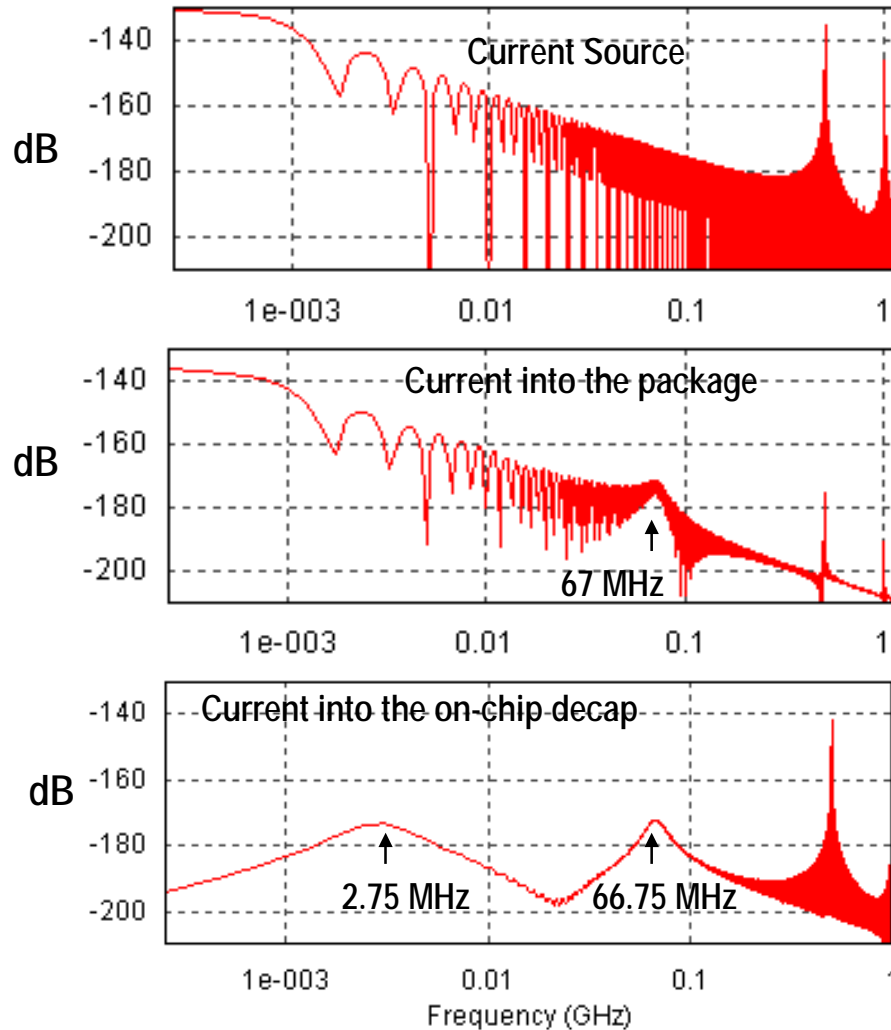
Case 2



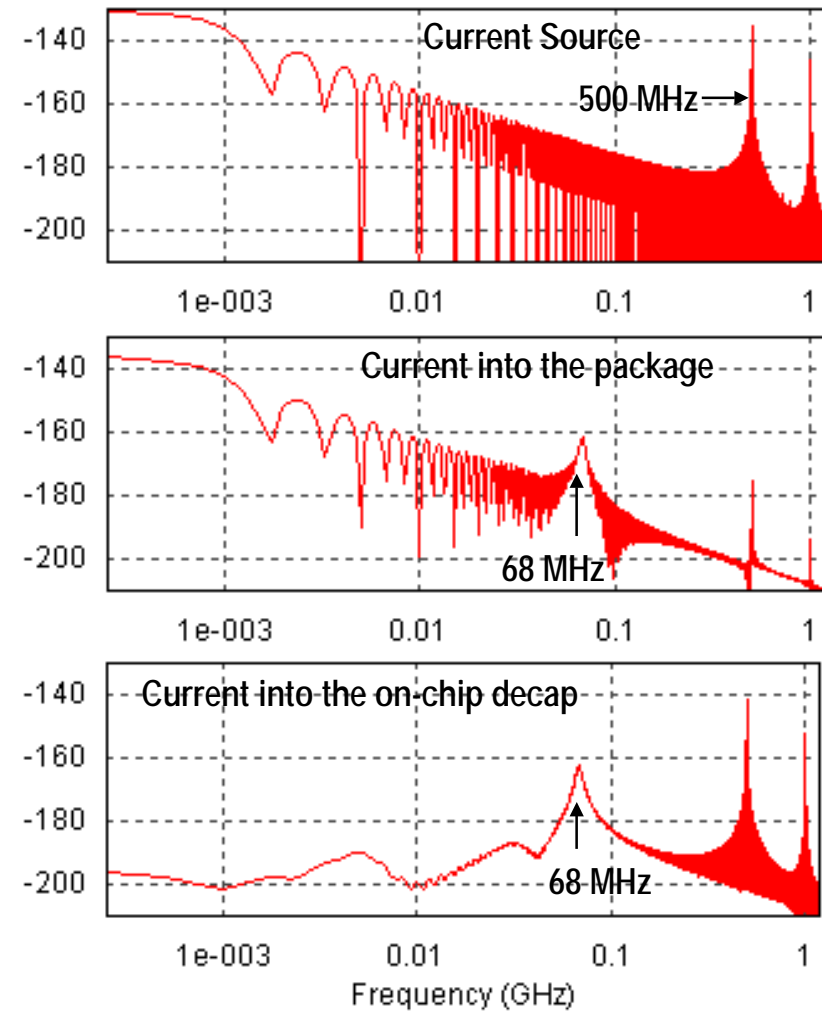
- In case 1, due to the high impedance of the PDS at 3 MHz, less current is absorbed by the package and the board.
- In case 2, the impedance of PDS below 40 MHz is relatively small, most of the current can flow through the package and the board.
- That is, if we reverse the direction of the current, the voltage supply in case 2 can provide more dynamic current to the core and cause less voltage droop.

Frequency Responses of Currents

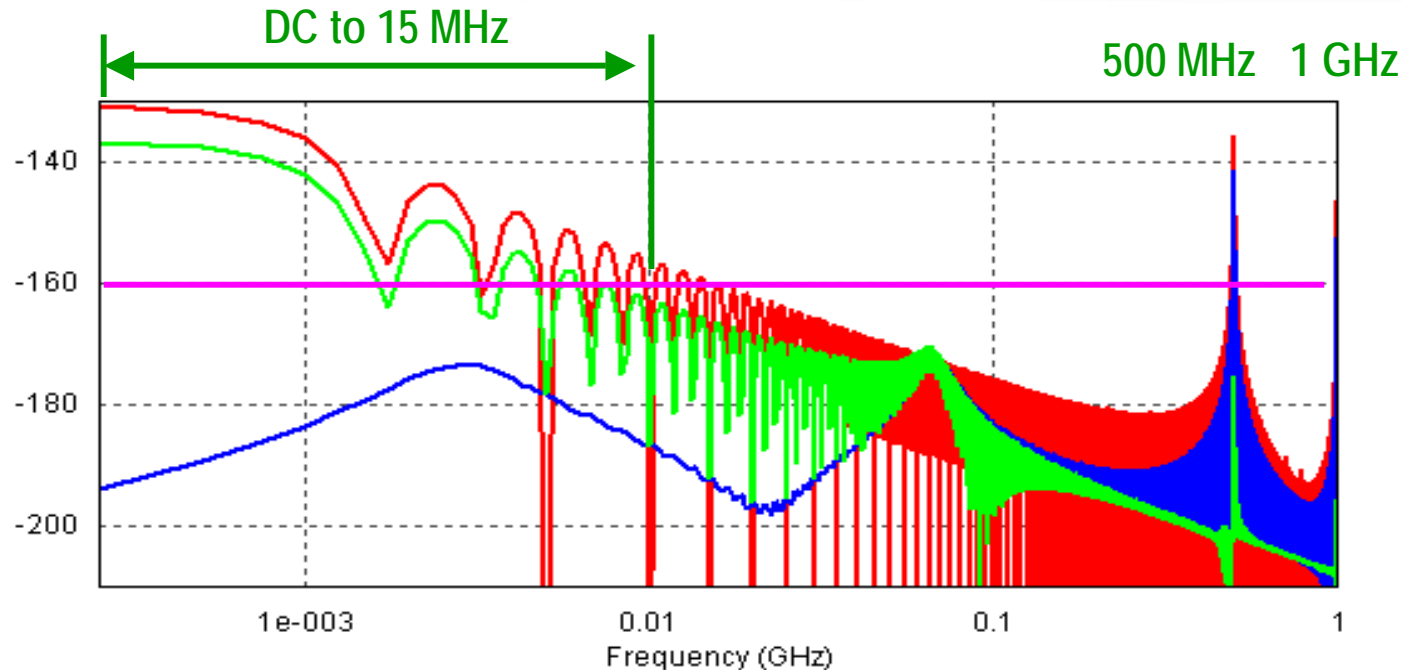
Case 1



Case 2



Power Density Windows



- The major power density windows in frequency domain are from DC to 15 MHz, 500 +/- 10 MHz, and 1000 +/- 5 MHz.
- In this case, 40 nF on-chip decoupling capacitor provides sufficient dynamic current in 500 MHz and its harmonics.
- The power distribution system on the package and the board should have low impedance from DC to 15 MHz.
- Since the power spectrum density from 15 MHz to 490 MHz is relatively low, the impedance requirement in this region is relatively lower.

- Power distribution analysis in frequency domain is insightful to help identify the oscillation frequencies of the system and determine suitable decoupling capacitors.
- The current waveform of the on-chip switching can be approximated as a periodic triangular function and its frequency response is a sinc square function at DC and harmonics of the current switching frequency.
- On-chip capacitors in tens of nF range should be able to provide low impedance above several hundreds MHz range.
- The PDS in a package and a board should be designed as a low pass filter with a bandwidth over the frequency spectrum of a single current pulse, which is from DC to 15 MHz in this case.
- Faster switching circuits usually result in a narrower current pulse. The narrower the single current pulse is, the wider the bandwidth has to be.
- It is very difficult to quantify the noise and determine the target impedance through calculation of Ohm's law because of the complexity of the system.
- However, since the power spectrum density reduces in frequency below the circuit switching frequency, the target impedance of PDS should also increase in frequency.
- The high impedance at tens of MHz, which is beyond the power spectrum window, has less impact on noise than the one at a few MHz.