

# Package and Chip Design Optimization for Mid-Frequency Power Distribution Decoupling

**Bernd Garben**

IBM Laboratory, 7032 Boeblingen, Germany,  
e-mail: garbenb@de.ibm.com, phone: 49-7031-16-2590, fax: 49-7031-16-2042

And

**George A. Katopis, and Wiren D. Becker**

IBM Laboratory, Poughkeepsie, NY  
e-mail: katopis@us.ibm.com, and wbecker@us.ibm.com

## Abstract

In this paper the mid-frequency power supply noise has been studied for a complex, next generation computer system by simulations of the complete module and board power distribution system. An MCM-D and MCM-C design and the effectiveness of on-chip and discrete on-module decoupling capacitors have been compared. The impact of delta-I ramping over several cycles and the impact of the continuous background switching and on-chip leakage have been analyzed. Conclusions are presented to optimize the chip and package design.

## Introduction

It is of increasing importance to contain the mid-frequency power noise caused by on-chip switching activity variations, because of tighter supply voltage tolerances due to decreasing operating voltage and shorter cycle times, and because of faster and larger current transients due to increasing switching frequency, chip current, and extensive clock gating [1], [2]. Therefore low impedance power delivery and optimized decoupling is mandatory. Power noise simulations are essential in the early development phase of chip and package design. For mid-frequency decoupling optimization the power distribution of the entire package with capacitors and all parasitic inductances must be simulated [3], [4], [5]. In this paper SPEED2000 from Sigrity Inc. has been used for the simulations [6]. The methodology has been described in detail in Ref. [4] where an IBM product with MCM-D was analyzed. This paper studies the differences between experimental MCM-C (full glass ceramic) and MCM-D (one plane pair thin film at MCM top side) designs.

## Module description and chip simulation parameters

A design of a multi-chip module (MCM) with size of 93mm by 93mm is assumed to contain eight processor (PU) chips, one clock chip, four L2 memory and two L3 memory interface chips and discrete decoupling capacitors for mid-frequency power noise decoupling. These capacitors can be ceramic low inductance capacitors with 8pH ESL, 30mohm ESR and 265nF capacitance depending on temperature. Five cases of different MCM technology and number of MCM decaps adjacent to the most critical PU chip in the MCM corner (table 1) have been analyzed and will be discussed in the next sections. The MCM is assumed to have the power connections encountered in previous IBM MCMs, namely 1100 power and 1100 ground connections to the processor board via a SMT connector. The processor board with the mid- and low-frequency decoupling capacitors is also included in the simulation model.

The operating frequency range for the next generation microprocessors is assumed to be 1GHz to 10GHz. Therefore, simulations have been performed at both these two frequencies. Frequency dependencies have been studied in more detail for an existing MCM and processor board in Ref. [5]. The on-chip switching is represented in these simulations as commonly done by current sources and no supply voltage is connected to the package. Thereby the mid-frequency noise is slightly overpredicted, but the simulations are faster, as shown in Ref. [7]. A delta-I step of 10A has been assumed for each PU chip and minor delta-I steps for the rest of the chips so that the total MCM delta-I equals 100A. It has been shown that the mid-frequency noise on the PU chips is proportional to the PU delta-I value. The noise propagation from the other chips to the PU chipsites is negligible due to the module capacitors between the chipsites. The delta-I transient has been assumed at first to occur within one switching cycle, but has also been extended over a variable number of cycles. The study has been started with zero background switching and neglecting leakage currents expected in the future generation of microprocessors. Moreover, resistors have been distributed parallel to the current sources as simplified models for background switching and on-chip leakage.

## On-chip decoupling capacitance variation

Fig.1 shows the voltage fluctuations at a current source in the center of the corner PU chip in case 1 after the sources

start switching at time zero. The corner PU chip has MCM decaps at only two edges in case 1 to size the worst case noise. Variations of the on-chip decoupling capacitance in the range from 400nF to 1600nF have a large impact on the mid-frequency noise amplitude. This capacitance is represented in the simulations by RC elements (40ps time constant) which are homogeneously distributed over the chip area parallel to the current sources. The importance of adequate on-chip decoupling capacitance has been emphasized in several papers before, e.g. [8], [9].

It has been shown that for the same delta-I the mid-frequency voltage oscillations are identical for 10GHz and 1GHz. This is expected, because both frequencies are much larger than than the package resonant frequency (41MHz for 400nF capacitance). In general, however, the average switching current and delta-I will increase with frequency.

The slope  $\Delta t/\Delta U$  has been taken at  $t=1ns$  for each mid-frequency oscillation from the simulations. The following simple charging equation is fulfilled over the analyzed range of the PU chip decoupling capacitance  $C_{pu}$ :

$$\frac{\Delta t}{\Delta U} = \frac{C_{pu}}{\Delta I_{pu}}, \text{ with } \Delta I_{pu} = 10A. \quad (1)$$

Moreover, the square of the oscillation period T from the curves in fig.1 is found to be approximately linear dependent on the series capacitance C of the PU chip capacitance and the capacitance of the adjacent MCM decaps according to

$$T^2 = 4 \cdot \pi^2 \cdot C \cdot L_{eff} \quad (2), \quad \text{and} \quad \frac{1}{C} = \frac{1}{C_{pu}} + \frac{1}{n \cdot C_{mcm}}, \quad (3)$$

with  $n$  = number of MCM capacitors adjacent to the PU chip,  $C_{mcm}$  = MCM decap capacitance.

It is concluded that the major oscillation is caused by the ‘horizontal’ resonant loop formed by the on-chip decoupling capacitors, the adjacent discrete on-MCM decoupling capacitors, and the effective loop inductance  $L_{eff}$  between these two sets of capacitors. The simulations yield  $L_{eff} = 44pH$  for the corner PU chip in case 1. Moreover,  $L_{eff}$  has been estimated for the horizontal resonant loop as follows:

$$L_{eff} = (L1 + L2 + L3 + L4) / n \quad (4), \text{ with}$$

- $L1$  = MCM decap ESL. 8pH has been assumed for low inductance MCM decaps in the simulations shown in fig.1,
- $L2$  = MCM decap mounting and via loop inductance from the decap to the top power/ground planes of the MCM. 137pH has been calculated in case 1) with an IBM L3D extraction programm and used for the simulations in fig.1. This loop inductance is presently not included in the SPEED simulations and is therefore added to the decap ESL
- $L3$  = loop inductance from the on-chip decaps to the MCM top planes is assumed to be negligible,
- $L4$  = path inductance of the MCM top plane pair . An approximation by the inductance of two parallel solid planes with 200um distance and equal path length and width yields 250pH. 200um plane distance has also been assumed for the MCM-C in the simulations to take the increased inductance due to the actual meshes into account.

Equation (4) yields 38pH for  $n=9$  (case 1) which is in good agreement with the 44pH obtained from the simulations.

### Variation of on-module capacitors capacitance, inductance and placement

The mid-frequency noise amplitude is almost independent of the MCM capacitor capacitance for  $C_{mcm} > 50nF$  up to a very large capacitance of 530nF as shown in Fig.2. This is expected from the results in the previous section, and is in contrast to the results reported in Ref. [4] for an actual product MCM-D which has a low inductive thin film top power/ground plane pair and a pin-in hole connector to the board. There, the ‘horizontal’ resonant loop has only an  $L_{eff}$  of 5pH, due to the low plane path inductance, which caused only a minor mid-frequency noise peak, whereas the major noise peak was caused by the ‘vertical’ resonant loop (down to the nearest board capacitors) with  $L_{eff} = 12pH$ . The simulations for the MCM-C considered in this study yield a relatively small  $L_{eff}=6.5pH$  for the ‘vertical’ loop. Therefore, the vertical loop has a negligible impact on the mid-frequency noise for this experimental MCM-C in case of  $C_{mcm} > 50nF$ .

Simulations with variations of the lumped inductance  $L1+L2$  yield the following mid-frequency noise variations:

- 5% increase, if  $L1+L2$  is increased from 145pH to 600pH, e.g. if ‘low-cost, high inductive’ decaps are used., and
- 4% reduction, if  $L1+L2$  is reduced from 145pH to 10pH, e.g. by shortening the via length corresponding to case 4.

The number of MCM decaps adjacent to the corner PU chip has been increased from 9 (case 1) to 14 (case 2) and 21 (case 3). Thereby the mf noise amplitude in the center of the corner PU chip is significantly reduced (table 1, fig. 3) and the noise peak of 128mV in the corner of this chip in case 1 is removed.

### Variation of MCM technology

Decreasing the MCM top plane path inductance, e.g. by usage of a thin dielectric is a very effective for reduction of  $L_{eff}$  and the mid-frequency noise, as shown by the cases 4 and 5 in Fig.3 and table 1 for the MCM-D design.

It is a good practice and of increasing importance to place capacitances with low inductance close to the chips at the four chip edges and to have low inductive vias and power plane connections [3], [10], [11], [12], [13]. Otherwise the on-chip decoupling capacitance must be increased as shown in Fig.3, but this is limited by the chip size.

### **Variation of background switching and leakage**

So far it has been assumed that the on-chip switching activity variation causes a delta-I step from zero to 10A on the PU chips. In reality most circuits do not simultaneously change their switching activity and such time differences damp the mid-frequency oscillation. Moreover, damping is also provided by constant leakage currents which are caused for example by thin oxide leakage.

As a first approximation the leakage and the background current have been assumed to be voltage independent and included in the simulations by placing resistors parallel to each of the 80 the current sources of the eight PU chips. The resistance has been varied from  $4.8\Omega$ , to  $2.4\Omega$  and  $1.6\Omega$ . Assuming an operating voltage of 1.2V this causes a total background and leakage current for the eight PU chips of 160A, 320A and 480A (2x, 4x and 6x of the assumed delta-I current). The resulting mid-frequency noise amplitude has been normalized by the noise value for zero leakage current (no parallel resistor) and plotted in Fig.4. There is a significant noise reduction e.g. by 29% in case of 480A.

Fig.4 shows also the influence of background and leakage current for the product MCM-D. Resistors with the same resistance values have been placed parallel to the 504 current sources which represent the chips on this module. Assuming the same operating voltage this corresponds to a total MCM background and leakage current of 126A, 252A and 378A respectively. The influence of the parallel resistors on the mid-frequency noise is much smaller for this module, because the total impedance equals at least  $3m\Omega$  ( $=1.6\Omega/504$ ) for the parallel resistors, but only  $0.4m\Omega$  for the module decaps at the resonant frequency (Ref. [7]). Therefore, there a smaller portion of the oscillation current flows through the resistors parallel to the current sources, and the damping is primarily determined by the ohmic resistance of the module pins and MCM decaps as discussed in Ref. [7].

### **Variation of delta-I ramp-up time**

Finally the noise reduction for the MCM in case 1) has been analyzed, if the delta-step takes several cycles instead of a single cycle. A significant noise reduction in the range from 5% to 52% is obtained, if the delta-I ramp-up (ramp-down) time is in the time range between the 1st voltage droop (6ns) and the 1st voltage overshoot (18ns). A small mid-frequency oscillation period (low  $L_{eff}$ ) compared with the switching cycle time is advantageous. However, the ramp-up time and therefore this noise reduction effect will decrease with increasing switching frequency.

### **Conclusions**

Large on-chip decoupling capacitance is of major importance to guarantee the mid-frequency noise tolerances of future computer systems. Moreover, a small loop inductance to the next level of decoupling devices is essential, especially if not sufficient decoupling capacitance can be placed on the chips. Damping of the noise oscillations by the continuously switching circuits and by on-chip leakage reduces the noise only, if a significant portion of the oscillation current flows through the switching or leaking circuits. The mid-frequency noise is significantly reduced, if the delta-I ramp-up (ramp-down) time is in the range from 25% to 50% of the noise oscillation period. The mid-frequency noise caused by on-chip switching will increase with increasing switching frequency due to smaller delta-I ramp-up (ramp-down) times and increasing total chip and delta-I currents.

### **Acknowledgment**

The authors would like to thank Bhupindra Singh from IBM Poughkeepsie, who provided the via loop inductance to MCM top planes, and Anand Haridass from IBM Austin for helpful discussions.

### **References**

- [1] S.H.Gunther, "Managing Microprocessor Power Consumption", IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 7-8, 2001
- [2] M.T.Zhang, "Powering Intel Pentium 4 Processors", IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 215-218, 2001
- [3] Li, Y.L., et al, "Enhancing Power Distribution System through 3D Integrated Models, Optimized Designs, and Switching VRM model", Proc. IEEE Electronic Components and Technol. Conf. (ECTC), pp. 272-277, 2000
- [4] B.Garben, M.F.McAllister, W.D.Becker, R.Frech, "Mid-Frequency Delta-I Noise Analysis of Complex Computer System Boards with Multiprocessor Modules and Verification by Measurements", IEEE Transactions on Advanced Packaging, Vol. 24, No. 3, pp. 294-303, Aug. 2001
- [5] B.Garben, R.Frech, J.Supper, "Simulations of Frequency Dependencies of Delta-I Noise", IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 199-202, 2001
- [6] www.sigritty.com
- [7] B.Garben, R.Frech, J.Supper, M.F.McAllister, to be published in IEEE Transactions on Advanced Packaging, 2002

[8] W.D. Becker, et al, "Modeling, Simulation and Measurement of Mid-Frequency Simultaneous Switching Noise in Computer Systems", *IEEE Trans. Compon., Packaging, and Manuf. Technol., Part B: Advanced Packaging*, vol. 21, no. 2, pp. 157-163, May 1998.

[9] D.Herrell, B.Beker, "Modeling of Power Distribution Systems for High-Performance Microprocessors", *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 3, pp. 240-248, Aug. 1999

[10] A.Sarangi, G.Ji, T.Arabi, G.F.Taylor, "Design and Performance Evaluation of Pentium III Microprocessor Packaging", *IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 291-294, 2001

[11] M.Tsuk, R.Dame, D.Dvorscak, C.Houghton, J.St.Laurent, "Modeling and Measurement of the Alpha 21364 Package", *IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 283-286, 2001

[12] S.Towle, et al, "Bumpless Build-Up Layer Packaging", *Proceedings of ASME Int. Mech. Eng. Congress and Exposition*, Nov. 2001

[13] B.Garben, A.Huber, D.Kaller, E.Klink, S.Grivet-Talocia, "Organic Chip Packaging Technology for High Speed Processor Applications", *6th IEEE Workshop on Signal Propagation on Interconnects*, May 2002

Table 1: MCM technology, MCM decaps at corner PU chip, mid-frequency noise amplitude

case	technology	decaps at corner PU chip	number of decaps at PU	mf noise amplitude
1	MCM-C	at 2 chip edges	9	107mV
2	MCM-C	at 3 chip edges	14	98mV
3	MCM-C	at 4 chip edges	21	90mV
4	MCM-D	at 2 chip edges	9	81mV
5	MCM-D	at 4 chip edges	21	62mV

