

A Design Methodology for The I/O Power Supply of Next Generation Packaging

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ABSTRACT

The method of three-dimensional I/O power modeling will be reviewed in detail based on the learning from the previous one-dimensional and two-dimensional models. This paper will cover the latest development of next generation microprocessor I/O power models and the adoption of a new three-dimensional modeling methodology to meet the challenging design requirements of a high performance signal bus with short turn-around times. The paper also presents a new technique of using damping resistors to attenuate the high frequency noise on the IO supply.

1. INTRODUCTION

Beginning with the Pentium® III processor, a method for power delivery modeling at the package and system levels has been developed by combining a three-dimensional field solver and SPICE simulation. These processors are designed with two independent power supplies, one for the core of the chip and the other for the I/O. However, because the core and I/O are very different in terms of current profiles, their noise signatures have significant differences as well. As a result different methods for modeling the power delivery have evolved in these areas. According to measurements and modeling in previous studies, multiple I/O buffers switching induces significant high frequency noise on the I/O power network [1] In this paper we will present a technique for suppressing the high frequency noise and prove the effectiveness of the proposed solution with three dimensional modeling and simulation.

2. THE MODELING AND SIMULATION METHODOLOGY

The other improvement was the incorporation of a distributed I/O pad ring and package plane model. Based on this result, the package capacitors were placed close to these noisy spots. [2]

The Pentium® III microprocessor Front Side Bus (FSB) was designed to operate at speeds of up to 200Mhz. This higher bus frequency led to both a higher current slew rate and a tighter timing budget for bus signals. In order to tolerate the transient noise resulting from the high current slew rate, the loop inductance at high frequency must be reduced to a minimum level. The method and assumption of this model were almost the same as the previous one-dimensional model except for two improvements

First was the adoption of an integrated capacitor-via-planes model which provides much more accurate loop inductance by taking into account the mutual effect between different levels of interconnect components, i.e. capacitor to micro-via, micro-via to planes, and capacitor to planes.

The other improvement was the incorporation of a distributed I/O pad ring and package plane model. Based on this result, the package capacitors were placed close to these noisy spots[2] .

Recently, die area and leakage power have started to limit the availability of on-die decoupling. When the core and IOs are shorted, this results in a requirement that the package decoupling respond faster and provide more charge. Furthermore, because of the high power consumed by the processor core, the core voltage may drop while the I/O is operating at full speed. In order to minimize the impact of core transients on the I/O, the power distribution networks for the two sets of circuits are separated in this design. The main advantage of having separated core and I/O power is that the processor can have more power management modes with fully functional FSB.

In this situation, the one and two-dimensional methods of the previous projects were not capable of providing adequate simulation results because they did not have enough time and space resolution. In this design, we have investigated two methods of building a three-dimensional distributed model for the power delivery.

The first one has been directly developed from the one-dimensional lumped model. It divides the package and motherboard into small tiles and extracts the parasitic for these tiles with a field solver in x, y, and z directions. These parasitics are then used in SPICE like simulators. The main advantage of this method is that it could be integrated with virtually any transistor level circuit simulator. The transistor level simulator is advantageous in capturing the effects of non linear terminations and, especially, modeling the low frequency response of the voltage regulator.

The second method, adopted here, is to use a time domain field solver. These solvers are generally limited in their ability to model a wide variety of circuits but are very good in capturing wave effects and modeling three dimensional structures. In this particular design, we have used SPEED2000, a commercially available tool. A particular advantage of SPEED2000 is the adaptive meshing. The mesh size could be modified easily and increased to more than 100 by 100 for the high frequency response.

In this design, The on die padding circuits and metal layers have been modeled with a two-dimensional distributed model. The circuits have then been combined with a three-dimensional package-motherboard model in SPEED2000 as showed in figure 1. The small square on the top represents the package layers and the shape at the center is the I/O power plane inside the package. Through via and pins on the base layer of the package, the I/O power plane is connected to the trace, decoupling capacitors, and voltage regulator on the motherboard. On the top layer of the package, there are vias representing bumps and are connected to the two-dimensional die pad ring model.

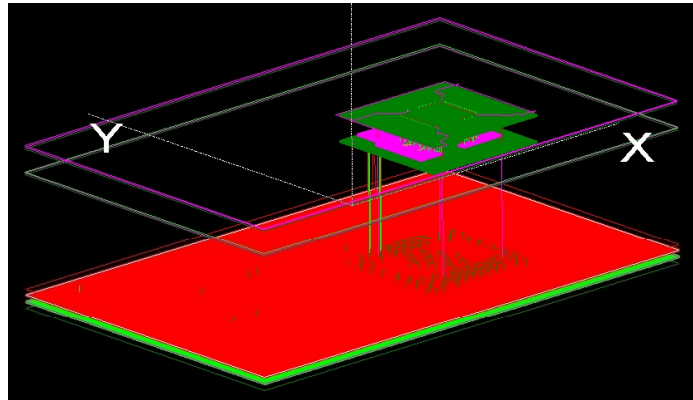


Figure 1: I/O power model from motherboard to package delivery

The pad ring model consists of 5 functional unit blocks (FUBs) on the data side and 4 FUBs on the address side. The buffer cell model including a voltage-controlled resistor as a driver, V_{cc}/V_{ss} metal 4/5/6 rails, decoupling capacitors, and a leakage resistor. The on-die metal rail model includes the frequency-dependant capacitive and inductive coupling[3] Finally Figure 2 shows the proposed technique of separating the high frequency (V_{tt_HF}) and low frequency (V_{tt_LF}) current paths with a resistor placed on the high frequency path between the driver and a package decoupling capacitor to damp the high frequency voltage droops induced by the toggling buffers. This resistor achieves the same objectives proposed by Waizman, et. al. [4] without having to control the effective series resistance of the decoupling capacitors. The implementation of this technique is however, non trivial and many questions related to the physical design and electrical performance needed to be answered. For example the correct value of the resistance had to be determined using[4]. The number of high frequency and low frequency power bumps, the number and quality of package capacitors, and the number of package pins had to be determined subject to the applicable performance and reliability constraints.

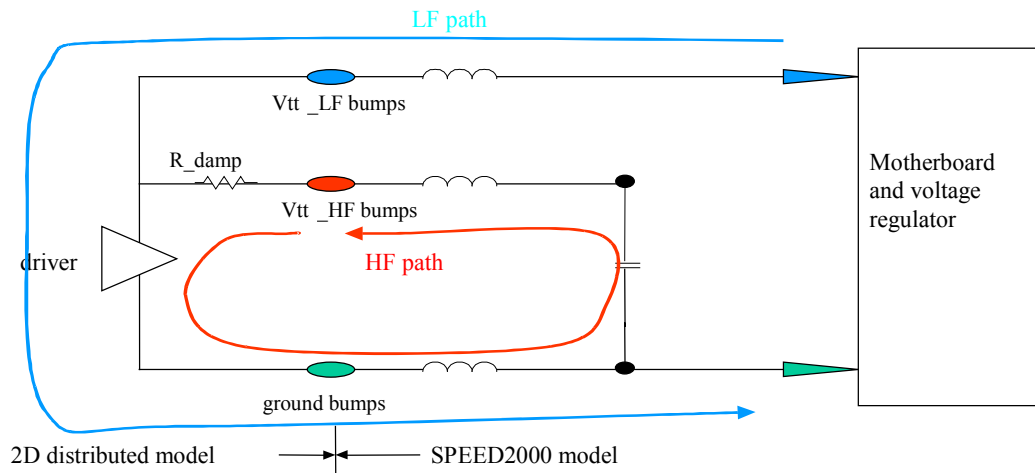


Figure 2: The damping resistors on the high frequency current path damp the SSN.

3. RESULTS

We used the SPEED2000 tool to extract the electrical model from the layout data base and performs the required simulations in the time domain. The results are then transformed to the frequency domain to obtain the impedance profile of the power supply. Based on these information, the resonate frequency and magnitude can be observed. By comparing the impedance profiles of different power delivery designs, the appropriate solution can be found. Figure 3 shows the impedance resonate peak without the damping resistor is about 5 times higher than the one with a 100 mohms damping resistor. Note that it is practically impossible to obtain such a resistor by controlling the series resistance of the decoupling capacitors. Figure 4 shows the on-die noise waveforms with the drivers toggling on the time domain at high speed and shows about 80% reduction on the peak-to-peak voltage with the implementation of damping resistors.

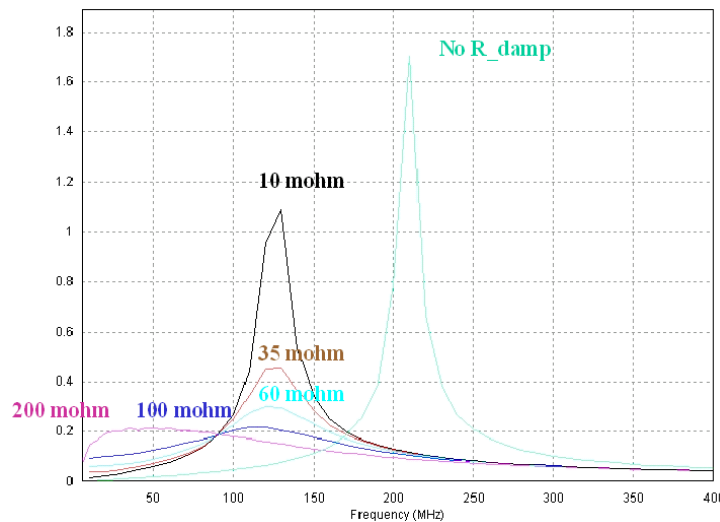


Figure 3: I/O power impedance with and without damping resistor

Another study shown in this paper is the placement of package capacitors. To optimize the placement we needed to know the noise distribution on die. In order to create the worst-case noise, half of the data drivers and all address drivers were toggled at the resonate frequency of the package. Then the on-die noise peak-to-peak noise at different pad ring locations were measured. Figure 4 shows the noise distribution of the padding. More capacitors were placed at the higher noise locations on the die.

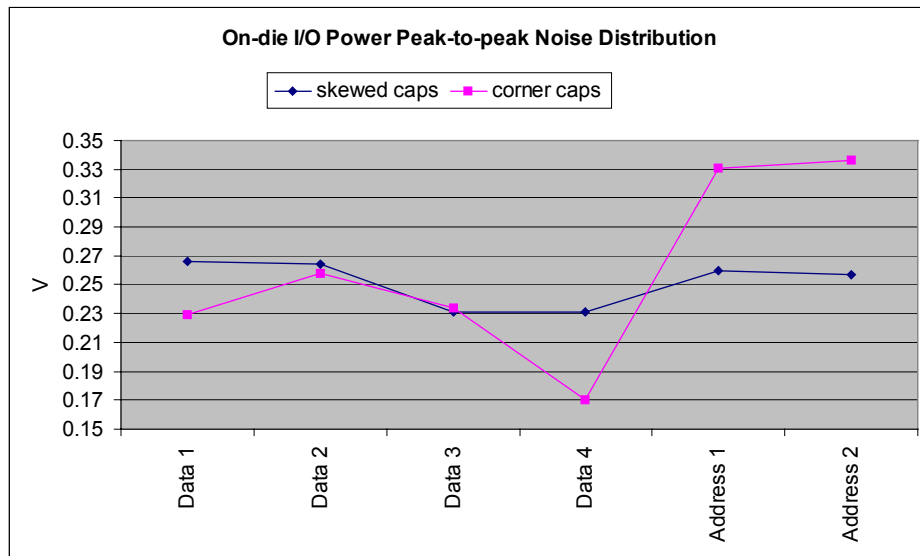


Figure 4: I/O power noise distribution with two different capacitor placement

4. SUMMARY

In this paper, we presented a design technique to separate the high frequency current path from the low frequency path in order to provide a damping resistor for high frequency noise. We have investigated several modeling and simulation technique and concluded that a time domain field solver capable of modeling 3D structures is the best approach for a comprehensive and efficient power delivery design and modeling.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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