

# Mid-Frequency Delta-I Noise Analysis of Complex Computer System Boards with Multiprocessor Modules and Verification by Measurements

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**Abstract**—This paper describes an efficient methodology for mid-frequency delta-I noise analysis of the power distribution network of a computer system. The method allows fast and accurate power noise simulations with SPEED97 on highly complex packaging structures. Simulation results for the mid-frequency power noise amplitudes on module and board planes and dependencies on decoupling capacitor parameters are presented. The package model used for the simulations allow the identification of the dominant resonant oscillations on the power distribution system following a delta-I step and yield the time response of the on-chip, on-module and on-board decoupling capacitors. The simulation results have been confirmed by measurements within 5%.

**Index Terms**—Bypass capacitors, circuit simulation, delta-I noise, decoupling capacitors, power distribution.

## I. INTRODUCTION

WITH the ever-increasing computer system operation frequency and power dissipation of complimentary metal oxide semiconductor (CMOS) chips, variations of the on-chip switching activity can cause large variations of the current demand of a multi-processor multichip module (MCM). The current variations can amount to more than 100 A within a few nanoseconds for an IBM high-performance system. The resulting mid-frequency voltage variations on the power and ground distribution system (delta-I noise in the range from a few to hundreds of MHz) must be contained within specified noise margins with an appropriate low impedance power distribution system and decoupling capacitors on the MCM and the system board to ensure system functionality [1], [2]. On-chip decoupling capacitors are required for high frequency power noise containment and they additionally help to reduce mid-frequency noise.

In this study, delta-I noise created by on-chip switching activity variations has been analyzed using the software tool SPEED97 from Sigrity, Inc., which is based on the finite-difference time-domain method to simulate electromagnetic field propagation inside packages [3]. First, SPEED97 was used to generate a broad-band frequency response to ensure that the power distribution impedance is sufficiently low so

that the noise does not exceed pre-specified values. Second, the time-domain response to a step in current is simulated in SPEED97. The results of this second step are described in this paper. The resulting delta-I noise can be directly compared with noise margins, which were specified by the system designer to guarantee timing and functionality.

Previously published results of analysis using SPEED97 and a pre-runner of this software tool have been on relatively small multilayer packages with four 10 cm by 10 cm power/ground distribution planes [4], or 14 power/ground distribution planes with dimensions of 6.9 in by 5.5 in (17.5 cm by 14.0 cm) [5].

The power distribution of the IBM S/390 (zSeries 900) system board, which has been analyzed in this study, has much higher complexity. There are two voltage levels—1.6 V, 1.9 V—along with a ground reference distribution.

The 1.6 V power/ground system of the system board consists of

- 1) one MCM with 30 chips (700 A average total power supply current) and
  - a) 22 power and ground distribution planes with a size of 11.5 cm by 11.5 cm;
  - b) 42 000 power and ground vias interconnecting these planes;
  - c) 1647 power and ground pins connecting the MCM with the power and ground planes of the system board;
  - d) 275 low inductance ceramic decoupling capacitors at the top surface of the MCM (each 210 nF at 20 C, AVX T60T Ceramic).
- 2) the system board with several slots for memory cards, power supplies and
  - a) 16 power/ground distribution planes with 55 cm by 45 cm size;
  - b) a total of 3876 ceramic capacitors for the following purposes:
    - i) for containing power noise in the mid-frequency and low-frequency ranges;
    - ii) for EMI and EMC;
    - iii) to improve signal integrity at the board connectors.

There are 2886 1 uF 0805 and 670 10 uF 1210 capacitors. These capacitors are mounted both on the front and back side of the board;

- c) 320 1200 uF electrolytic capacitors with a specified equivalent series resistance of 29 m $\Omega$  per ca-

Manuscript received January 16, 2001; revised April 27, 2001. This work was presented at the IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging, Scottsdale, AZ, October 23-25, 2000.

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Publisher Item Identifier S 1521-3323(01)06248-7.

capacitor on daughter cards for low-frequency decoupling.

The MCM has one low-inductance 1.6 V/ground plane pair in thin film technology on top of the MCM ceramic carrier. The ten remaining voltage/ground plane pairs and all 1.9 V/ground plane pairs reside in the ceramic portion of the MCM. It is necessary to include both the MCM and board power/ground distribution system in the simulation for accurate mid-frequency delta-I noise analysis and for understanding of the sensitivities.

In Section II, the methodology which has been applied to generate the input file for SPEED97 simulations will be described. This details the appropriate structure simplifications made to increase the simulation speed. These simplifications are also appropriate for analyzing other complex package structures. In Section III, several simulation results will be discussed including a sensitivity analysis. In Section IV, measurement comparisons to the SPEED97 simulations will be shown.

## II. METHODOLOGY

There are several methods of entering the geometrical data into SPEED97. There is a graphical user interface that can be used to generate the input file for the simulation; the package geometry, all vias and connections between circuits (e.g., current sources and capacitors) and the package can be entered through this interface. Sigrity also provides a translator which provides a means to directly import package design data from an Allegro.brd file. A third alternative was used in [5] which generated the input data from the detailed design data with user-written software. However, these input generation methods have the following problems in case of complex system boards.

- 1) The input of the large number of vias and circuits through a graphical user interface is too time consuming and not practical.
- 2) The brute force translation of the package geometry from our Allegro.brd file would result in a SPEED97 simulation with a large number of vias on a small simulation grid because these vias are on a 400  $\mu\text{m}$  grid and a grid smaller than 400  $\mu\text{m}$  would be required for the simulation. This would reduce the simulation speed significantly and is therefore not practical.
- 3) Moreover, cadence design data are not available at the beginning of the development of a new system when the first analysis is done to determine our decoupling strategy.

We have chosen a variation of the method in [5].

A C-program has been written which quickly generates the complete input file for the SPEED97 simulation of a complex system board. The C-program can be easily adapted to any system development phase and new system boards. The number and placement of capacitors on the board can be changed easily and optimization of the number and placement of the decoupling capacitors is done by changing the input to the C-program. The board design data in the Allegro.brd format is not a prerequisite, but it can be used when it is available. In the early design stages, the C-program converts a listing of planes, vias, and capacitors described in an ASCII

file to SPEED97 input. After the printed circuit board layout is complete, the C-program translates the design data from the Allegro extract file into a SPEED97 input file format. Moreover, the C-program has the flexibility to make use of appropriate structure simplifications to control the simulation time of the SPEED97 analysis.

We now describe how the geometry needs to be simplified to model the IBM zSeries 900 system board. The complex package structure needs to be simplified without losing accuracy to perform the simulations within reasonable time; our goal is twelve hours for a single simulation run. A Windows NT workstation with 450 MHz PentiumII processor and 384 MB RAM was used for the simulations of the IBM system board in this study. The simulation time increases with the number of planes, plane size, and decreasing grid size. The grid subdivides the planes into small sections for the simulation. The grid size depends on the smallest via distance and on the signal rise time. The following simplifications have been done.

- 1) The number of power and ground vias between the MCM planes has been reduced to increase the via distance and simulation grid. The MCM thickness has been reduced too, so that the ratio between number of via pairs to MCM thickness is the same as in reality. This is a key step to accurately model the effective loop inductance of all MCM vias, which is proportional to the via length and to the reciprocal number of power/ground via pairs. The diameter of the vias has been increased to achieve the same ratio of via diameter to distance of adjacent power/ground vias as in reality. This ratio determines the loop inductance of a single power/ground via pair besides the via length [6]. These compensations are applicable for modules such as the analyzed MCM, where all power/ground vias go straight from the top to the bottom power/ground plane pairs.
  - a) In the early design phase, the MCM power and ground vias are extensions of the MCM power and ground pins which yields 1647 vias instead of the 42 000 power and ground vias in the real MCM. 950  $\mu\text{m}$  grid size is sufficient in this case, because the module pins have a minimum distance of 1.1 mm and the minimum via distance in the board (determined by the decoupling capacitor vias) equals 1 mm. Further reductions of the grid size have a negligible impact on the results. The chips are represented by 504 current sources with sinesquare waveform, which start switching at time zero. This represents on-chip switching. The current flow is reversed compared to reality. No dc voltage source has to be connected to the package for these simulations. Fig. 10(a) shows as example the current ( $i_1$ ) for one source with 1 ns cycle time and 200 ps rise- and 800 ps fall time. Since the chips have different switching cycle time in the range from 1 ns to 2 ns and the real wave form is not exactly known, the current source parameters have been varied:
    - i) 1 ns cycle time, 200 ps rise- and 800 ps fall time;

- ii) 1 ns cycle time, 100 ps rise- and 200 ps fall time;
- iii) 2 ns cycle time, 200 ps rise- and 800 ps fall time.

The peak current has been adjusted in order to keep the average current and delta-I value constant. The mid-frequency noise amplitude changed only by 0.5% for these source parameter variations. The on-chip capacitance is modeled as  $R-C$  (resistor-capacitor) elements in parallel with the current sources. The MCM capacitors are modeled as  $R-L-C$  (resistor-inductor-capacitor) circuits and are connected to voltage/ground via pairs at the MCM top surface. Only 4.5 h are required to simulate 100 ns with this MCM model and the board structure simplifications described below.

- b) After the physical design phase is complete, the verification model is built and run. The MCM planes are connected by 3400 power and ground vias in a pattern that represents the individual chipsites. A more accurate MCM capacitor placement results, and each chip can be represented with its own current amplitude and frequency. There are 1280 noise sources connected to via pairs at the MCM top surface to represent the switching activity on the MCM. This model has a 500  $\mu\text{m}$  grid size and requires 23 h to simulate 100 ns. In total this model has 5000 circuits (capacitors and current sources), 30 000 nodes and 21 000 via segments.

The results of these two models are within 5% in mid-frequency noise amplitude and oscillation period, if

- a) all current sources have the same switching cycle;
- b) the current is distributed homogeneously over all sources;
- c) the total delta-I step is kept constant.

The impact of source parameter variations for the different chips is not part of this paper.

- 2) The MCM power and ground plane structure is represented by four planes; a plane pair at the top, and another at the bottom of the MCM. This simplification is necessary for maintaining the simulation run time and avoids large, unreal parasitic plane capacitances which would be created by the MCM thickness reduction to model the correct effective inductance described in step 1, above. This simplification has been tested by varying the dielectric thickness to simulate adding more plane pairs and the conclusion is that the error due to omission of the other MCM planes is smaller than 3%. The top plane pair in the model is a thin film plane pair in case of a thin film on ceramic MCM design (1.6 V) or a ceramic plane pair in the case of a ceramic-only design (1.9 V).
- 3) As in the MCM portion of the model, only the top and bottom board power/ground plane pairs are in the package model. This simplification is essential for a large board in order to achieve acceptable simulation speeds. The full number of board vias in their actual locations for connection to the MCM and on-board decoupling capacitors

are modeled in conjunction with either one of the MCM models. The board thickness, the distance of the top and bottom planes from the adjacent board surface and the via locations and diameter of the vias are modeled as designed. The dielectric thickness between the plane pairs at the top and bottom has been reduced by a factor of four and the plane conductivity increased by a factor of four to achieve for the four planes of the model approximately the same board path inductance and impedance as for the 16 planes of the real board. The principles behind this approximation method simply are

- a) the inductance of two parallel planes is proportional to the plane spacing;
- b) the capacitance of two parallel planes is proportional to the reciprocal plane spacing;
- c) the reciprocal total path inductance of several plane pairs is obtained by the addition of the reciprocal path inductance of the individual plane pairs;
- d) the total capacitance of several plane pairs is obtained by the addition of the capacitance of the individual plane pairs.

The accuracy of this method was tested comparing a simulation using an eight plane board with a simulation using a four plane board. In this case the four plane board has half dielectric thickness for each plane pair and doubled conductivity compared with the eight plane board. Fig. 1 illustrates the method. Fig. 2 shows the noise voltage curves (a 1 ns moving average is used to eliminate the high-frequency noise) on the top MCM planes and on the bottom board planes. The agreement between the simulations with eight planes and four planes approximating eight planes is excellent. The mid-frequency noise amplitude on the MCM differs only by 1.4%, which is acceptable.

- 4) The power/ground planes are solid planes in SPEED97 simulations whereas the real module has mesh planes. The mesh planes have twice path inductance and half capacitance compared with solid planes as found by two dimensional modeling using the IBM CZ2D tool [7]. This has been taken into account by doubling the dielectric thickness for each module plane pair. As a result the oscillation period  $T_1$  (defined in Section III) is increased by 33% due the increased path inductance of the module planes, but the noise voltage on the top module planes is increased by only 2%. It is concluded that mid-frequency noise simulations with solid planes and compensating by increasing the dielectric thickness for the module plane pairs is acceptable for this package. The dc resistance of the planes is also effected by the meshing, but the impact of the dc resistance change on the mid-frequency noise amplitude is negligible.

All power/ground pins of the module, the corresponding board vias and the actual vias of all board capacitors have been included in the simulation model with the C-program using the Cadence design data. The vias in the 1.6 V and GND board planes in the simulation model are shown in Fig. 3 which has been generated with the SPEED97 input file. The on-board

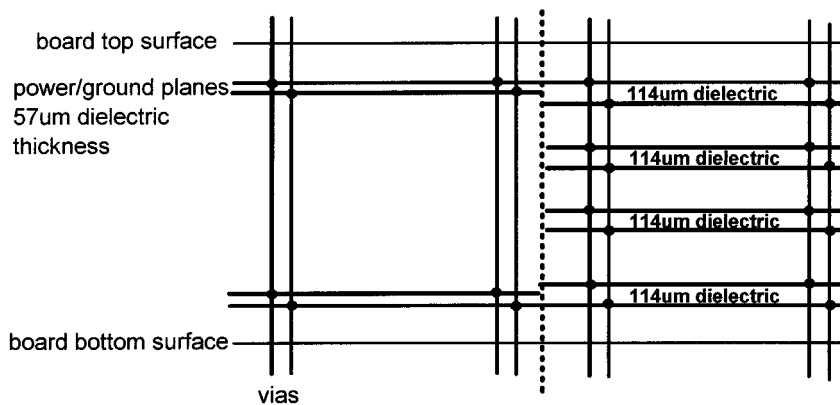


Fig. 1. Board with (right) eight symmetric power/ground planes and (left) with four power/ground planes approximating eight planes.

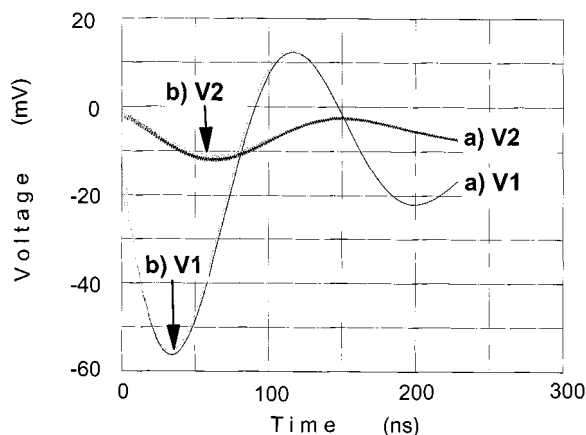


Fig. 2. Noise voltage (1 ns moving average) between the top power and ground plane pair of MCM ( $V_1$ ) and between the bottom power and ground plane pair of the board ( $V_2$ ): (a) board with four planes approximating a board with eight planes and (b) board with eight planes.

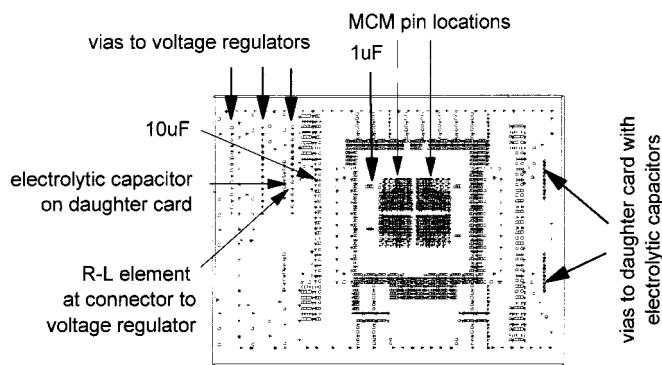


Fig. 3. Vias in the 1.6 V and ground board planes in the simulation model and locations of board capacitors and the  $R-L$  element for which the current flow is discussed in Section III-B.

and on-MCM decoupling capacitors are represented by lumped  $R-L-C$  elements which are connected to the corresponding board and MCM vias. The inductance,  $L$ , includes the decoupling capacitor inductance and the loop inductance from the decoupling capacitor to the nearest power or ground plane of the board or MCM. The current loop has been closed on the board at the location of the connector to the voltage regulator either by lumped  $R-L$  elements or by shorting vias between the board planes (ideal power supply). Both termination methods

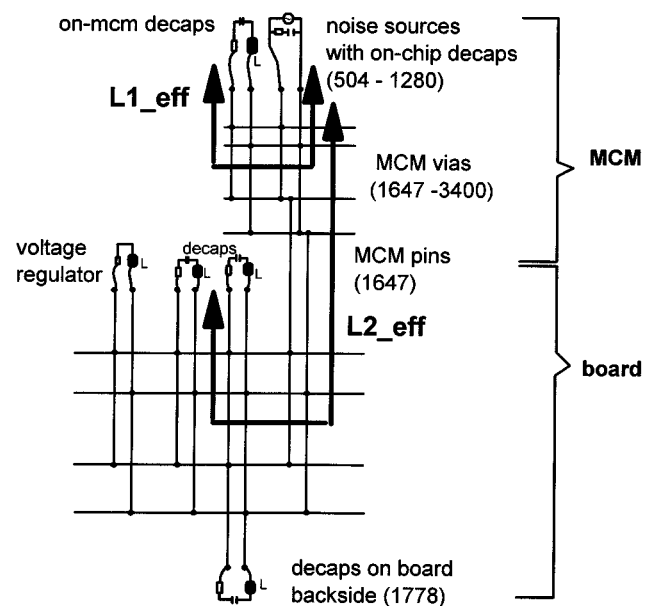


Fig. 4. Package cross section as used for the mid-frequency power delta-I noise simulations.

yield almost identical noise curves within the first 100 ns after a step in current. The  $R-L$  values are derived from properties of the connector and of the voltage regulator capacitors. Fig. 4 is a schematic of the package cross section used for the simulation.

### III. SIMULATION RESULTS

#### A. 1.6 V/Ground Power Distribution System

Fig. 5 shows the voltage variations between the top 1.6 V and ground planes of the MCM close to the MCM center. The current sources at the MCM top surface start switching at time zero with a 1 ns cycle and an aggregate 140 A average current. Study of the system operation has led us to the conclusion that the worst case current step is 20% of the maximum 700 A MCM current. The model is a linear system so the noise voltage is proportional to the delta-I and the results can be scaled to any other delta-I value, if desired. The noise waveform shows three oscillations as seen in Fig. 5.

- 1) A high-frequency oscillation with the same frequency (1 GHz) as the current sources. Increasing the on-chip de-

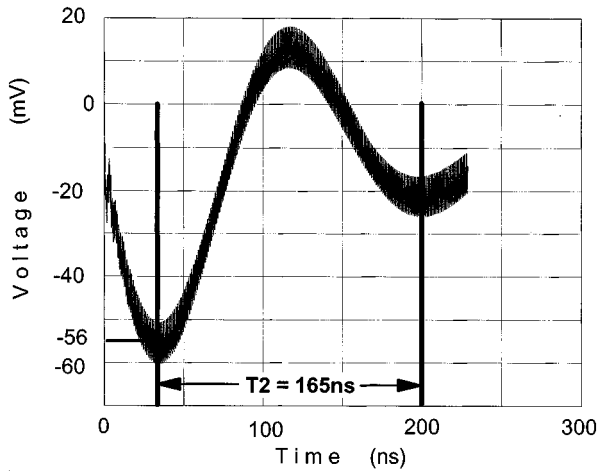


Fig. 5. Noise voltage between the top 1.6 V and ground MCM plane pair for  $\Delta I = 140$  A and 200 nF module decap capacitance. The current sources start switching at time zero with 1 ns cycle.

coupling capacitance decreases the high-frequency oscillation amplitude and, of course, reduces also the mid-frequency noise amplitude.

- 2) A mid-frequency oscillation with 167 MHz ( $T_1 = 6$  ns period), which is visible only during the first 50 ns after the  $\Delta I$  step due to the large damping of the top MCM planes (thin film). This oscillation is hard to be seen with the time scale used in Fig. 5, but it can be better identified in the oscillations of the current flowing into the MCM via [Section III-B, Fig. 10(b)]. This oscillation is caused by the resonant loop formed by the source (on-chip) decoupling capacitors, the adjacent on-mcm decoupling capacitors, and the inductance of the loop between these two sets of capacitors.
- 3) A mid-frequency oscillation with 6.1 MHz ( $T_2 = 165$  ns period) which is caused by the resonant loop formed by all capacitors connected to the module top surface (including the source decoupling capacitors), board decoupling capacitors, and the path between the two sets of capacitors including the effective series inductance of the decoupling capacitors. The amplitude of this mid-frequency oscillation is called  $V_1$  in the following discussion.  $V_1$  equals 56 mV for 200 nF on-mcm decoupling capacitor capacitance, which is below the mid-frequency noise limit that has been specified for this package.

The voltage between the bottom board 1.6 V/ground plane pair close to the module shows an oscillation with the same period  $T_2$ , but with a smaller amplitude. The noise between the bottom board plane pair is recorded at the location of one 1  $\mu$ F board capacitor close to the MCM as shown in Fig. 3 and is called  $V_2$  in the following discussion. The capacitance of the on-MCM decoupling capacitors has a strong influence on the mid-frequency noise amplitudes on the MCM ( $V_1$ ) and on the board ( $V_2$ ) as shown in Fig. 6. The total on-chip decoupling capacitance is constant and equals 7360 nF. The oscillation period  $T_2$  decreases with decreasing MCM capacitor capacitance or decreasing source (on-chip) capacitance. A straight line is obtained in Fig. 7 where  $T_2^2$  is plotted versus the series ca-

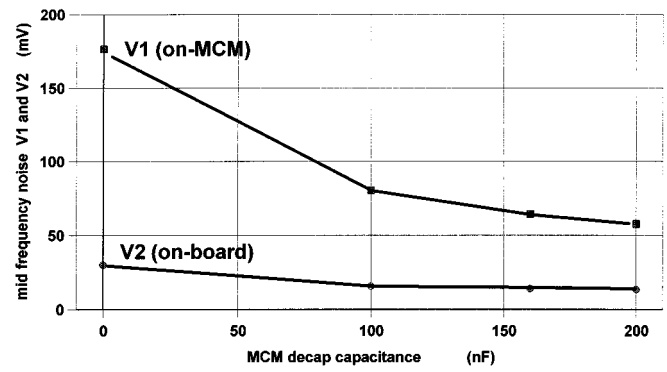


Fig. 6. Mid-frequency noise amplitudes  $V_1$  (top MCM plane pair) and  $V_2$  (bottom board plane pair) for variations of the MCM capacitor capacitance.

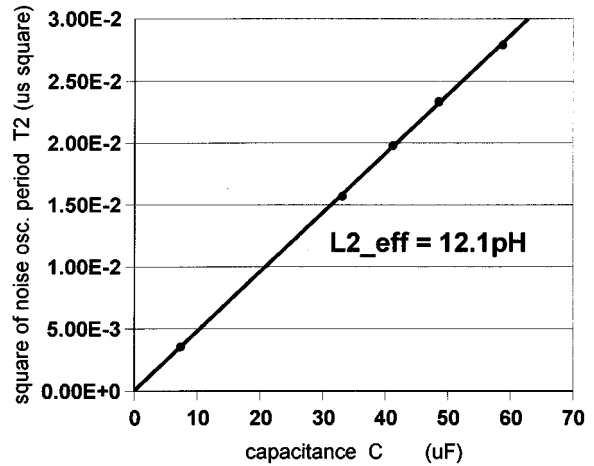


Fig. 7. Square of the noise oscillation period  $T_2$  versus series capacitance of total MCM (including source) capacitance and total board decoupling capacitance.

capitance  $C$  of the total MCM capacitance and the total board decoupling capacitance as calculated by

$$\frac{1}{C} = \frac{1}{C_1 + C_2 + C_3} + \frac{1}{C_4} \quad (1)$$

where

$C_1$  = total on-chip capacitance (all sources);

$C_2$  = capacitance of all on-MCM capacitors;

$C_3$  = capacitance of the MCM plane pairs;

$C_4$  = capacitance of all on-board capacitors.

An inductance of 12.1 pH is derived from the slope in Fig. 7 for the effective loop inductance,  $L_{2,eff}$ , from the MCM and source capacitors to the on-board capacitors using

$$T_2^2 = 4 \cdot \pi^2 \cdot C \cdot L_{2,eff}. \quad (2)$$

Simulations with doubled module pin length yield a 17% increase of  $V_1$  and  $L_{2,eff}$  increases by 6.5 pH.  $V_2$  does not significantly change. The module pins with 6.5 pH effective loop inductance are the major contributor to  $L_{2,eff}$  for this

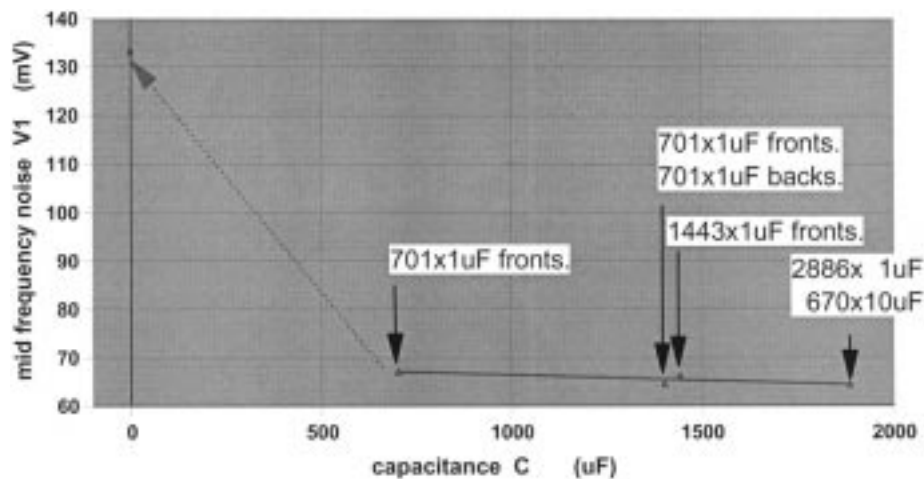


Fig. 8. Mid-frequency noise amplitude  $V1$  (top MCM plane pair) versus total capacitance of the  $1\ \mu\text{F}$  and  $10\ \mu\text{F}$  on-board capacitors.

package.  $L2_{\text{eff}}$  can be reduced by using shorter MCM pins, increasing the number of pairs of power/ground pins, or reducing the spacing between the power and ground pins. By reducing  $L2_{\text{eff}}$ , the oscillation time,  $T2$ , and the mid-frequency noise amplitude on the module is also decreased. It should be noted that an estimation of the loop inductance of all pairs of module  $1.6\ \text{V/ground pins}$  using inductance formula [6] for pairs of cylindrical wires yields an inductance in the range from  $4.1\ \text{pH}$  to  $8.2\ \text{pH}$ ; the  $6.5\ \text{pH}$  in the simulation is well within this range.

The second major contribution to  $L2_{\text{eff}}$  comes from the board planes. Simulations with doubled dielectric thickness for the board plane pairs yield 14% larger amplitude  $V1$ , 34% larger amplitude  $V2$  and  $3.2\ \text{pH}$  increase of  $L2_{\text{eff}}$ . Therefore the contribution of the path from the module pins to the nearest board capacitors to  $L2_{\text{eff}}$  equals  $3.2\ \text{pH}$  for the nominal dielectric thickness. The board capacitors have to be placed as close as possible to the module to reduce this path inductance and the mid-frequency noise amplitude  $V1$ . As expected, doubling the number of board power/ground plane pairs has almost the same effect as a dielectric thickness reduction by factor 2 as shown in Fig. 2.

The simulations show that the 700 on-board capacitors which are the nearest to the MCM are most efficient for the reduction of the on-module mid-frequency noise amplitude  $V1$  (Fig. 8). The addition of more on-board capacitors farther away from the MCM has a negligible effect on  $L2_{\text{eff}}$  and  $V1$ . Simulation up to  $2\ \mu\text{s}$  with 700 board capacitors has shown that the noise on the MCM planes does not exceed the mid-frequency noise amplitude,  $V1$ , during this extended time range. The effect of on-board decoupling capacitor depopulation on the on-board noise is not part of this study.

The dependence of the on-MCM ( $V1$ ) and on-board ( $V2$ ) mid-frequency noise amplitudes on the inductance of the  $1\ \mu\text{F}$  board decoupling capacitors is shown in Fig. 9(a) and (b). This inductance includes the loop inductance from a decoupling capacitor to the top or bottom board plane pair. The nominal inductance value on this board is  $500\ \text{pH}$  using a special pad and via design [8]. Increasing the capacitor inductance from  $500\ \text{pH}$  to  $2\ \text{nH}$  has a 3% effect on  $V1$ . This effect is small because the decoupling capacitor inductance is a relatively minor portion of

$L2_{\text{eff}}$  for this package and the inductance of the  $10\ \mu\text{F}$  board decoupling capacitor has not been changed.  $L2_{\text{eff}}$  increases by 6% ( $0.74\ \text{pH}$ ) only, because the nearest board capacitors are (approximately) in parallel for the  $T2$  resonance. Of course, the increase of  $V2$  with increasing decoupling capacitor inductance is larger (16%).

#### B. Time Response of On-Chip, On-MCM and On-Board Decoupling Capacitors

The current versus time has been recorded during the simulation for one source close to the module center, one module via, one on-MCM decoupling capacitor, one  $R-L$  element at the voltage regulator connector and for board decoupling capacitors at locations which are indicated in Fig. 3. Fig. 10(a) shows the waveforms of

- 1) current  $i1$  from the current source for 1 ns cycle time and 200 ps rise- and 800 ps fall time;
- 2) current  $i2$  flowing through the ‘on-chip’ capacitor parallel to this current source;
- 3) current  $i3$  flowing from the source into the MCM via.

As expected, the current,  $i3$ , equals  $i1 + i2$  (Kirchhoff’s first law). The current  $i2$  follows the switching cycle of the source, because this “on-chip” capacitor has no series inductance. The current  $i3$  rises within 3 ns, then oscillates at first with the mid-frequency oscillation period  $T1$  (6 ns) for a short time due to the large damping [Fig. 10(a)–(c)]. Then  $i3$  oscillates with lower damping with the mid-frequency oscillation period  $T2$  [165 ns, Fig. 10(c)] with a phase shift of a quarter of the  $T2$  period in respect to the voltage oscillation on the top MCM planes (Fig. 5). This phase shift is well known for LC resonant loops with small damping. The final  $i3$  value equals the average current of one source ( $277.8\ \text{mA}$ ), which is half of the source peak current. The current  $i4$  flowing through the on-MCM decoupling capacitor rises within 3 ns as  $i3$ , oscillates at first with approx.  $T1$  period [Fig. 10(b)] and finally oscillates with period  $T2$  and variations in the direction of the current flow [Fig. 10(b) and (c)].

As expected, Fig. 10(c) clearly shows that the currents through the board capacitors and the  $R-L$  element at voltage regulator connector rise much slower than  $i4$ . The current  $i5$

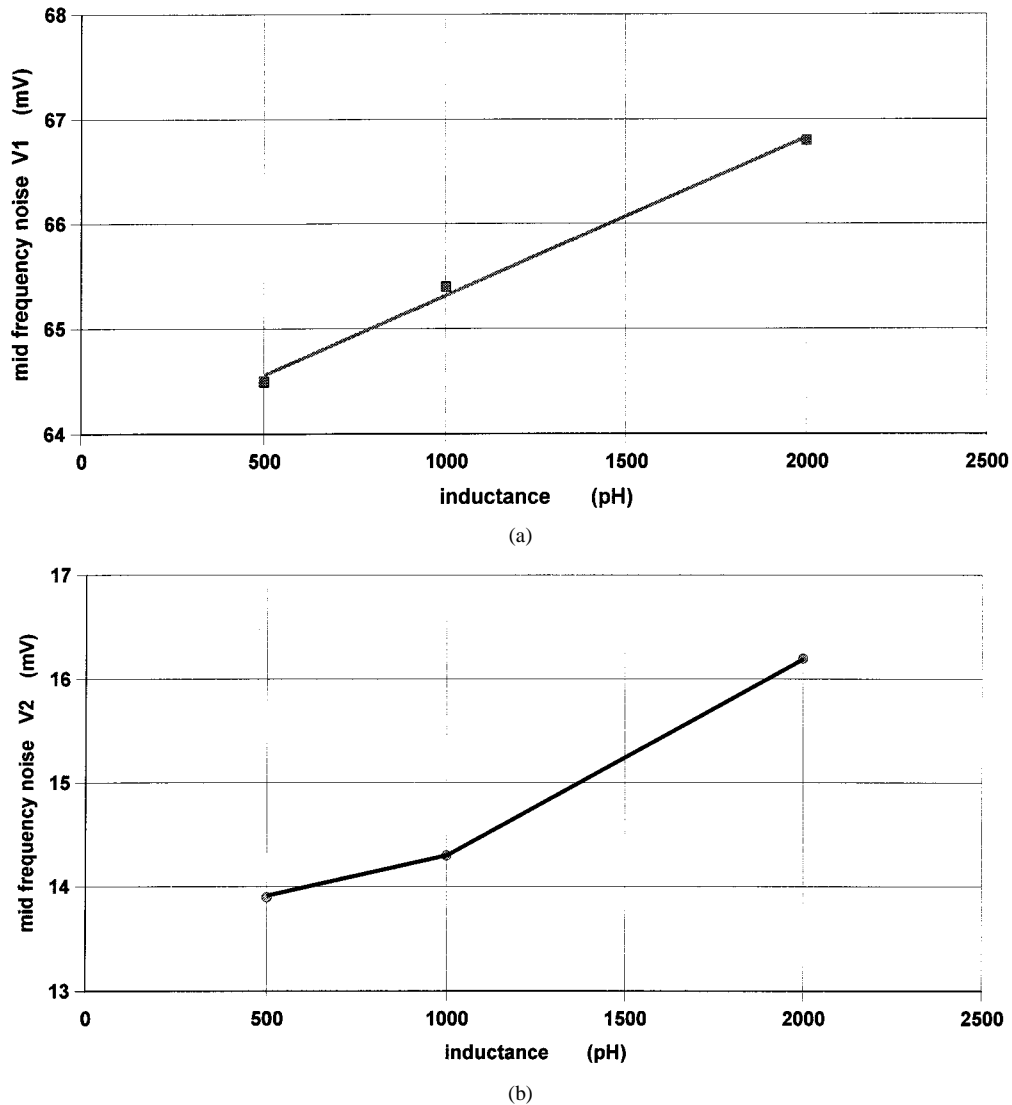


Fig. 9. Mid-frequency noise amplitudes  $V1$  (top MCM plane pair) and  $V2$  (bottom board plane pair) for variations of the inductance of the  $1 \mu\text{F}$  on-board decaps. The inductance includes the loop inductance of the pads and of the vias from the decaps to the next 1.6 V and ground plane pair.

through the  $1 \mu\text{F}$  board decap oscillates also with the period  $T2$  with current flow changing direction. The current,  $i7$ , is the current through one of the 22 capacitors which represent the 320 electrolytic capacitors on the daughter cards. The current,  $i8$ , is the current through one of the lumped  $R-L$  elements which are used in this simulation to close the current loop.

### C. Second Power/Ground Distribution System (1.9 V/Ground)

The second power/ground distribution provides 1.9 V to the clock chip and to the four memory bus adapter chips (MBA1, ..., MBA4) on the MCM. The top MCM 1.9 V/ground planes are ceramic planes and there are only 51 on-MCM capacitors for 1.9 V. Fig. 11 shows the voltage variations on the top MCM planes below one MBA chip (MBA1) for a 6.6 A  $\Delta I$ . Current sources start switching at time zero with a 4 ns cycle time with 2 sine-square pulses per cycle. Again, there are two mid-frequency noise oscillations.

- 1) Oscillations with  $T1 = 13$  ns period (77 MHz) during the first 80 ns caused by the source capacitors and the

loop inductance to the nearest on-MCM capacitors. The damping is smaller for ceramic planes than for thin film planes as seen in Fig. 5.

- 2) Oscillations with  $T2 = 185$  ns period (5.4 MHz) caused by the on-MCM and source capacitors and the loop inductance to the on-board capacitors. Here the effective loop inductance  $L2_{\text{eff}} = 82$  pH. It is much larger than for the first power/ground distribution system, because the MCM has only 84 1.9 V power pins. The simulations yield 66 pH MCM pin loop inductance for this voltage level, which is again within the range of 37 pH to 74 pH using inductance formula.

### D. Two-Dimensional Peak Noise Distributions

Two-dimensional distributions of the peak power noise values have been obtained by the simulations and are shown in Fig. 12(a)–(c). The peak noise is predominantly determined by the mid- and high-frequency power noise amplitudes. The strong impact of the decoupling capacitors at different levels

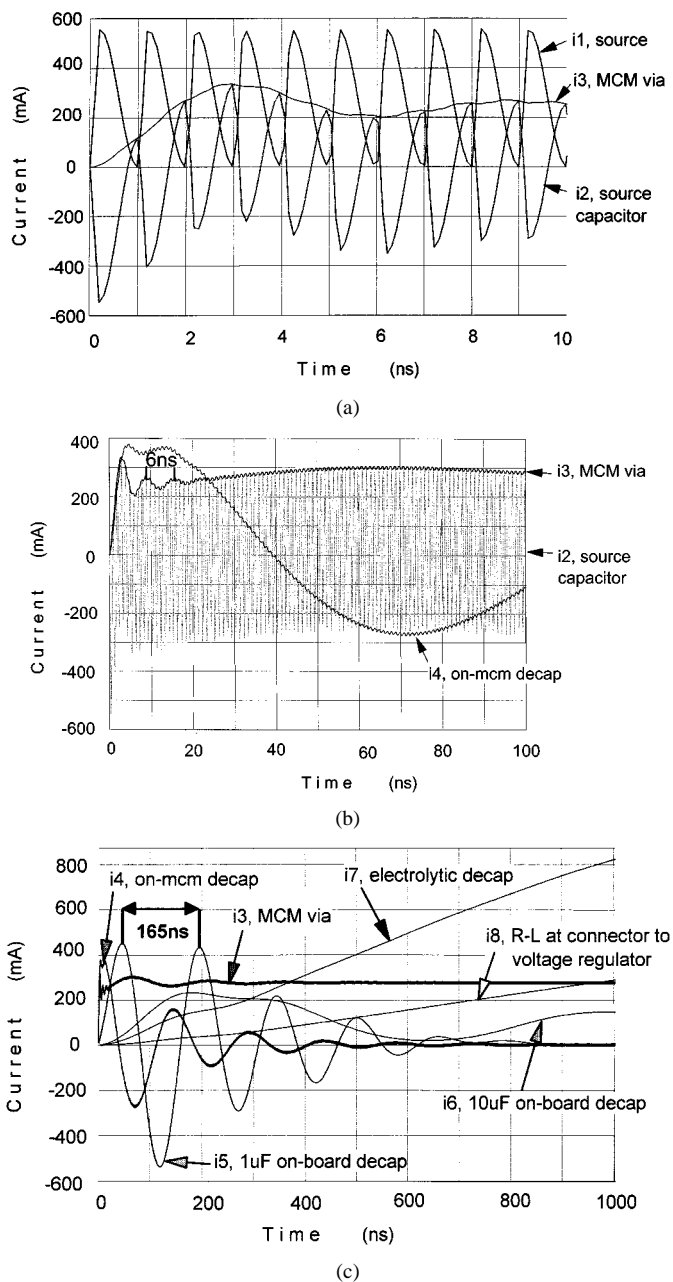


Fig. 10. Currents during the first 10 ns [Fig. 10(a)], 100 ns [Fig. 10(b)], and 1000 ns [Fig. 10(c)],  $i_1$  = source current,  $i_2$  = source (“on-chip”) capacitor current,  $i_3$  = MCM via current,  $i_4$  = on-mcm decap current,  $i_5$  =  $1 \mu\text{F}$  on-board decap current,  $i_6$  =  $10 \mu\text{F}$  on-board decap current,  $i_7$  = electrolytic decap current,  $i_8$  = current through one  $R$ - $L$  element at voltage regulator connector.

on the mid-frequency noise amplitudes has already been shown in Figs. 6, 9(a), and (b) in Section A. The major results of the peak noise distributions are as follows.

- 1) The peak noise on the top 1.6 V/ground MCM plane pairs is relatively homogeneous which is attributed to the large number of decoupling capacitors between all chipsites on the MCM [Fig. 12(a)].
- 2) The peak noise on the top 1.9 V/ground MCM plane pairs is also strongly reduced by the decoupling capacitors which are placed around the clock and the four MBA chips [Fig. 12(b)]. The 4 MBA chips are located in the MCM corners.

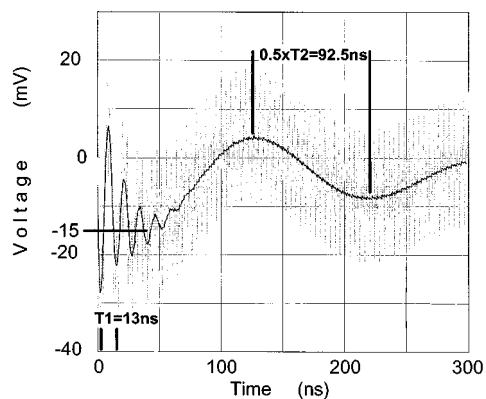


Fig. 11. Noise voltage between the top 1.9 V and ground MCM plane pair (ceramic) at chipsite MBA1 and 4 ns moving average for 4 ns switching cycle,  $\text{delta}I = 6.6 \text{ A}$ .

- 3) The peak noise on the bottom board planes is largest below the center of the MCM [Fig. 12(c)]. This is because the MCM is the noise source and all the decoupling capacitors on the board are outside the MCM area.

#### IV. VERIFICATION BY MEASUREMENTS

The MCM has specially routed wires from the chip power and ground distribution of six chips to 12 module pins. These wires are routed like signal wires from the MCM top surface to the MCM pins without connections to the module power/ground planes inside the module. The pair of wires from each of the 6 chips is routed differentially to remove external noise. Using these 12 pins, we can make a differential measurement of the on-chip voltage variation at the backside of the board. High frequency probes and a specially designed template at the backside of the board are used so that a broad frequency range of noise is measured. In addition, we have also measured the voltage variations on the bottom plane pair of the board near one MCM corner. A  $\text{delta}I$  step of 237 A has been generated on the MCM 1.6 V supply by turning the system clock on or off. The capacitance of the 275 decoupling capacitors on the MCM were in the range from 200 nF to 210 nF, each, during the measurements.

The measured mid-frequency noise oscillation amplitude was 96 mV and the oscillation period 173 ns for the center chip. The simulations yield the following results.

- a) 95 mV noise amplitude and 169 ns oscillation period, if the capacitor capacitance equals 200 nF.
- b) 92 mV noise amplitude and 173 ns oscillation period, if the capacitor capacitance equals 210 nF.

The noise amplitude of the simulations is within 5% of the measurements and the 210 nF exactly matches the oscillation period. Fig. 13 shows an overlay of simulated and measured power noise curves for 210 nF MCM capacitors. The simulations are done using the more detailed “verification model” and  $R$ - $L$  elements at the connector to the voltage regulators. However, the measurements yield a larger damping of the mid-frequency oscillation than simulation show which we are investigating further.

The 14 mV mid-frequency noise amplitude was measured on the bottom board planes below one MCM corner. The simulation yields exactly the same value.

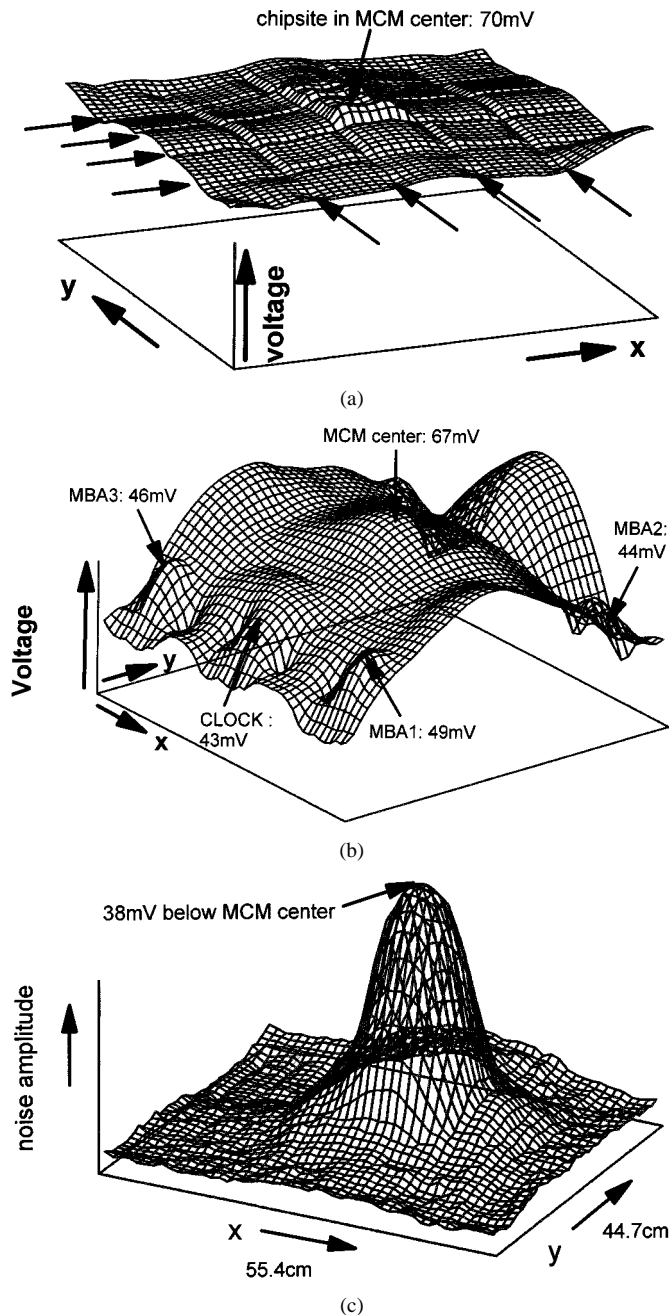


Fig. 12. Two-dimensional peak noise distributions. (a) Peak noise between top 1.6 V and ground MCM plane pair,  $\Delta I = 140$  A. The arrows mark columns and rows with decoupling capacitors between chipsites. (b) Peak noise between top 1.9 V and ground MCM plane pair,  $\Delta I = 6.6$  A. (c) Peak noise distribution between the bottom 1.6 V and ground board plane pair,  $\Delta I = 140$  A.

## V. CONCLUSIONS

Mid-frequency power noise simulations with the software tool SPEED97 based on the finite-difference time-domain (FDTD) method allow the analysis of very complex system boards which include a multiprocessor module and a board with a size of 55 cm by 45 cm. The generation of the simulation input file with a C-program (instead of using the graphic interface offered by the software tool) improves the flexibility and speed for model generation and changes. Appropriate structure simplifications have to be made for complex packages to

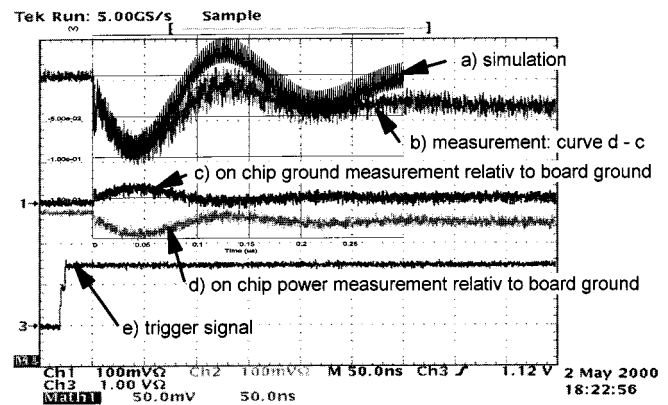


Fig. 13. Comparison between measurements and simulation. (a) Simulated noise voltage for source close to MCM center. (b) Noise voltage for chip in MCM center obtained from the measurement curves (c) and (d) by subtraction. (c) On-chip ground measurement relative to board ground. (d) On-chip power measurement relative to board ground. (1.6 V) measurement relative to board ground.

achieve reasonable simulation times, and acceptable accuracy. These simplifications include a reduction of the number of board power/ground plane pairs and a reduction of the number of power and ground vias interconnecting the module planes. These simplifications result in less planes and a coarser mesh for simulation. If the impedance is accurately maintained by a reduction of the dielectric thickness for each board plane pair and a reduction of the module thickness, the mid-frequency noise amplitude and oscillation period are maintained within 5% as verified by measurements. This provides an early verification of the mid-frequency noise margins during package development and an optimization of the board decoupling capacitor placement which is supported by two dimensional peak noise distribution simulations. The sensitivity of the mid-frequency noise amplitude in dependency of the dominant decoupling parameters, e.g., the capacitance of the module decoupling capacitors, is provided too.

## ACKNOWLEDGMENT

The authors wish to thank G. Katopis, IBM Poughkeepsie, and J. Supper, H. Harrer, and T. Winkel, IBM Boeblingen, for their helpful discussions.

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