A Simulation Study of Simultaneous Switching Noise

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Abstract

This paper describes a new methodology for simultaneous switching noise (SSN) simulations by using a system level signal integrity (SI) analysis software, which is combinations of a quick full wave electromagnetic field solver for multiple-layer structure based on FDTD (Finite Difference Time Domain) and a circuit solver. The solution is based on the geometry, material, stack-up structure, and basic circuit imformation. The simultaneous switching noise issue is studied for two types of chipset packages - OLGA (Organic Land Grid Array) and WBGA (Wirebond Ball Grid Array) - with 40 drivers switching simultaneously.

Different simulation conditions, such as with or without on-die interconnection model, different on-die decoupling capacitor values, are imposed during the simulations. Simultaenous switching noise (SSN) effects such as skew, signal overshoort, ring back, and power-ground voltage fluctuations, are obtained and compared. These data can be used for a design guideline specification or for package performance improvement purposes. It is believed that all these studies are very informative to chip and package analysis and design for high-speed system applications.

Introduction

The rapid and continue advances in integrated circuit process technology have resulted in many new challenges to the interconnection package design. The number of devices that has been integrated on a single chip is dramatically increased, while the devices are becoming more sensitive to the power-ground noise. The simultaneous switching noise (SSN) can cause logic circuits to switch state falsely, if it is uncontrolled [1] and signal integrity issues have significant impacts on the performance of high-speed digital systems [2][3]. Simultaenous switching can also cause problems in signal timing and quality such as signal degradation in rising time, signal channel transmission delay skew, and increase in signal overshoot and ring back at receiver. The effects of simultaneous switching noise depend on the interconnection network between different devices, such as drivers and receivers, including the signal, power and ground paths, the non-linear I/O buffer characteristics, and other parasitic factors.

In this paper, the SSN is studied under different simulation conditions for two types of packages: with or without on-die interconnection models, different on-die decoupling capacitor values, lossy or lossless for on-die decoupling, etc. A package model is first built based on its physical structure such as the geometry, stack-up, and the material of the medium in the package by using a commercial signal integrity (SI) simulation tool – SPEED2000 [4]. Drivers, terminations and the interconnection model are linked to the package by using lumped circuit models. This SI software has merged electromagnetic analysis and circuit analysis into one simulation engine so model extractions is not necessary. That is different from the process the traditional SSN analysis method. The electromagnetic field analysis methodology used by the tool has automatically taken into account the effects of wave propagation, local inductance and capacitance coupling or the coupling between different components, such as power and ground planes, vias and traces.

Through the simulation study, the data of simultaneous switching noise effects are obtained and compared with different simulation conditions that mentioned before. These data can be used for a design guideline specification or for package performance improvement purposes. Meanwhile, because the simulation includes the on-die level interconnection model, the data are more close to the reality. Different on-die level interconnection models have been tested with different on-die decoupling capacitance values. It is found that some decoupling capacitance values will introduce circuit resonance into the package and on-die interconnection system. Different on-die level interconnection models are tested for trying to find out how it impacts resonance in the system. Finding the resonance frequeency in power/ground inconnection system and removing it or reducing the impedance at the resonant frequency near digital system working frequency is the key for reducing power/ground noise or SSN level. It is believed that all these studies are very informative to chip and package analysis and design for high-speed system applications.

Methodology

The SSN simulation environment is assumed to consist of a set of drivers that are connected to loads through a general chip interconnection package with power and ground, as illustrated in Figure 1. Depending on the simulation conditions, the on-die interconnection models and PC boards can be added. The drivers are directly connected to the package when simulating the cases without interconnection models.

The package model is built by using a translator to translate a package layout file (in Allegro brd or mcm format)

into a SPEE2000 input file format. Figure 2 is the screen capture of a typical package layout view in SPEED software. The VSS (Gnd) net is in yellow, VCC (Pwr) in red, and the nets in other colors represent different signal nets. In addition to the package itself, two planes are added below the package to provide simplified power delivery structure of a printed circuit board (PCB) as shown in Figure 2. Although the size of the added planes can be the real size of a PCB, in this case study, the size is selected a little larger than the size of the chip package in order to reduce the mesh numbers. As a result, the total simulation time is reduced significantly without loss of accuracy if not PCB's edge reflect and resonance.

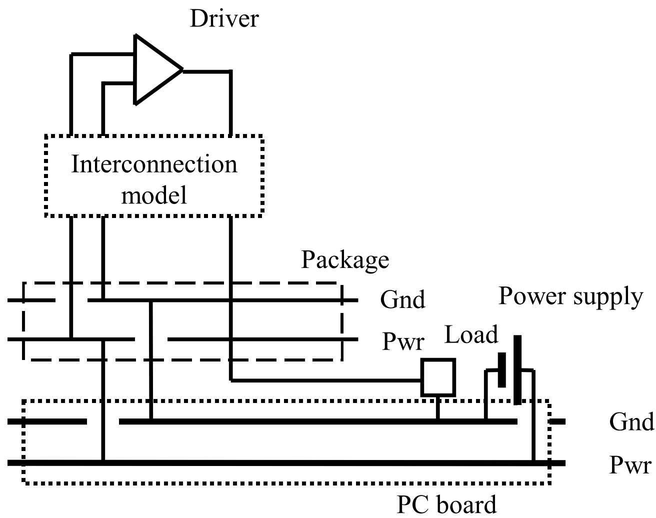

Figure 1. General configuration of a SSN simulation environment.

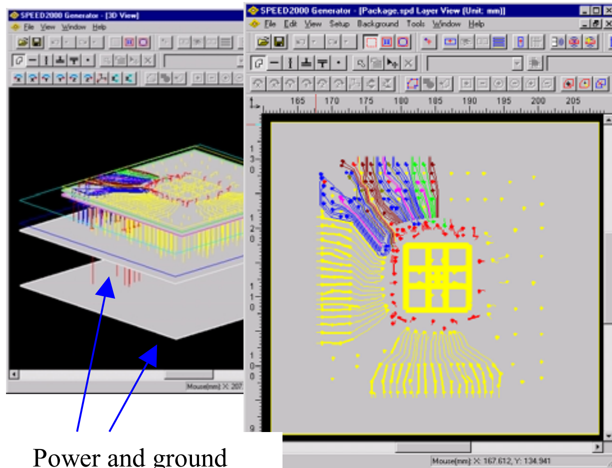

Figure 2. Screen capture of the package to be simulated (3-D view and Top view).

The non-linear I/O buffer output characteristics can be modeled and used in the simulation by using the Voltage-Controlled-Resistor (VCR) element converted from IBIS I/O buffer model or transistor level buffer's characteristic curves.

Die level interconnection models are represented by using lumped circuit elements. The values for the lumped circuit elements are obtained from the actual geometry of the die and bonding wires. An example of the wirebond and on-die interconnection models is given in Figure 3. Five signal nets and their nearby power/ground nets (3 each) are chosen to characterize the equivalent circuit. During SSN simulations, this equivalent circuit is repeatly used depending on the number of drivers switching simultaneously. The elements in red represent Pwr while the elements in blue represent Gnd. Signal nets are in black. The bonding wires are modeled as equivalent RL circuit elements. Mutual inductances between bonding wires within the same set are also taken into account in the simulations. The on-die decoupling capacitor and a serial resistor are added between power and ground as indicated by arrows in Figure 3. The top of the package is connected to the interconnection models through the nodes indicating at the left hand side of Figure 3.

This simulation process for SSN, apparently, is different from a traditional SSN simulation process. For tranditional SSN simulation, a field solver is first used to extract the parasitic parameter models from physical package structures and then the extracted equivalent models and circuit models including buffer and other lumped circuit models are used for simulations within a complete circuit simulation environment such as HSPICE. The former has a lot of advantages over the latter such as simulation speed, simplified process, covering all details of local return path, etc.

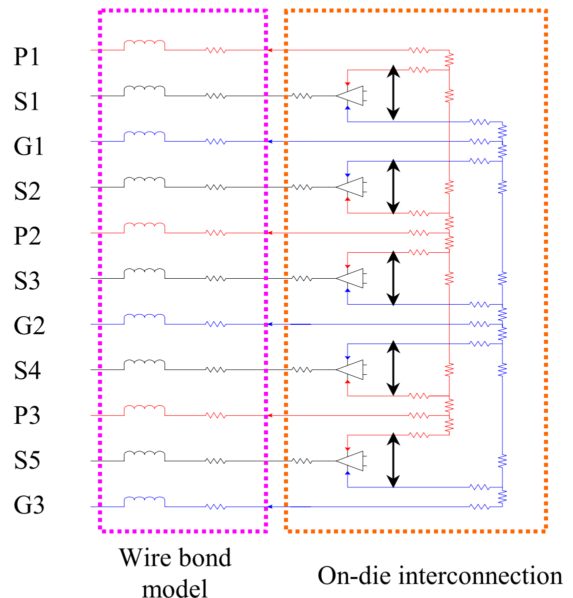

Figure 3. Wirebond and on-die interconnection models for WBGA package. On-die decouplings are added at the locations indicated by arrow.

Results and Discussions

For each package, SSN simulations for different on-die decoupling capacitance and its series resistance are performed. Both even and odd excitation modes are simulated. Odd mode is simulated at selected victim net(s) for each package. Skew is calculated at the receiver (load) end.

By doing SSN simulation with both even and odd excitation modes, one can find out the maximum skew, overshoot, ring back of the victim net at the receiver end. Meanwhile, the voltage fluctuation between power and ground due to the SSN can also be studied with different simulation conditions. In the following figures, three types of curves are shown – driver output voltage waveform, receiver waveform ,and the voltage fluctuation between power and ground at top of the package outside the chip device.

The effect of interconnection model for BGA&C4 package is shown in Figure 4. Even mode waveforms of driver, receiver ,and voltage fluctuation between power and ground without decoupling capacitor for selected victim net are shown. Overshoot, undershoot and power-ground noise slightly decrease when including the on-die interconnection model in simulations.

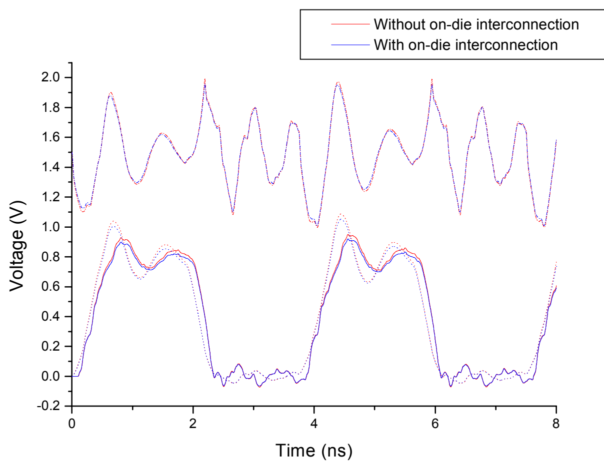

Figure 4. Comparison of voltage waveforms with and without on-die interconnection model for BGA&C4 package.

Figure 5 shows the impact of different decoupling capacitance values on SSN. The serial resistance value R is chosen so that the product of R and C is 40 pF-Ω. Curves of even mode at selected net are shown. For the open case, no on-die decoupling is added during the simulations. The maximum and the minimum power-ground voltage are listed in Table 1. By choosing proper on-die decoupling, the power-ground noise can be reduced dramatically. The skews calculated at the load end for selected voltage levels between even and odd modes are listed in Table 2. Skew is reduced when on-die decoupling is included. When no on-die decoupling is added, the skew can be as large as 40 picoseconds. By adding the decoupling capacitor, the skew can be reduced to 15 ps.

Table 1. Maximum and minimum power-ground voltage for different decoupling capacitance values based on even mode simulations.

	Maximum (V)	Minimum (V)	Difference (mV)
Open	1.9592	1.0092	950
50 pF	1.6223	1.3849	237.4
100 pF	1.5579	1.4503	107.6
200 pF	1.5229	1.4681	54.8

Table 2. Skew comparison for different decoupling capacitance values at selected reference voltages (WBGA package). The skew is in Pico seconds.

	0.25V	0.31V	0.35V	0.39V	0.45V
Open	3.1892	40.8905	40.3189	37.9192	32.0616
50 pF	11.7807	12.2356	12.8682	14.8240	16.4237
100 pF	11.7163	11.8841	12.3170	14.0922	15.4657
200 pF	11.5716	11.5765	11.9101	13.6030	14.8732

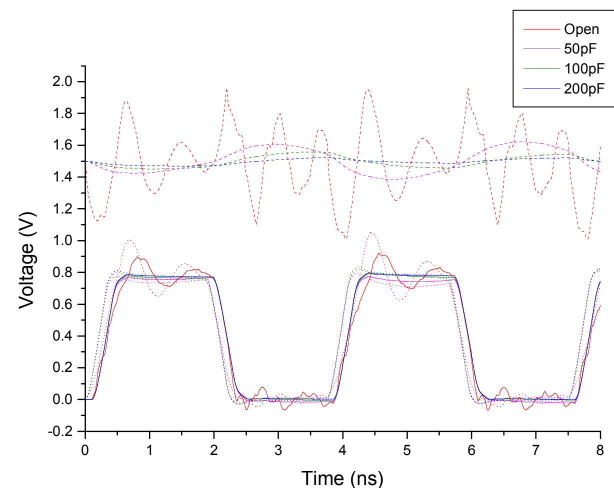

Figure 5. Comparison of voltage waveforms for different on-die decoupling capacitance values (BGA&C4 package).

The effect of the serial resistance values is also studied. Figure 6 shows the results of even mode with 100 pF decoupling capacitor for different serial resistance values. The lossless case indicates no serial resistor is added. No significant difference can be seen from the simulation results.

For wirebond packages, bonding wires play an important role on the performance. Bonding wires have strong mutual inductance between each other and can cause considerably increases in skew. Table 3 lists skew calculated without and with wirebond model. 100 pF decoupling capacitors are added for both cases. For the cases without wirebond model, the decoupling capacitor and its serial resistor are added between power and ground pins at the drivers. When considering the wirebond and die level interconnections, a

model as shown in Figure 3 is imposed. Even mode waveforms at the selected net is shown in Figure 7.

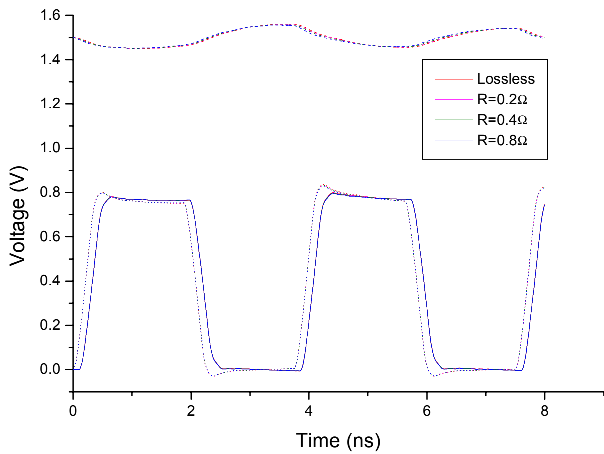

Figure 6. Comparison of voltage waveforms for different serial resistance values (BGA&C4 package).

Table 3. Skew comparison for cases without and with wire bond model at selected reference voltages (WBGA package). The skew is in Pico seconds.

	0.25V	0.31V	0.35V	0.39V	0.45V
Without wire bond	27.184	27.908	26.923	25.138	21.360
With wire bond	102.14	111.14	116.51	121.85	130.64

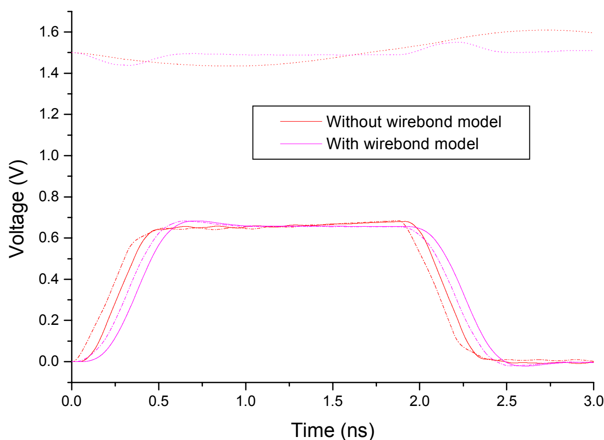

Figure 7. Comparison of voltage waveforms with and without wirebond and on-die interconnection model for BGA&wirebond package.

The impact of different decoupling capacitance values on SSN is also studied. Figure 8 shows the even mode waveforms for different decoupling capacitance values. The skews calculated between even and odd modes for different decoupling capacitance values are listed in Table 4 and the power-ground voltage fluctuations are listed in Table 5. By comparing the results, one can find that on-die decoupling capacitor can reduce on-die power-ground noise but does not have too much help on reducing skew. Bonding wire inductances seem to be the dominant factor of skew.

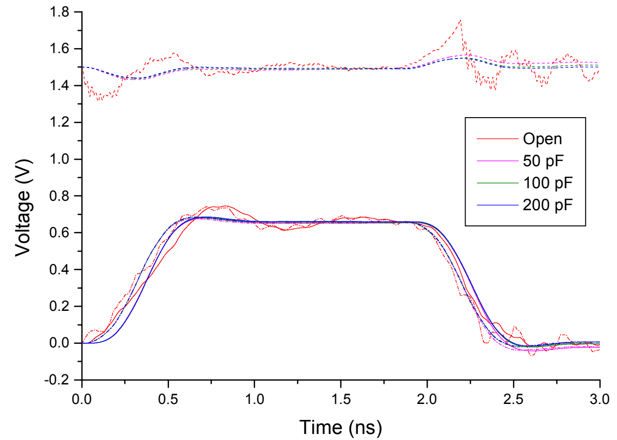

Figure 8. Comparison of voltage waveforms for different on-die decoupling capacitance values (WBGA package).

Table 4. Skew comparison for different decoupling capacitance values at selected reference voltages (WBGA). The skew is in Pico seconds.

	0.25V	0.31V	0.35V	0.39V	0.45V
Open	55.995	82.037	109.221	127.371	149.277
50 pF	100.519	109.624	115.075	120.538	129.601
100 pF	102.139	111.143	116.506	121.853	130.642
200 pF	102.907	111.861	117.181	122.473	131.136

Table 5. Maximum and minimum power-ground voltage for different decoupling capacitance values based on even mode simulations (WBGA package).

	Maximum (V)	Minimum (V)	Difference (mV)
Open	1.7558	1.3143	441.5
50 pF	1.5666	1.4324	134.2
100 pF	1.5508	1.4386	112.2
200 pF	1.5483	1.4420	106.3

Conclusions

In this paper, the effects of bonding wires vs. C4 on-die interconnection, and on-die decoupling on SSN are studied. It has been shown that on-die interconnection has impacts on SSN simulations. To better model the package, die level information has to be included in the simulations. For different packages, different on-die interconnection models have to be built to reflect the actual die level information. On-die decoupling capacitors is one of major methods to reduce power/ground noise level on die and output signal noise, careful selection of on-die and on-package or on board can reduce SSN significantly and avoid any resonance in power/ground interconnection system. In this study, we did not find the series resistor of on-die decoupling capacitor impact on SSN since the resonance did not happen in studied cases and it may play key role when the resonance happens.

Reference

1. Katopis, G. A., “Delta-I noise specification for a high-performance computing machine,” *Proceedings of IEEE*, Vol. 73, No. 9 (1985), pp.1405-1415.
2. Becker, W., H. Smith, T. McNamara, P. Muench, J. Eckhardt, M. McAllister, G. Katopis, S. Richter, R. Frech and E. Klink, “Mid-Frequency Simultaneous Switching Noise in Computer Systems,” *Proceedings of 47th Electronic Components and Technology Conference*, San Jose, CA, May 1997, pp. 676-681.
3. Smith, L., “Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology,” *Proceedings of IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging*, San Diego, CA, October 1999, pp. 163-165.
4. Information on SPEED software of SIGRITY can be found at www.sigrity.com.