Distributed Models for Multi-Terminal Capacitors – Using 2D Lossy Transmission-Line Approach

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Abstract

As clock speeds increase into the gigaHertz regime and rise times decrease into the picosecond regime, the interaction between capacitors and power/ground planes of a package on which they are mounted becomes vitally important to the performance of a power delivery system. To include the interaction between the capacitor and the package, a 3D distributed model is proposed to more accurately evaluate the total loop inductance of a capacitor mounted on pads over vias connected to power/ground planes. The comparison of loop inductance modeling methods based on one-plane and two-plane models using various modeling tools is given. The modeled data match well with the measured data. After validating the distributed capacitor models, performance evaluation of the complete power delivery system based on a lumped and a distributed model of capacitors is made.

1. Introduction

Decoupling capacitors are used extensively in the electronic industry to solve signal integrity problems, which includes simultaneous switching noise (SSN) and electromagnetic interference (EMI) issues [1-8]. As clock speeds increase into the gigaHertz regime, and rise times continue to decrease into the picosecond regime, the parasitics of decoupling capacitors, packages, and their interaction become vitally important to the performance of a power delivery system. As a separate component, the capacitor has a self-inductance that has been well-characterized [9]. The total loop inductance including all interactions between the capacitor, vias, and the package/interposer/board on which it is mounted has also been well characterized [10].

In this paper, a simple one-plane capacitor model is first given. The modeled and measured self-inductance of various capacitors was compared. The combined total loop inductance is directly modeled using both Ansoft's Q3-D and Speed2000 modeling tools. Speed2000 is a new simulation tool aimed at electrical design and evaluation of packages and printed circuit boards [11]. The measured and modeled total loop inductance was correlated. A two-plane capacitor model is also given. The combined total loop inductance is directly modeled using Speed2000 modeling tool. The measured and modeled total loop inductance was also correlated.

After validating the distributed capacitor models, a distributed load current model represented the non-uniform power distribution on a chip is hooked up the on-chip interconnect. The on-chip interconnect is then tied to a 6-layer package. The package model is connected a circuit model with a socket and a motherboard. A power supply model is linked to the other end of this circuit model. Performance evaluation of the complete power delivery system based on a lumped and a distributed model of capacitors is made.

2. Validation of ESL Modeling Methods

An integrated structure with a die side capacitor (DSC), vias, pads, and power/ground planes was chosen for the correlation studies. This structure consists of 2 metal layers, 2 measurement points (location 1 & 2), and a discrete capacitor attached to the top metal layer with 2 pads. One of the pads is in an isolated region that is connected to the layer below with three rows of vias. The DSC structure is shown if Figure 1.

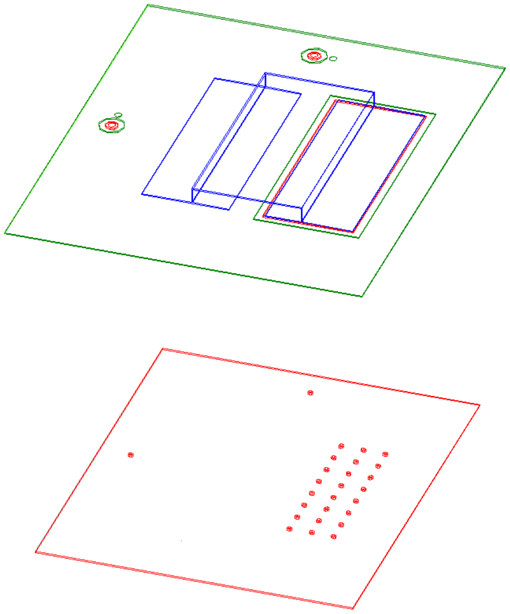

Figure 1. DSC S18 Structure

The loop inductance is 'measured' by measuring the resonance frequency when the discrete capacitor is attached [10]. The resonant frequency, ω_o, is a function of the capacitance value of the capacitor and the parasitic loop inductance of the DSC structure. The equation, $\omega_o = \sqrt{\frac{1}{LC}}$, is used to calculate inductance from the measured resonant frequency given the capacitance value of 1μF. Alternatively, the inductance can be estimated using the imaginary impedance (reactance) waveform Im{Zin}. The inductance can be approximated using L = Im{Zin} / ω. This approximation is good for frequencies that are far enough away from any resonant frequency.

2.1 One-Plane Model using Ansoft

An existing technique for extracting the total loop inductance of DSC type structures using Ansoft is to replace the discrete capacitor with a metal plane [12]. The metal plane is placed at the same height as the lowest capacitor layer that faces the metal planes the capacitor is attached to. The plane effectively shorts the two attachment pads together. The total loop inductance for location 1 from Ansoft is 274 pH. The measured total loop inductance value using the resonance frequency [10] is 286 pH. The difference between measured and modeled data is within 5%.

2.2 One-Plane Model using Speed

The same approach used in the Ansoft modeling can also be used in Speed. However, in the case of Speed, the output will be reactance as a function of frequency, Im{Zin}, instead of inductance. Inductance can be estimated by ignoring the parasitic capacitance and using the equation Zin = jωL. To get the frequency domain results, a gaussian voltage source is applied at the input. The gaussian pulse is used because of it's Fourier transform will lead to a wide main lobe and consequently give good frequency domain results for a wide frequency band. A resistor is added in series to add some damping to the time domain response [13]. However, good results have been obtained without using the resistor or by using other values for the resistance. The resistor affects the total number of time steps required in the simulation. If the voltage or current waveforms in the time domain do not smoothly approach zero at both ends of the time domain data, then the FFT will be subject to spectral leakage [14]. In other words, the FFT applied can introduce false resonance into the frequency domain results. The pulse used had a 1 volt peak amplitude, a 1ns time delay, a pulse width of .7ns, and a 1 ohm resistor in series. The input impedance is calculated at node 2 in the Speed2000 circuit shown above. The impedance is calculated by using the voltage at node 2 in reference to node 0 divided by the current through the resistor.

Some modifications to the Ansoft structure shown in Fig. 1 have to made to make the structure work in Speed. The most important modification is to make the capacitor legs sets of vias instead of rectangular metal pieces since Speed is not capable of handling vertically oriented metal layers. The diameter of the vias are chosen such that the total area of a set of vias matches the total area in the original metal piece. The resulting radius is

$$r = \sqrt{\frac{ab}{\pi N}} \tag{1}$$

where r is the radius, N is the total number of vias, and ab is the cross-sectional area of the rectangular section used to represent one of the capacitor legs. In this case N was set to 16, and a radius of 28um was calculated. The results for location 1 are shown below. The Im{Zin} compares well with the measurements, as shown in Fig 2. The inductance as a function of frequency is then estimated using L = Im{Zin} / ω. The result is shown in Fig 3.

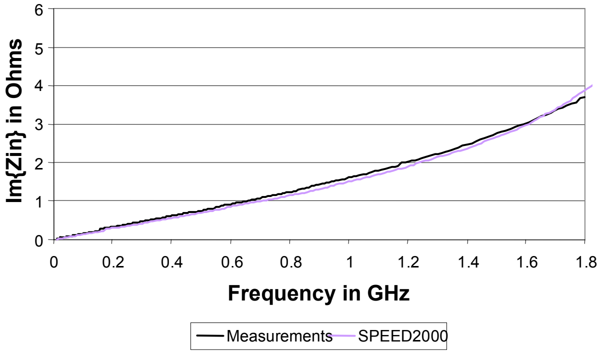

Fig 2. Location 1: Im{Zin} as a function of frequency

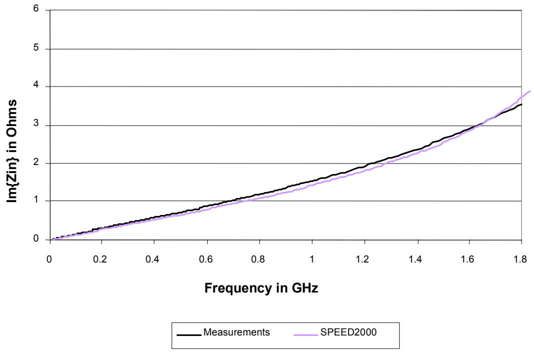

Fig 3. Location 1: Im{Zin}/ ω as a function of frequency

At low frequencies the measured inductance decreases dramatically due to the resonance associated with the discrete capacitor (1µF). The inductance of both the Speed simulation and measurements goes up with higher frequencies because of a high frequency resonance point that is present in the structure. This high frequency resonance is due to the effective loop inductance and the parasitic capacitance not associated with the discrete capacitor.

The difference in magnitude of the two curves in Fig 3 may be partly due to the inaccuracy of modeling the capacitor legs as sets of vias. For example, if N=30 in (1) then r is calculated to be 20um. With this arrangement of vias the overall low frequency inductance calculated by Speed varies by 2% from Fig 3.

The same methodology is applied to location 2. The results for location 2 are shown below in Figs 4 – 5.

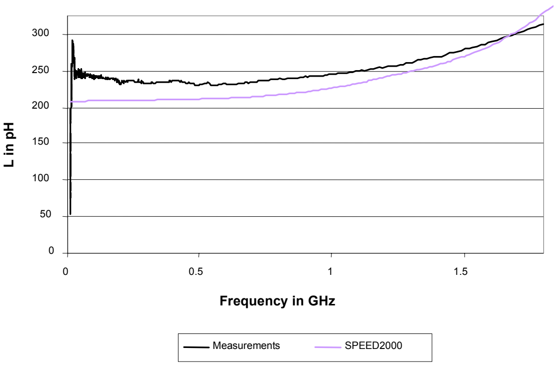

Fig 4. Location 2: Im{Zin} as a function of frequency

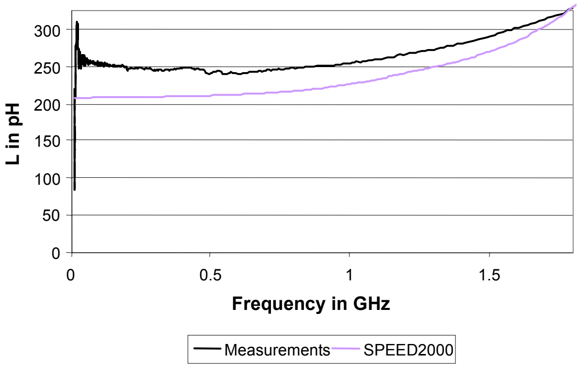

Fig 5. Location 2: Im{Zin}/ ω as a function of frequency

2.3 Two-Plane Model using Speed

Although the inductance can be extracted using the POR technique that was developed for Ansoft, Speed is also capable of using a new methodology to extract inductance. Instead of replacing the discrete capacitor with a metal plate, this technique models the discrete capacitor with a two-layer capacitor created from a very thin high K dielectric. In this case the Speed simulations are closer to the original structure that is being measured.

As in the previous method, inductance is estimated using L = Im{Zin} / ω. In order to obtain the waveform Im{Zin} / ω correctly, there must be enough time steps in the Speed simulation to capture the low frequency behavior that occurs near the resonance. The total number of time steps, N, to get the most accurate result is

$$N = \frac{T}{\Delta t} = \frac{1}{f_o \Delta t} \qquad (2)$$

where T is the total time period, f_o is the resonant frequency (around 10 MHz in this case), and Δt is the time step in Speed. In this case the number of time steps is 0.64 million, but the results still showed good accuracy at low frequencies for 0.13 million time steps. At 0.13 million time steps, the simulations took 1.5 hours. The results are seen below in Figs 6 – 7.

The effect on the inductance estimated using L = Im{Zin} / ω is exactly what is expected. By using a parallel plate capacitor instead of a shorted metal plate, the low frequency reactant behavior of the structure is now much closer to the measured behavior. This drop in Im{Zin} / ω is due to the resonance associated with the loop inductance and the discrete capacitor. The results from the new methodology also demonstrates the accuracy achieved using one plane modeling technique [12] since there is little difference in the inductance estimated at frequencies that are not close to the resonant frequency.

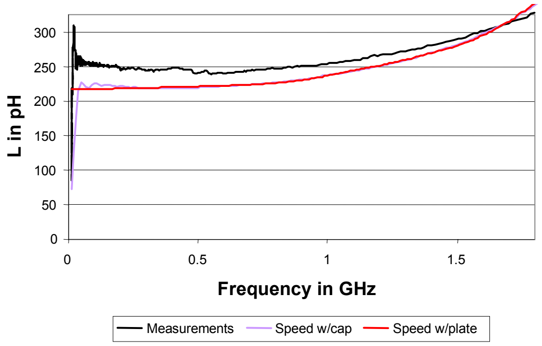

Fig 6. Location 1: Im{Zin}/ ω as a function of frequency

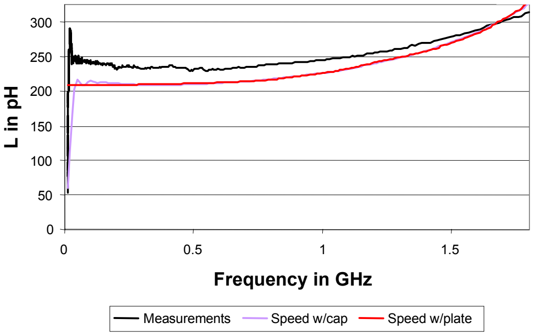

Fig 7. Location 2: Im{Zin}/ ω as a function of frequency

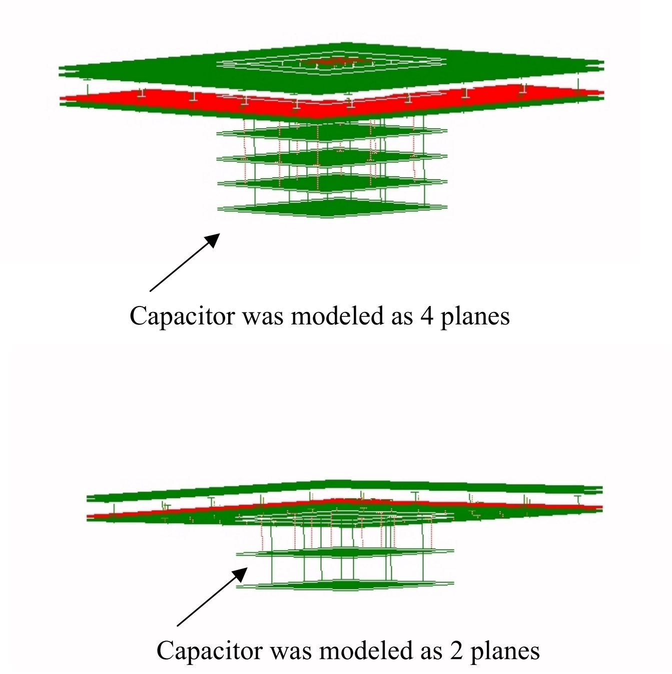

Figure 8. distributed capacitors under a six-layer package.

3. Comparison of Distributed and Lumped Models

To test the methodologies described in the previous section, a six-layer package was modeled on Speed. The package stackup is Signal-Vss-Vtt-Vcc-Vss-PGA Pads. The details of the package can be found in Ref. 15. A distributed 5x5 load current model represented the non-uniform power distribution on a chip is hooked up the on-chip interconnect. Each of these load current sources is modeled as a pulse function with a period of 30ns. The on-chip interconnect is then tied to the six-layer package. The package model is connected a circuit model with a socket and a motherboard. A power supply model is linked to the other end of this circuit model. Figure 8 shows a 2-plane and a 4-plane distributed capacitor models connected to the six-layer package model in Speed.

Figure 9 plots the worst-case voltage differential between adjacent Vcc and Vss nodes. The waveforms indicate that the difference between the distributed and the lumped models can be significant.

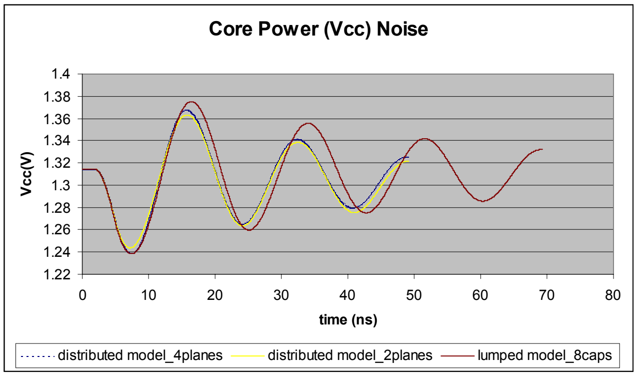

Figure 9. Core power noise for three different models.

4. Conclusion

To include the interaction between the capacitor and the package, an integrated model was given for evaluating the total loop inductance of a capacitor mounted on pads over vias connected to power/ground planes. The comparison of loop inductance modeling methods based on one-plane and two-plane models using various modeling tools is introduced. Both one-plane & two-plane models show good correlation between modeled and measured data using an integrated structure with a DSC, vias, pads, and power/ground planes. After validating the distributed capacitor models, performance evaluation of the complete power delivery system based on a lumped and a distributed model of capacitors is made. The traditional lumped model obtains larger inductance value than the distributed model. The simulation results indicate that the difference between the distributed and the lumped models can be significant.

The results also show that Speed is capable of fast and accurate simulations of complicated structures. In addition, based on the evaluation some important observations about Speed's modeling capabilities can be made. First of all, Speed doesn't consider the parasitics of the portion of a via that protrudes above the top plane or below the bottom plane or penetrates through a plane. However, this portion of the via can be modeled by Speed by adding lumped RLC circuits. Second, the resistance of a via is not modeled in Speed2000, but will be considered correctly in the near future. Also, Speed doesn't consider fringing fields that originate from the edges of planes.

Acknowledgments

The authors would like to thank their Manager, PR Patel for his support of this work. The authors would also like to thank their colleagues Michael Cornelius and Jayashree Kar for their assistance in collecting supporting data.

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