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Achieving 3.2 Gb/s, 400 MTS AGTL+
IO through robust power delivery
design with minimal package size

Chee-Yee Chung
Weimin Shi
Alex Waizman

Intel Corporation

Abstract

This paper details the design of an optimized and robust IO power delivery network for the 400MTS (double pumped 200MHz), 3.2Gbytes/s, AGTL+ Processor-Side Bus (PSB) that links the Intel MCH chipset and the Intel® Pentium® 4 processor. The MCH package size is minimized through power/ground BGA ball count reduction, while compensating the degraded power delivery through the addition of on package decoupling capacitors. This optimized power delivery design is derived through exploring the preferred current return path, and analyzing the power network behavior in both time and frequency domain. Validation results in actual system environments show close correlation with predictions.

Authors Biographies

Chee-Yee Chung is currently with the Desktop Platforms Group, Intel Corp. in Chandler AZ where he is responsible for the signal integrity analysis of chipset design. Prior to this, Chee-Yee worked in the area of package design and electrical analysis. His technical interests lie in all areas of high speed interconnect electrical performance.

Weimin Shi is a senior analog engineer in the Desktop Platform Group, Intel Corporation in Hillsboro OR. His technical interests include modeling of signal integrity (SI), electromagnetic compatibility/interference (EMC/I) and electrostatic discharge (ESD) in high-speed electronic systems.

Alex Waizman is a Principal Engineer of Intel iMPG Design Center. Alex graduated from the Technion, Institute of Technology in 1986 with BSEE degree, and joined Intel in 1988. Alex worked on a variety of analog like topics including: Ethernet Physical access, Delay Line and Phase Locked Loops, High speed testing and High speed IO design. Today Alex is responsible for the package design, motherboard integration and silicon power delivery in the iMPG Design Team

Introduction

In the past, the design analyses of the IO interconnect of a bus system and its respective power delivery network is usually treated separately. There are probably two motivations behind this approach. By combining the IO interconnect and power delivery network analysis together, the complexities of the simulation models are beyond the capability of simulation tools and computing resources. On the other hand, it is commonly agreed that we could decouple the two networks if we can ensure a stable power delivery system such that its impact on the IO system performance is negligible. In this case, a stimulus representing a certain di/dt and ICC current consumption of the IO system is used to determine the worst-case noise in the power supply network. If this worst-case noise is within the pre-determined voltage tolerance target, then in the IO simulations, a perfect power supply can be assumed.

As bus speeds and edge rates increased, it becomes extremely challenging to decouple the IO interconnect design from the power delivery design. The objective of this paper is to present the IO power delivery design, analysis and validation of the Intel® Pentium® 4 processor (CPU) bus Interface (PSB) on the Northbridge Memory Controller Hub (MCH) device. We will first describe the PSB interface and the design constraints placed upfront. Next, we will describe the design considerations made in deriving the final implementation. A combination of frequency and time domain predictive analyses are used and the respective validation results were collected. Through this design analysis process, we have been able to arrive at a cost optimal solution. Validation results demonstrate the accuracy of the predictive analyses and robustness of the PSB interface.

PSB Interface Overview & Design Constraints

The Intel® Pentium® 4 PSB (Processor Bus Interface) is an AGTL+ Bus that contains 64 data signals, 8 strobes signals (2 strobes per 16 data), 32 address signals, and some other miscellaneous signals and clocks [1]. With 400MTS data signals, the PSB provides a 3.2GB/s bandwidth between the CPU and MCH. The signals are designed as 50Ω ground (VSS) referenced transmission lines on the processor and chipset packages, as well as on the motherboard, and series terminated with 50Ω resistor on both the CPU and MCH to avoid reflections.

Package			Motherboard		
Layers	Thickness (um)	Function	Layers	Thickness (mil)	Function
SR	21	Solder Mask	SR	1	Solder Mask
3F	17	Conductor / Routing trace	Outer Top	2.1	Conductor / Component Place
ILD32F	30	Build up Dielectric	ILDTOP	4.5	Dielectric - FR4
2F	17	Conductor / Planes	Inner Top	1.4	Conductor / Planes
ILD21F	30	Build up Dielectric	Core	44	Dielectric - FR4
1F	25	Conductor / Planes	Inner Bot	1.4	Conductor / Planes
Core	800	Core Dielectric	ILDBOT	4.5	Dielectric - FR4
1B	25	Conductor / Planes	Outer Bot	2.1	Conductor / Routing trace
ILD21B	30	Build up Dielectric	SR	1	Solder Mask
2B	17	Conductor / Planes	total	62	
ILD32B	30	Build up Dielectric			
3B	17	Conductor / BGA			
SR	21	Solder Mask			
total	1080				

Table 1 Stack-up for package and motherboard design

The MCH die used for this study is packaged in the FCBGA (Flip Chip Ball Grid Array) package [2, 3]. The minimum number of layers for this package technology is 6-layer, and the stack-up is shown in Table 1. This package technology and design innovation utilizing it has been previously described in [2,

3]. For high frequency power delivery decoupling, 0306 (30 mils x 60 mils, with terminals on the 60 mils dimension) reverse geometry form factor multi-layered ceramic capacitors (MLCC), with 0.22uF each, can be placed on the package. A standard 4-layer desktop motherboard with its stack-up shown in Table 1 is used for the connection between the CPU and the MCH.

Design

The IO power supply voltage (VTT) is set at 1.5V nominal and the design goal is to maintain +/- 5% tolerance (TOL) at DC and low frequency, while allowing an additional +/- 5% TOL for AC and higher frequency fluctuations. Thus, a total of +/-10% voltage fluctuation on the power supply is allowed on the die. The worst-case steady state current for the IO interface is estimated to be 2.5A. These, together with the current changing rate behavior are summarized in Table 2.

Voltage			Current		
Parameter	Value	Units	Parameter	Value	Units
VTT	1.5	Volts	ICCmax	2.5	Amps
DC Tol	5	% tolerance from VTT (+/-)	Freq	200	Mhz (Max data rate)
AC Tol	5	% tolerance from VTT (+/-)	di/dt	5	A/ns
Total Tol	10	%			

Table 2 Power delivery design requirements

The intent of the design is to achieve a power delivery network impedance that when excited by the switching current from bus activities, the noise generated in the voltage supply will still meet the tolerance requirements. To facilitate the design of the network impedance, it is best to design in the frequency domain. Out of the +/- 5% DC TOL, +/- 1.5% is usually reserved for band gap setting accuracy due to the oscillation from switching voltage regulator module. From Extended Adaptive Voltage Positioning (EAVP), using the remaining +/- 3.5% DC TOL budget, the target impedance (Z) for the power delivery network design from DC to infinity frequency is then [4, 4]:

$$Z(f) = \frac{2 * Tol * VTT}{ICC} = \frac{2 * 0.035 * 1.5}{2.5} = 42m\Omega$$

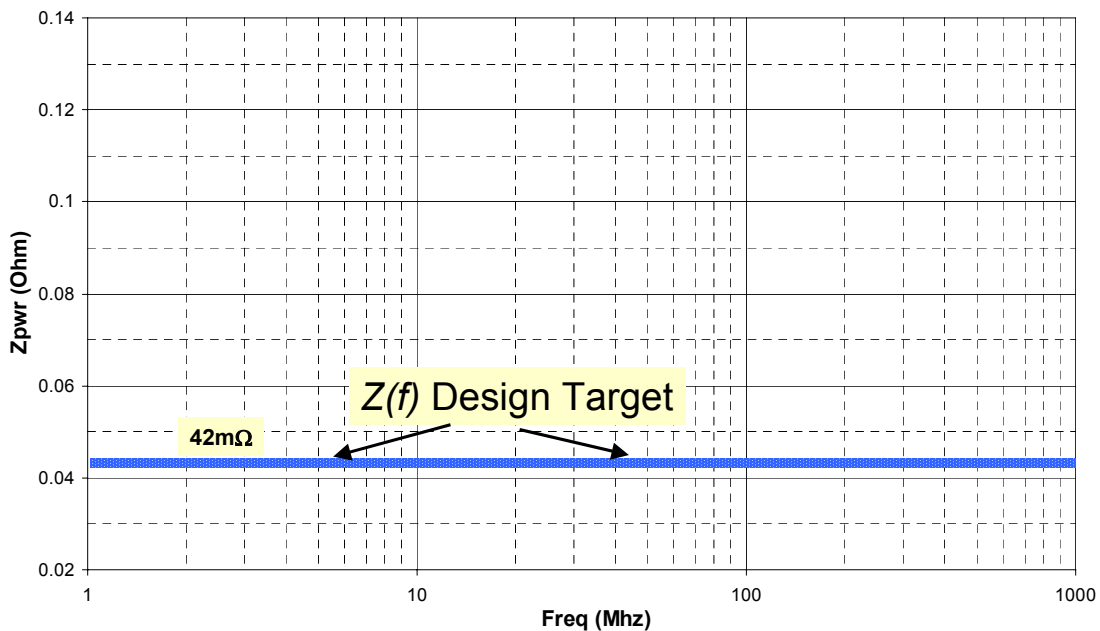


Figure 1 Z(f) design target for the interface.

This is simply shown as a straight line in Figure 1. The remaining 5% AC TOL is set aside for mismatch and other tolerances (manufacturing, environment) that might occur.

From early silicon layout, which is validated later on, the amount of on-die capacitance is estimated to be 41.5nF with 0.03mΩ of series resistance. Following the design approach identified in [5], we could not achieve the required effective loop inductance with a 37.5mm square package to meet the $Z(f)$ requirement. In order to reduce this inductance, we would have to either increase the package body size (which will increase the size of the power corridor, more BGA balls, etc.) or move the capacitors onto the package closer to the die. Detailed cost and layout analysis resulted in placing the capacitors onto the package and maintaining the original package size.

The left of Figure 2 shows the MCH package BGA footprint and the associated power corridor for the PSB interface. The right of Figure 2 shows the placement of capacitors on the die side of the package. These capacitors are connected to the 2F (VSS) and the 1F layers (VTT) of the package where the stack-up is as described in Table 1. The VSS and VTT planes then connect to the die through vias and flip chip solder bumps. In order to control the resonance peak due to interaction between the package capacitors and on-die capacitors, additional resistance are added in series with the package capacitors, besides their inherent ESR (equivalent series resistance). However, this additional resistance could not be added in series with the power supply network, as it would increase the DC resistive IR noise. Thus, a different VTT plane, on the 1B layer of the package, is used for delivering power from the motherboard to the die. The 1B plane is also used as current path to recharge the package capacitors, through connections on the die. The schematic of the resultant power delivery network, illustrating this design scheme, is shown in Figure 3.

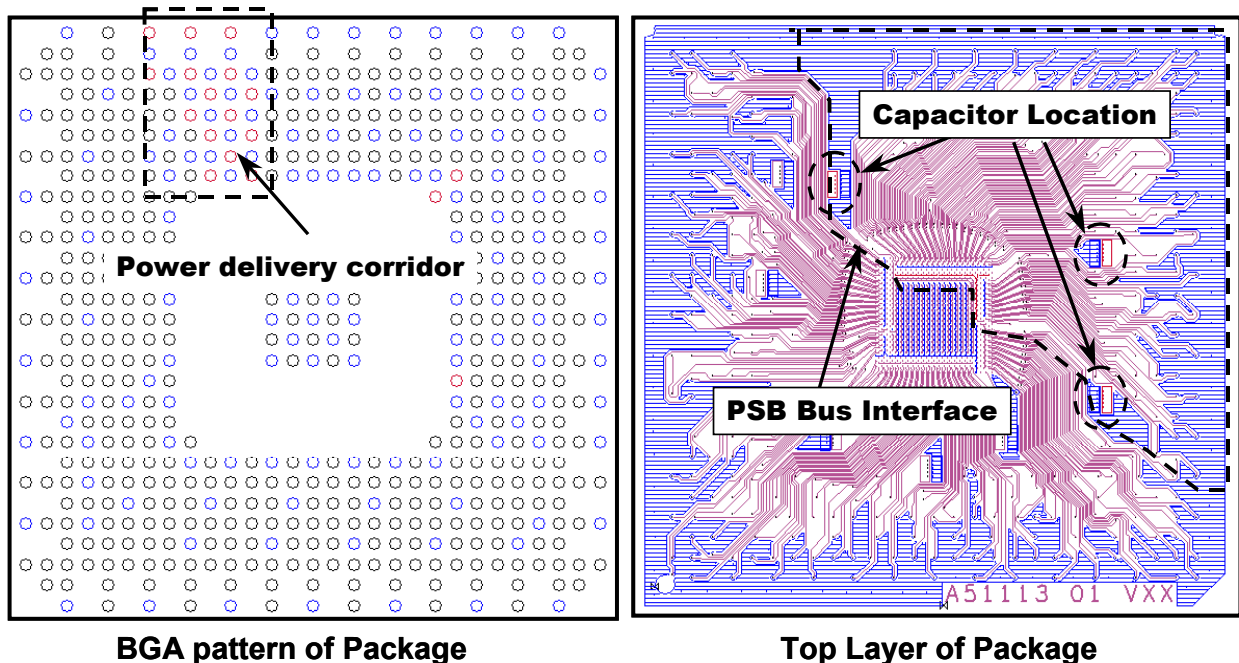


Figure 2 Package BGA ballout showing the power corridor for PSB interface and Package Capacitor placement

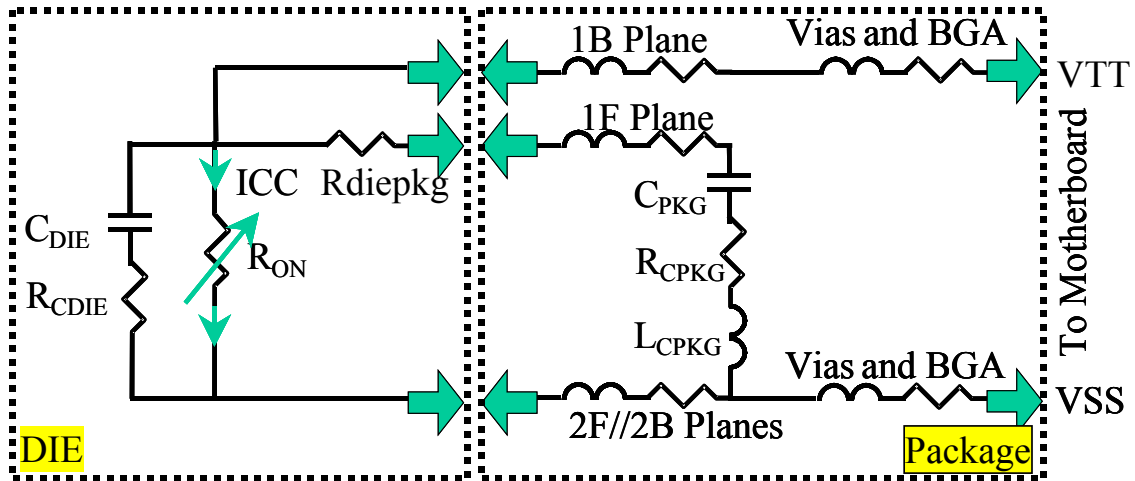


Figure 3 Schematic showing package capacitors connection and package planes utilization.

Predictive Analysis

To analyze the performance of the design and to validate the design solutions, analysis in both time and frequency domains are performed [7]. Analysis in frequency domain allows the study of the impedance profile of the power delivery system to ensure no significant resonance is present. These are accomplished through SPEED2000 simulations [8]. Ansoft Q3D model extractions were also employed to characterize mounting parasitic of the package capacitors [9]. For the analysis performed, the plane patches on the package and motherboard, the package pins and socket together with all the vias were modeled in SPEED2000, and is shown in Figure 4.

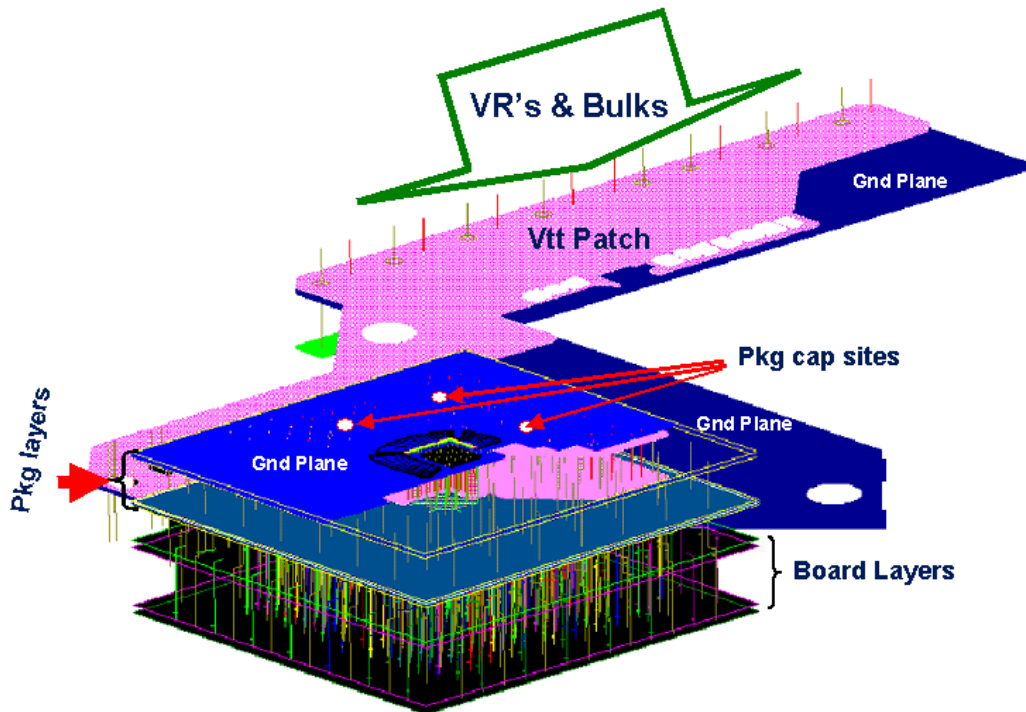


Figure 4a 3D view of SPEED2000 models illustrating capacitor sites and plane cutout.

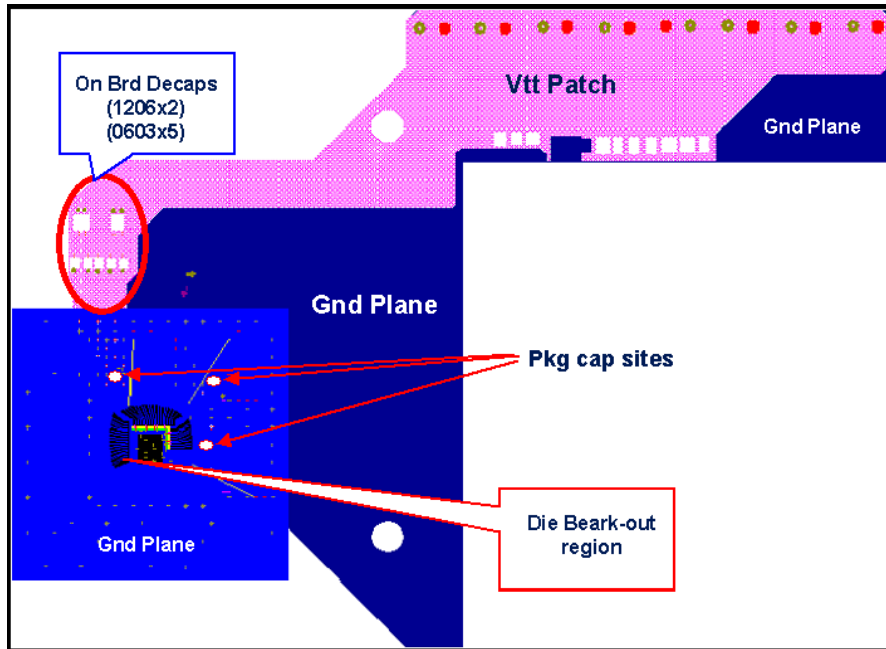


Figure 4b 2D view of SPEED2000 models illustrating capacitor sites and plane cutout.

The on-die capacitors and driver/receiver buffer models, in the form of IBIS, are included as sub circuits in SPEED2000 as well. Figure 5 shows the resultant power delivery network impedance vs. frequency, for the optimal design described in the previous section. This result is generated from time-domain simulations through Fourier transform. As can be observed in Figure 5, the $Z(f)$ designed met the requirements defined by the specification at all frequencies except for a resonance peak at 71MHz. However, there is a +/-5% AC TOL budget for any mismatch, which will be validated in the time domain simulations to show the design still meeting the voltage TOL requirements.

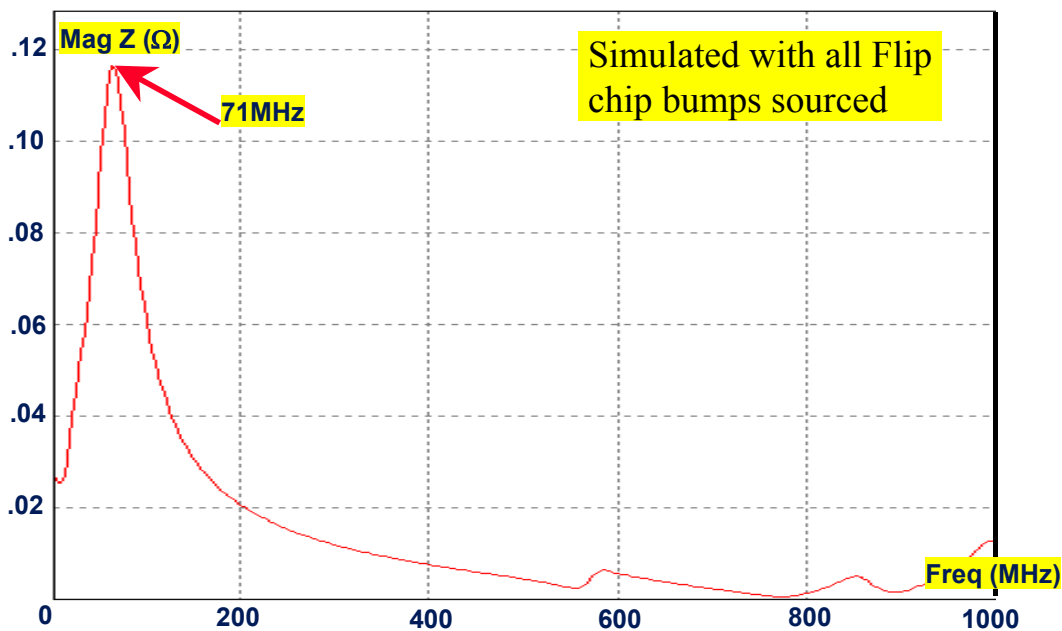


Figure 5 SPEED2000 simulation results for power delivery network impedance profile.

Time domain simulations showing signal quality and VTT noise are shown in Figure 6. Due to simulation time constraints, only 32 bit address and 16 data signals are switching in this simulation. In a realistic worst case situation, another 16 data signals could be switching at the same time, making the voltage noise $\sim 1.25x$ worse compared to the voltage noise shown in Figure 6, which still meets the voltage noise specification. The switching rate used in Figure 6 are for the highest data switching frequency, which is 200MHz base frequency with double pump resulting in 400MTS data rate, and also for 71MHz base frequency double pump resulting in 142MTS data rate, where a resonance peak occurs in the power delivery network of Figure 5. As can be seen in Figure 6, the case where the switching rate coincides with a power delivery network resonance peak resulted in the higher noise on the power supply. This demonstrates the importance to design to the design specification, and controlling all resonance peaks in the power delivery network for noise reduction. Since the interest is on the power delivery robustness, the crosstalk noise from trace coupling was not included in this model.

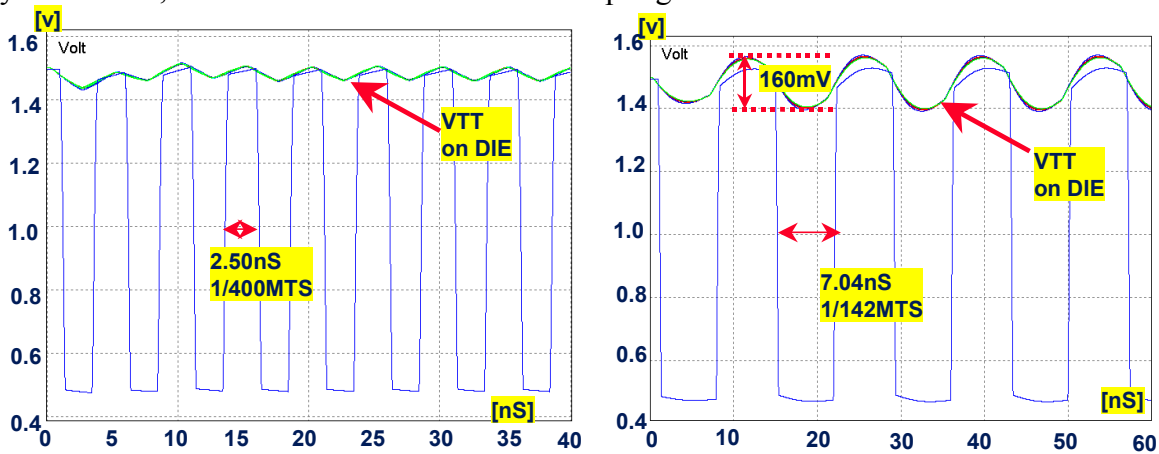


Figure 6 Signals waveforms and Vtt noise for MCH driving at the highest bus frequency and worst-case bus frequency

Validation

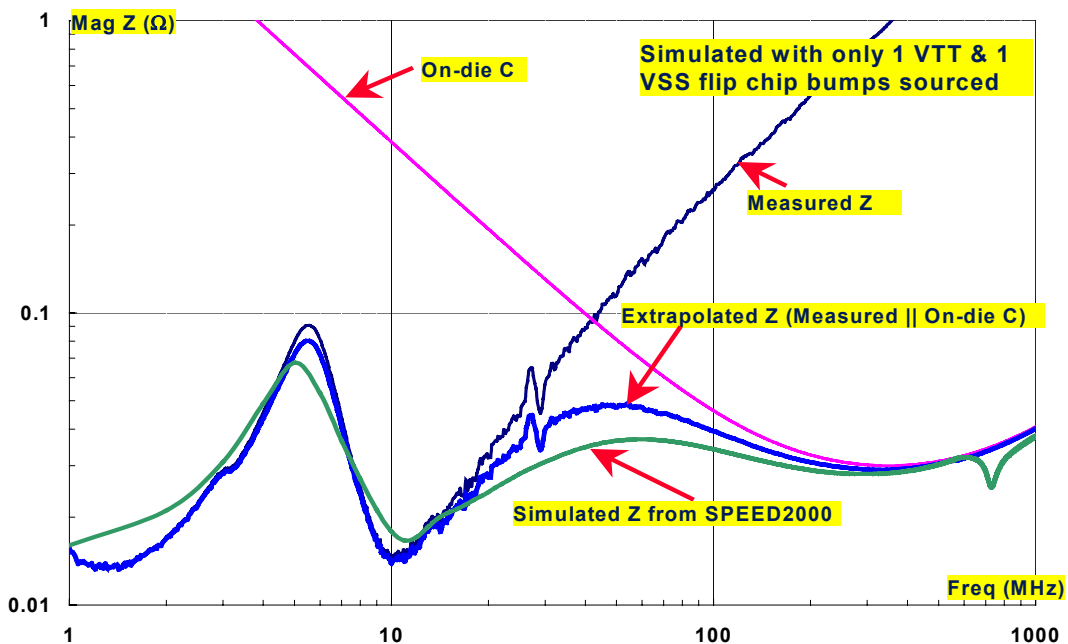


Figure 7 Z vs. Frequency correlation results – with all package capacitors.

An Agilent 4291B impedance analyzer is used to measure the power delivery network impedance for frequency range of 1MHz to 1GHz, after Short, Open and Load calibration is performed. The measurements are done at the package flip chip bumps. The MCH package with the package capacitors was attached to the motherboard in this measurement. The MCH die was not mounted however on the package in this measurement to allow access to the bumps. The rest of the decoupling capacitors on the motherboard are also mounted.

Since this measurement setup can only measure at one VTT and one VSS bumps, its $Z(f)$ characteristic will be different when compared to Figure 5, where all the flip chip bumps are sourced equivalently. For correlation with measurements, the simulation models are modified to reflect the measurement setup and the addition of on-die capacitance in parallel with the measurement result is included and called "Extrapolated Z". The results are shown in Figure 7. Figure 7 demonstrates good correlation between the measured and the predicted $Z(f)$ and confirmed the robust power delivery network design, satisfying the $Z(f)$ design target required.

Conclusion

This paper has demonstrated an approach to achieve high speed IO performance with optimal package size. Validation results in frequency domain have shown good correlation with the predicted results. Further correlation results and discussion will be shown during the conference presentation.

Acknowledgements

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