

PDN Optimization for Laptop and Desktop Computer Platforms

Minglei Wang
Intel Corp.

Jinsong Hu
Sigrity Corp.
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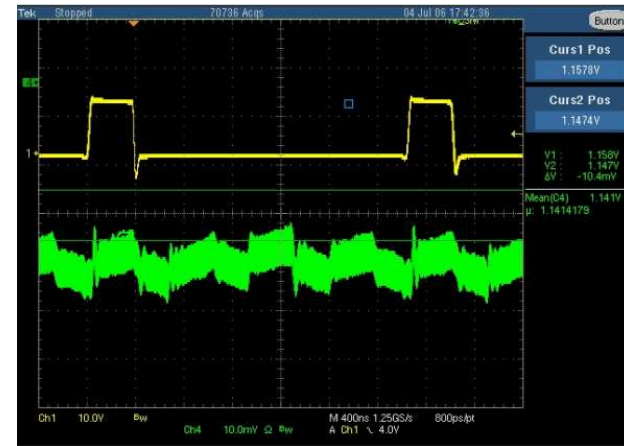
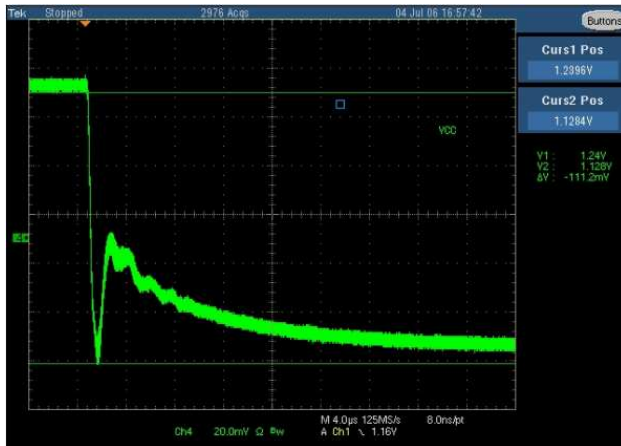
Content

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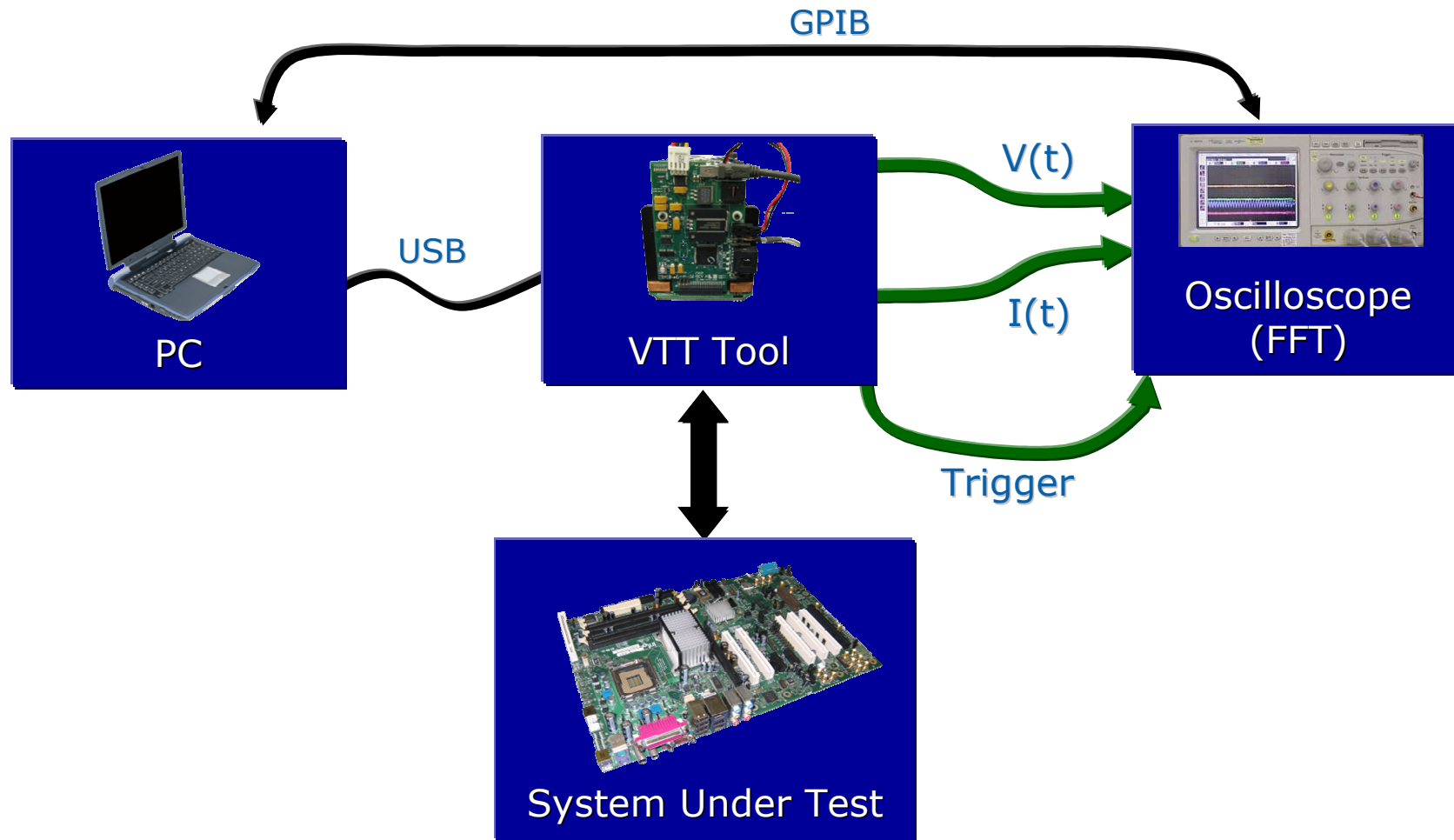


Traditional decaps optimization

Try to optimize decap placement by experience, and then do the **time domain** or frequency domain validation cycling.



Time Domain Measurement Topology



Summary for traditional decaps optimization method

- Need experienced power engineer, otherwise they can NOT adjust decap types, values and placement wisely;
- Time consuming for the try-validation cycling, if the modified design does NOT pass the power spec, the designers must turn back to adjust decaps again and again;
- Overall, the decap optimization efficiency for the traditional flow highly depends on experience, and it is VERY hard to find an optimal scheme to satisfy both performance and cost.



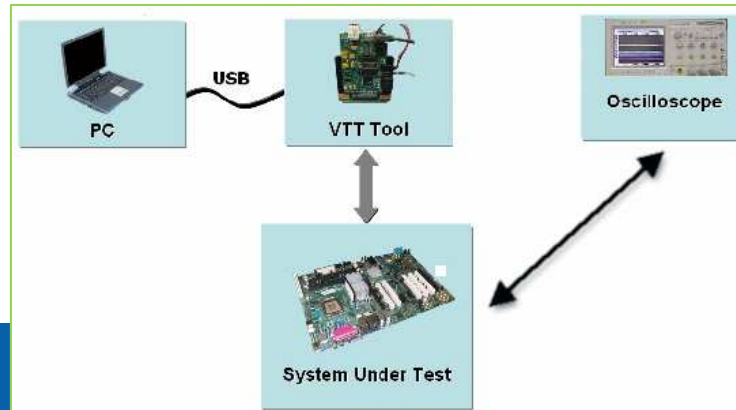
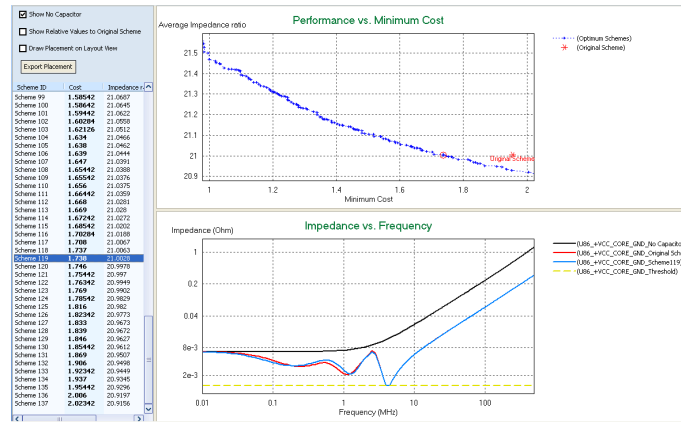
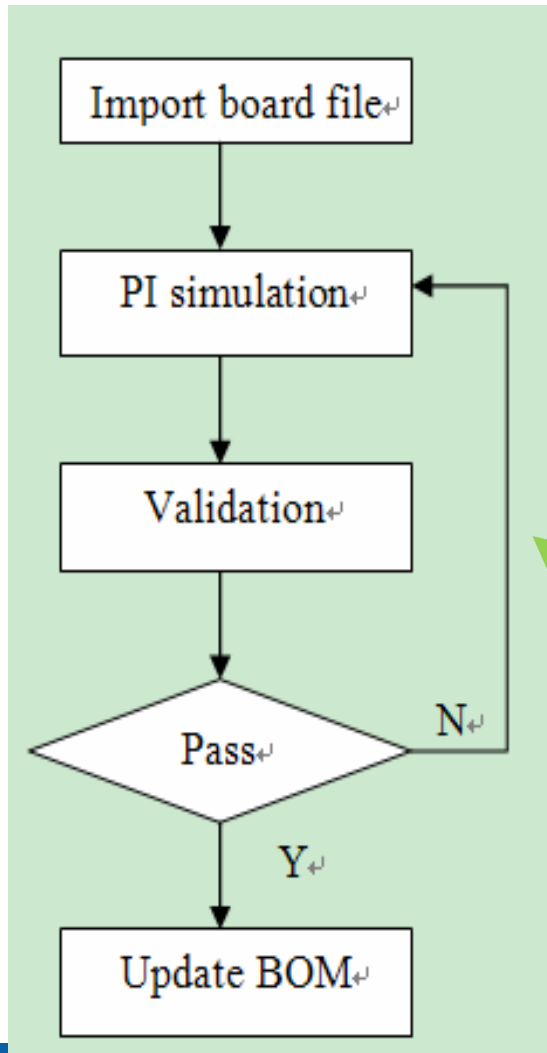
EDA tool based decaps optimization

OptimizePI ...

- A very useful solution to optimize power delivery system design
- Automates the placement and selection of decoupling capacitors (decaps)
- Improves both performance and cost of the interested Power Delivery Network (PDN)
- Task-focused flow, very easy-to-use setting environment



EDA Optimization Flow



Validate the NEW decaps optimization flow

- **We used this OptimizePI tool both on our Laptop and Desktop platform...**



Case1: Laptop Platform Optimization

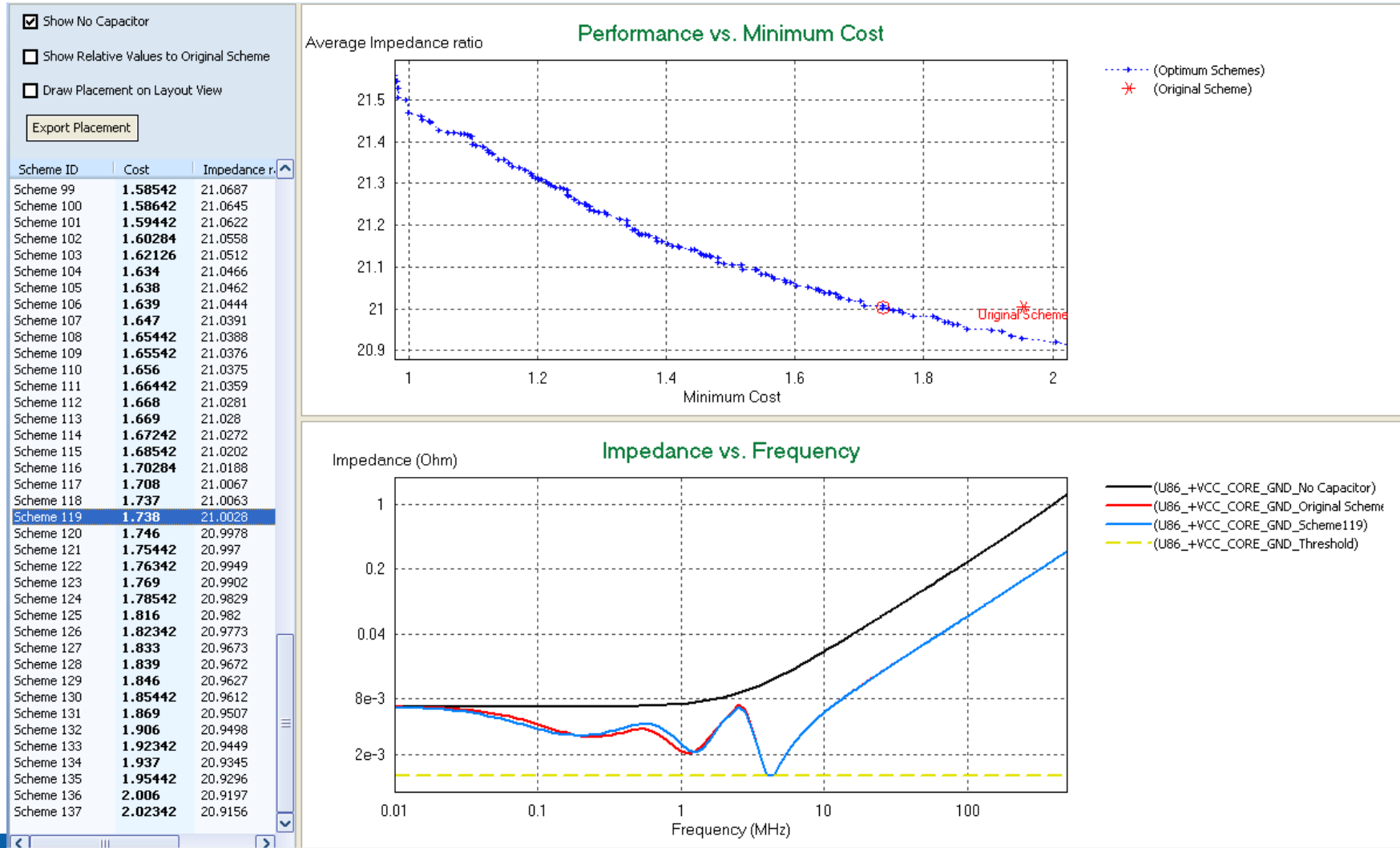


CPU Power Rail optimization

- Current design constraints for Laptop platform: thin and light, design space very limited, hard to place decaps, harder to optimize;
- Above is the input impedance observation for the CPU power rail (VCC_CORE/GND rail)



Optimization result for CPU power



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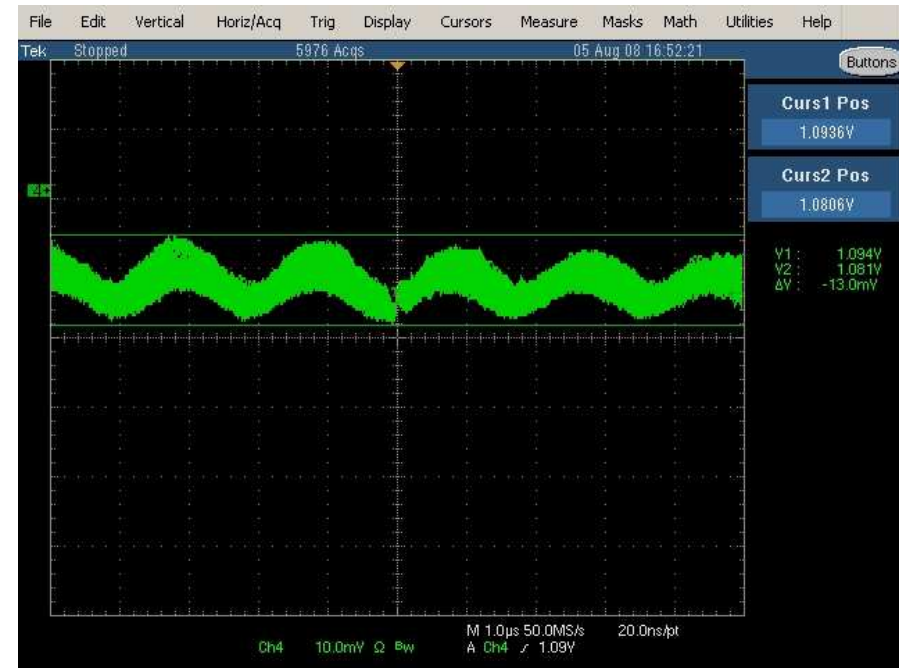


Measured power ripple at CPU

Before OPI



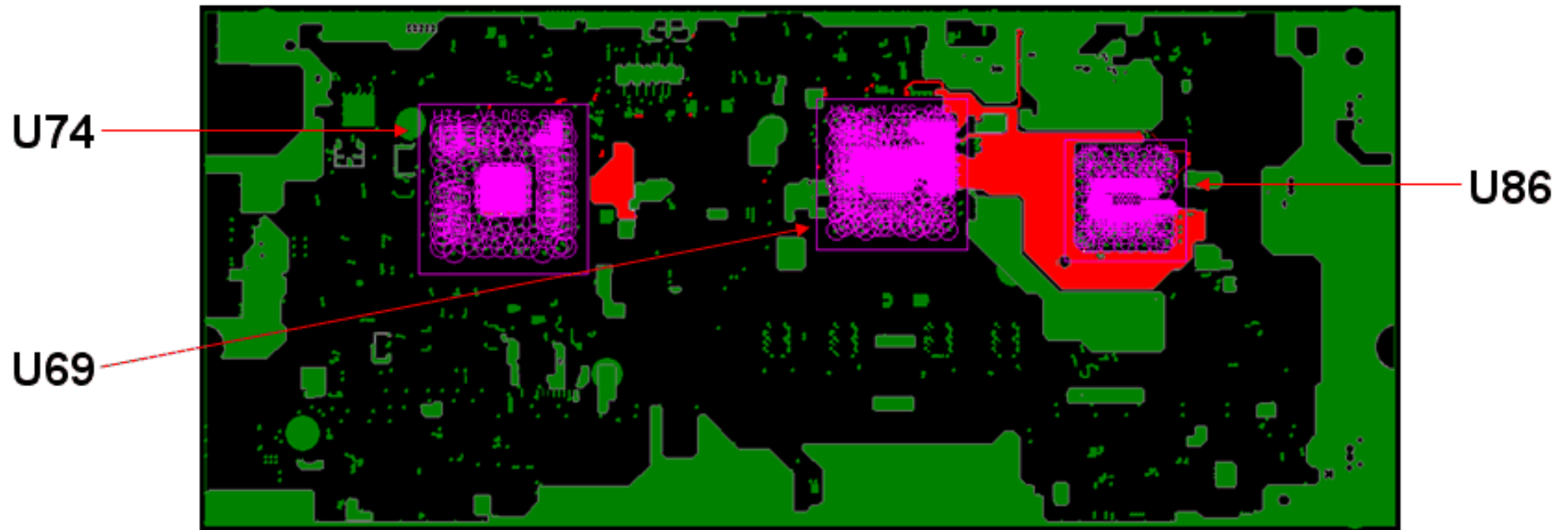
After OPI



Power Rail	cost down	Noise before optimization	Noise after optimization
CPU Power	11.1% (0.21\$)	9.8mv (Spec:20mV)	13mv



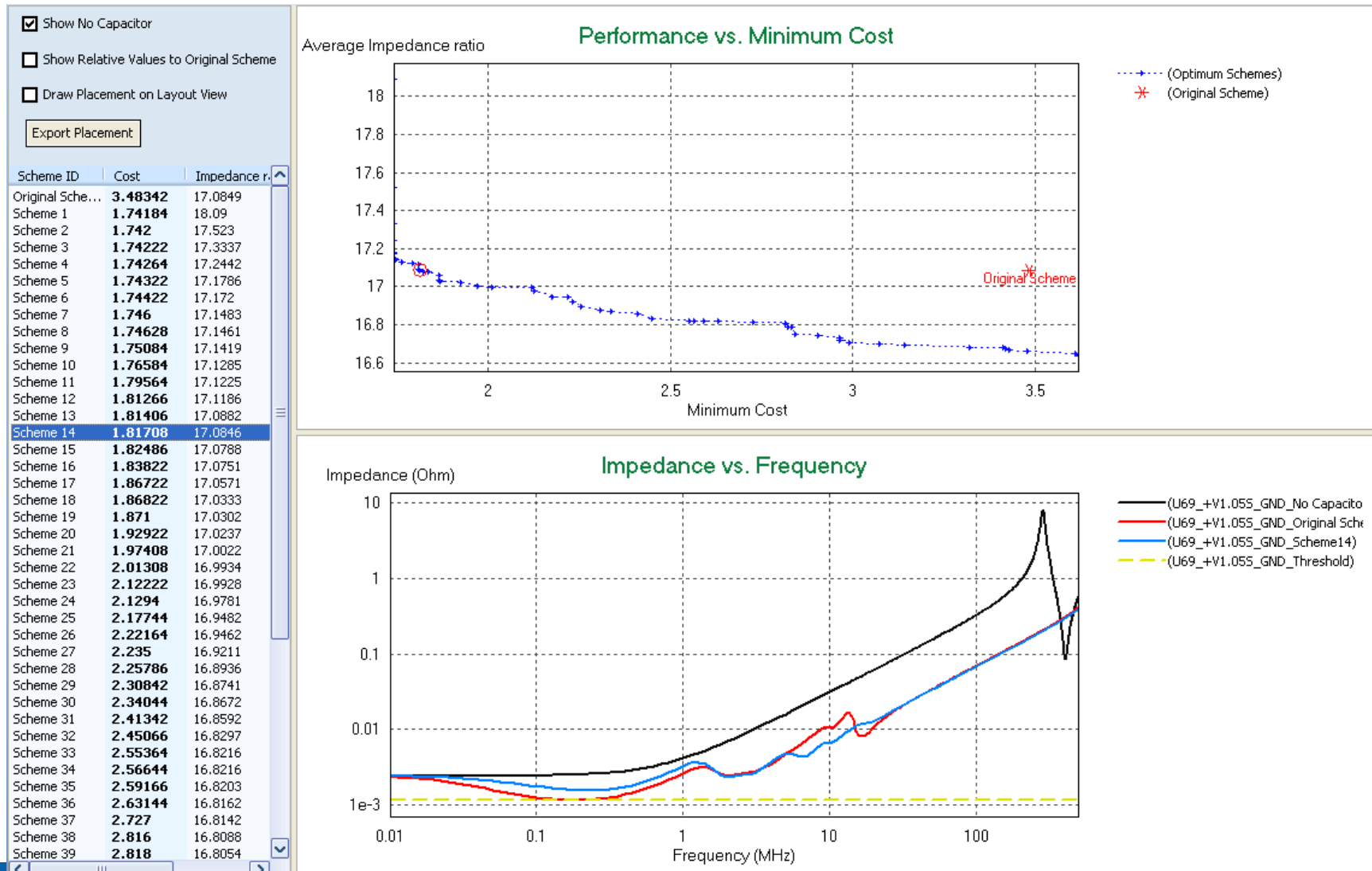
Decaps optimization for Chipset Power rail



U69 MCH, U74 ICH and U86 CPU



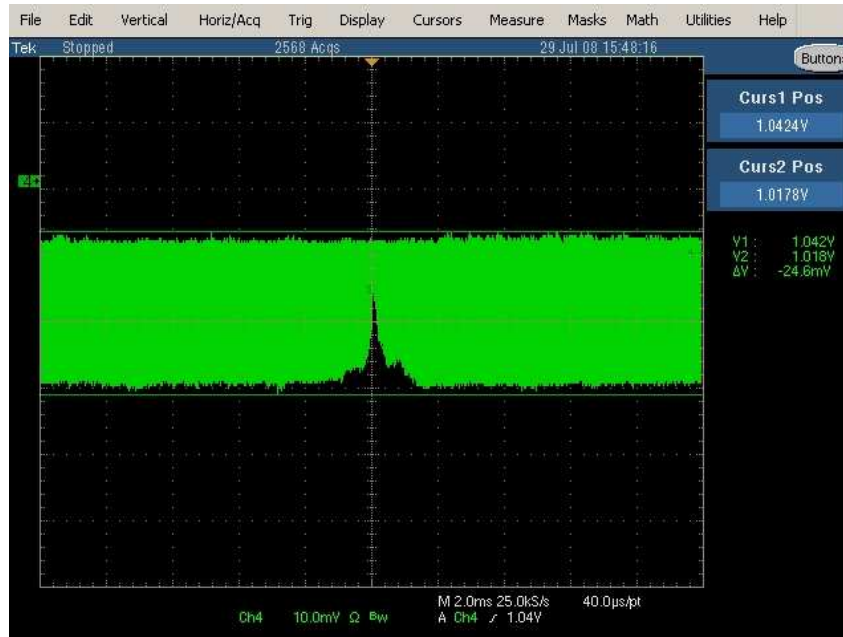
Optimization result for Chipset power



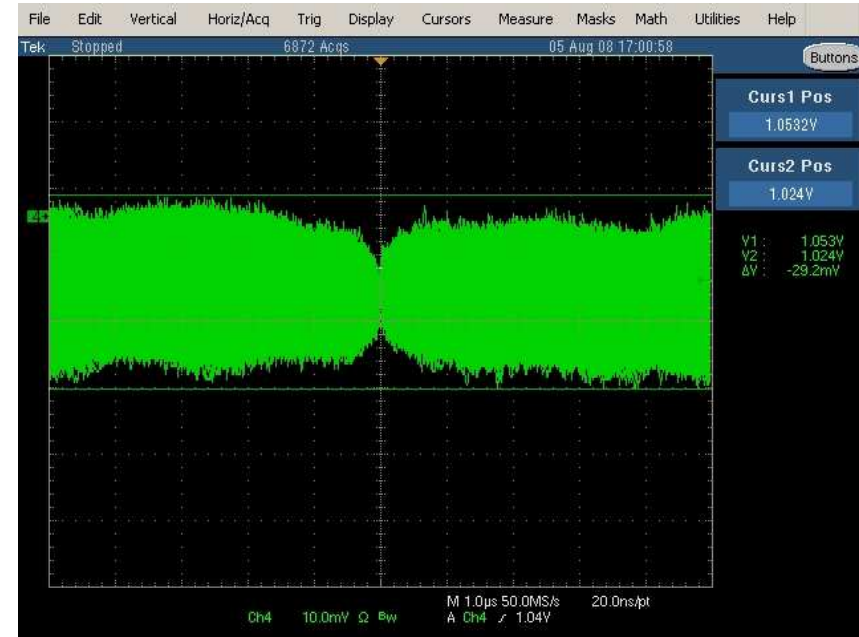
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Measured power noise at MCH U69

Before OPI



After OPI



Power Rail	cost down	Noise before optimization	Noise after optimization
MCH Power	47.8%	35.4mv (Spec:50mV)	29.2mv



Measured power noise at ICH U74

Before OPI



After OPI

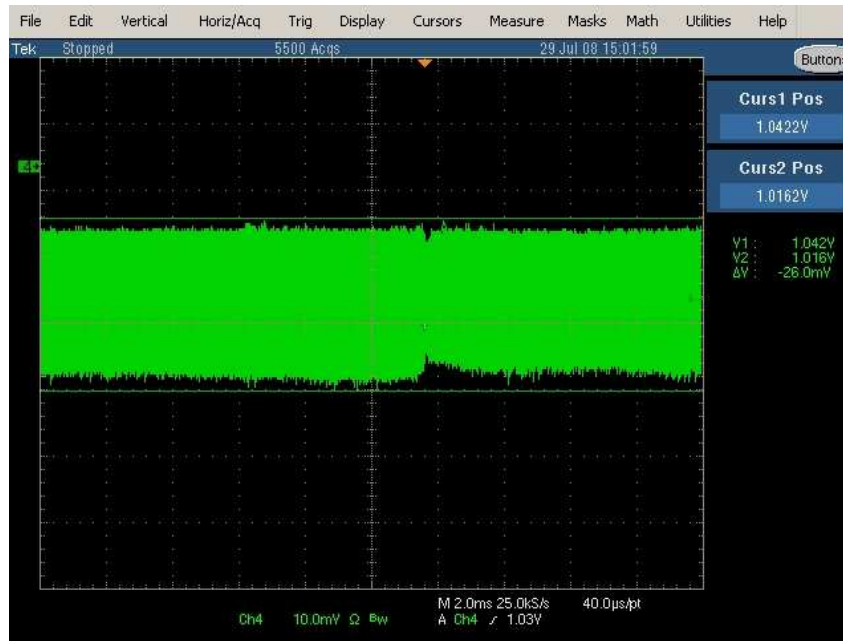


Power Rail	cost down	Noise before optimization	Noise after optimization
ICH Power	47.8%	31mv (Spec:50mV)	36mv

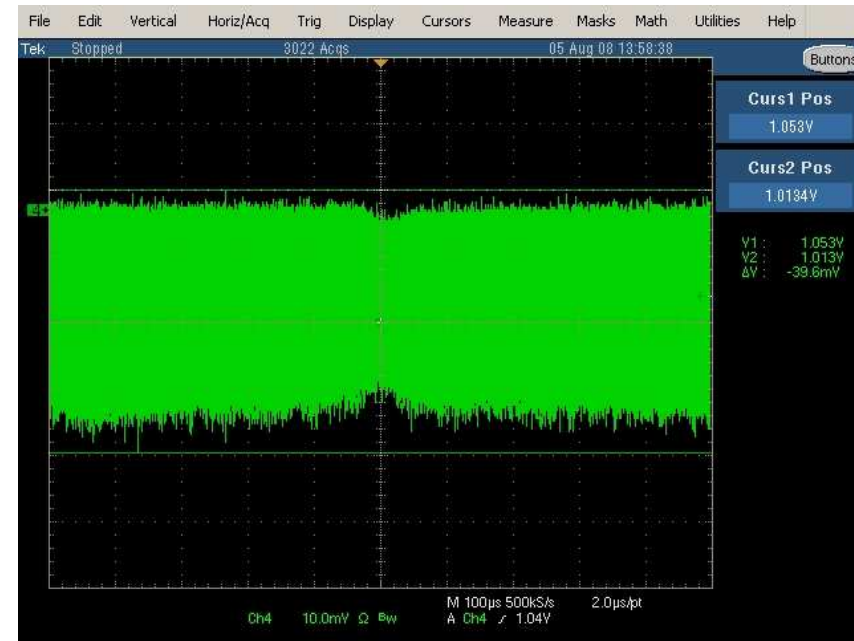


Measured power noise at CPU U86

Before OPI



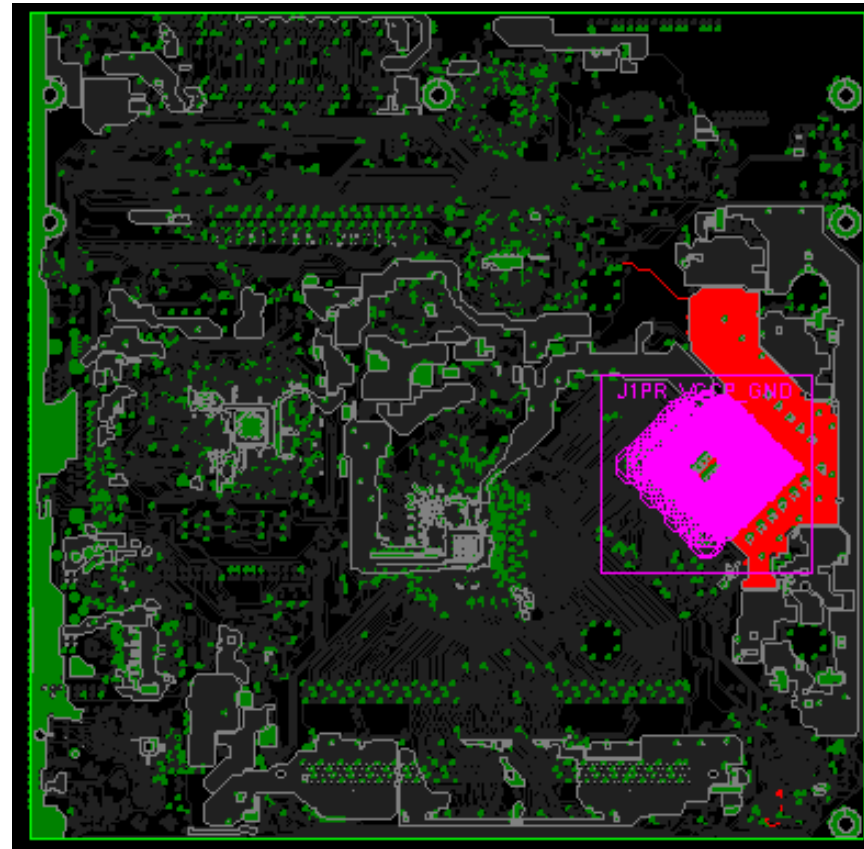
After OPI



Power Rail	cost down	Noise before optimization	Noise after optimization
CPU Power	47.8%	26mv (Spec:50mV)	39.6mv



Case2: Desktop Platform Optimization

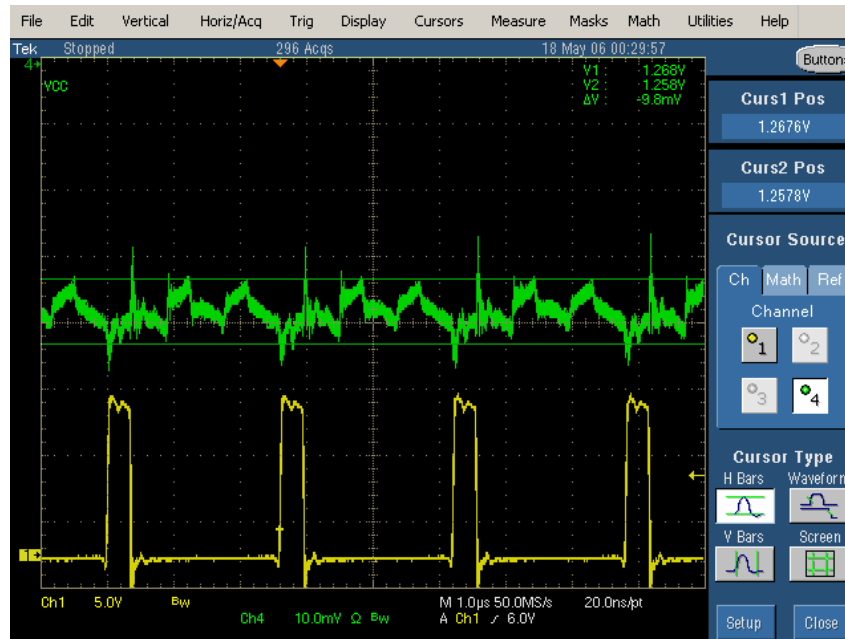


- Current design constraints for Desktop platform: high current, high load step and high voltage fluctuation, hard to place and optimize decaps;
- Above is the input impedance observation for the CPU power rail (VCCP/GND rail)



Measured VCCP noise at CPU J1PR

Before OPI



After OPI



Power Rail	cost down	Noise before optimization	Noise after optimization
CPU Power	14.2%	9.8mv(spec: 15mv)	9.6mv



Decap placement table generated by OptimizePI for VCCP/GND

Before Optimization

* Refdes	Decap Placement Part No.	ID
C21TH	CAP_402-0_1UF_20%_16V_402_E_0_1UF	2
C63VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C64VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C65VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C66VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C67VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C68VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C69VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C70VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C72VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C73VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C75VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C76VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C78VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C80VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3

After Optimization

* Refdes	Decap Placement Part No.	ID
C21TH	---	---
C63VR	---	---
C64VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C65VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C66VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C67VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C68VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C69VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C70VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C72VR	---	---
C73VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C75VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C76VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C78VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C80VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3

➤ Rework list can be adjusted accord to the above placement table.



Cost and Performance optimization summary

MIMOS (Laptop Platform)			
Power Rail	Decoupling capacitors cost down	Noise level before optimization	Noise Level After optimization
CPU Power	11.1% (0.21\$)	9.8mv	13mv
Core Power(1.05V)	47.8% (1.66\$)	35.4mv(MCH) 31mv(ICH) 26mv(CPU)	29.2mv(MCH) 36mv(ICH) 39.6mv(CPU)
TOSTON (Desktop Platform)			
Power Rail	Decoupling capacitors cost down	Noise level before optimization	Noise Level After optimization
CPU Power	14.2%	9.8mv	9.6mv



Summary

- Reviewed the drawbacks of the traditional ways: time consuming, over-design, experience based, hard to find trade-off between cost and performance
- A new EDA based method (OptimizePI) was employed to validate the decap optimization, the final result showed significant cost-down while maintaining acceptable power performance.



Q&A

