

DesignCon 2010

Simulation and Measurement of an On-Die Power-Gated Power Delivery System

Jimmy Huang, Intel
[jimmy.huat.since.huang@intel.com, (+604)-2532385]

Tan Fern Nee, Intel
[fern.nee.tan@intel.com, (+604)-2531518]

Yong Lee Kee, Intel
[lee.kee.yong@intel.com, (+604)-2533543]

Pang Sze Geat, Intel
[sze.geat.pang@intel.com, (+604)-2538004]

Ooi Poey Ling, Intel
[poey.ling.ooi@intel.com, (+604)-6145532]

Jess Kiu, Intel

[jess.cheng.sing.kiu@intel.com, (+604)-2534373]

Abstract

For low-power design, power switch gate is introduced to the SOC to reduce the leakage current from the un-used IP block during power-saving mode. However, it introduces additional IR loss and reduces the voltage margin. It also induces huge current spike and pulls down the on-package voltage to almost zero during the switch gate turn-on transition to charge up the on-die decap. This paper demonstrates the full-path simulation and lab measurement to characterize the gated PDN behavior. Mitigation solution for the tight DC margin and on-package sudden voltage droop is provided. Good correlation between silicon and measurement is shown.

Author's Biography

Jimmy Huang is a Senior Power Integrity Engineer at Penang Design Center, Intel. He has been with Intel for 6 years working on power delivery system for microprocessor and chipset. His focus area is component level power delivery design and package electrical.

Tan Fern Nee is Power Delivery Technical Lead for Intel Penang Design Center, Malaysia. She has 12 years of experience in package and board electrical analysis experience, ranging from Signal integrity, power delivery, electromagnetic and RF board design. She is part of the electrical analyst team for tester-interface unit, burn-in boards and now PC / mobile platforms. She obtained her Bsc (Hons) Degree of EE at University of Leeds.

Yong (Ricky) Lee Kee is Design Technical Manager for Intel Malaysia. He is part of the design team for several PC platforms starting Pentium IV, Core2, Atom, and latest i7-Nahalem. Prior to Intel, he is a CAD design engineer for Analog Device Inc based in NC USA. He obtained his MSc of EE at University of Tennessee while working at Microsystems Prototyping Laboratory which is housed within the ECE Department for University of Tennessee, funded by Jet Propulsion Laboratory (JPL) of NASA. He obtained BSc in Computer Engineering from Mississippi State University.

Sze Geat Pang obtained his bachelor degree in EE from Tun Hussein Onn Technology University (UTHM), Malaysia. He has been with Intel for three years engaging in the design of silicon, package, and board aspects of power delivery. He optimizes power delivery design within tight cost constraints and develops methodologies enabling more thorough scrutiny and fine tuning of the design.

Jess Kiu obtained his bachelors degree in electronics at Sheffield Hallam University. He joined Intel as a fresh graduate and had since been working as a back-end design engineer for 4 years. He had also been doing IR drop DC Static simulation for the past 3 years on multiple chipset projects.

Ooi Poey Ling obtained her bachelor degree in EE from Multimedia University, Malaysia. She has been with Intel for 6 years working in analog circuit design for chipset.

Introduction

Power integrity has always been a critical problem for ASIC, FPGA, full-chip custom designers and other designers alike. Voltage drop occurs as the current runs through the resistive and inductive components such as package pins, copper traces, on-die power gates (used to save power) and the metal layers on the die itself. While the supply voltage may meet the specified requirements at the package pins, the planning and design of the power grid on the chip must ensure that the power specification is met inside the die itself.

With more and more IPs and transistor blocks integrated into a single SOC chip, the full-chip power integrity analysis is getting more complicated than ever before. With the huge range of noise tolerance, impedance target and individual unique package plane shape, every Power Delivery Network (PDN) is custom-designed. For low-power design, power switch gate is introduced to the SOC to reduce the leakage current from the un-used IP block during power-saving mode. However, the resistive path between the drain and source of the power switch gate itself can introduce additional IR loss and reduce the DC voltage margin. The complexity adds on as these power gated PDN domains may share the same voltage regulator module (VRM) from the PCB motherboard. The mutual coupling noise occurs when the power integrity voltage noise propagates through the PDN structure from one end to another end. The power gates are embedded across the chip as well. It definitely is not an easy task to solve this complicated SOC product. As engineers tackle complex, larger PDN count designs, there is a need for innovative approaches to power integrity analysis that can predict and verify the power gated PDN characteristic with reasonable computing resources, but without compromising accuracy. With accurate and robust analysis, the gated power floor plane, IR drop budgeting, power-up-down sequences, de-coupling capacitor count and placement can be determined in the early phase to avoid over-conservative design and higher product cost. This paper aims to demonstrate a robust and accurate full-path power integrity analysis to the power switch gate PDN covering both static DC IR drop and dynamic power gate behavior.

Background

Conventional techniques of reducing the design's dynamic/switching power by clock gating unused clock trees does not reduce power enough to compensate the high leakage current that is inherent by deeper sub-micron technology. Hence, for extended battery life and to mitigate higher power consumption, introduction of power gating techniques, in which Vcc supplies for selected areas of the circuit will be cut off by switches or sleep transistors to reduce the leakage has becoming a norm.

Power well/domain isolation by using different supply networks for each power and/or ground domain is a common practice in low power designs since it provides the flexibility to control each domain independently. This is especially necessary in order to control standby off-state current for which individual domains can then be powered down. One approach is to use MOSFET devices to form a switch between an external and internal power network. For mobile computing applications, the power signature is highly dependent of usage model. When a particular feature is not needed, the associated functional blocks can be powered off. This can be achieved by turning off the devices controlling the internal power networks for these blocks; one can disconnect the internal

power network from its connection to the battery and hence minimize the standby mode leakage current. The ground network is still shared across the die. The design and performance penalty include the additional silicon real estate and the time taken to power up/down and subsequently activate one or more blocks.

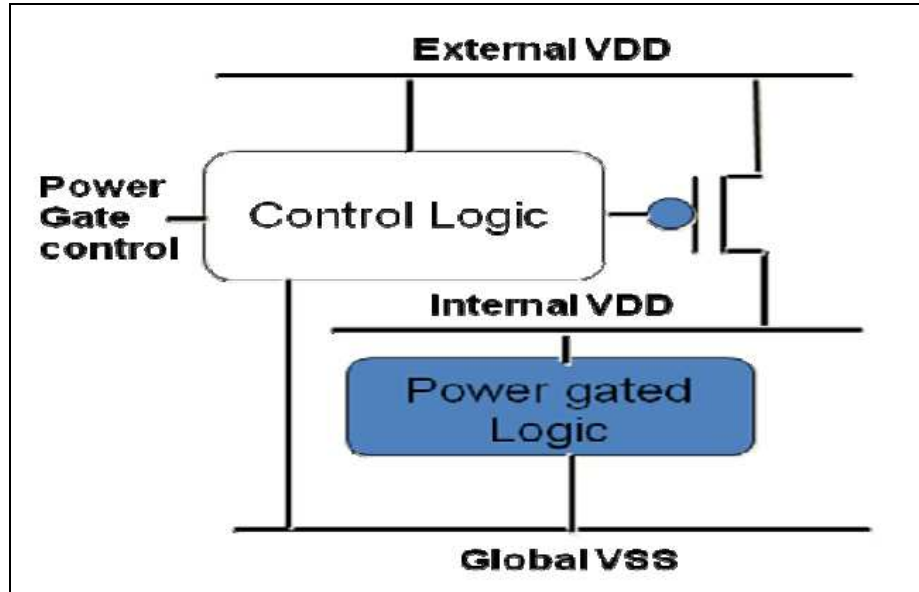


Fig. 1. Power Gate PFET between gated logic and power supply

The distributed power gating methodology used (shown in figure 1) is a header cell (PFET) where the source is connected to the external power network which is then connected to the battery through the C4 bumps, package and PCB traces. The drain is connected to the internal VCCg (“g” indicates gated) network. A power enable signal routed from the PMC (Power Management Controller) controls the gate through some dedicated logic.

Full Path IR Drop Analysis

For gate level timing and circuit SPICE simulation, the minimum DC voltage is used to simulate the worst-case V_{min} condition. Therefore, delivering reliable power to the transistor gate level is always critical because failure in doing this will expose the functional logic to the unknown ambiguous voltage level states.

DC IR drop can happen in a chip, package, PCB motherboard and VRM tolerance. On-die resistance refers to the several metal layer power grids in either x or y axis, and via that connect from one metal layer to another metal layer, and the resistance between Drain-Source (R_{ds}) of the P-MOSFET power switch gate (PFET). On-package IR drop includes C4 bumps, copper plane, via and solder ball connecting the die to the PCB.

Much attention has been given to on-chip power loss caused by the micron size ultra-small device, but the package-board level IR drop can also have significant contribution to the total power loss, which sometimes gets unnoticed. It gets more complicated when the small package itself has multiple power nets (>50) with complex and irregular shapes.

This huge number of power nets may cause power plane cut, necking, insufficient via and imbalanced current path. It is a challenging to ensure that every C4 bump is well supplied in this complicated design situation.

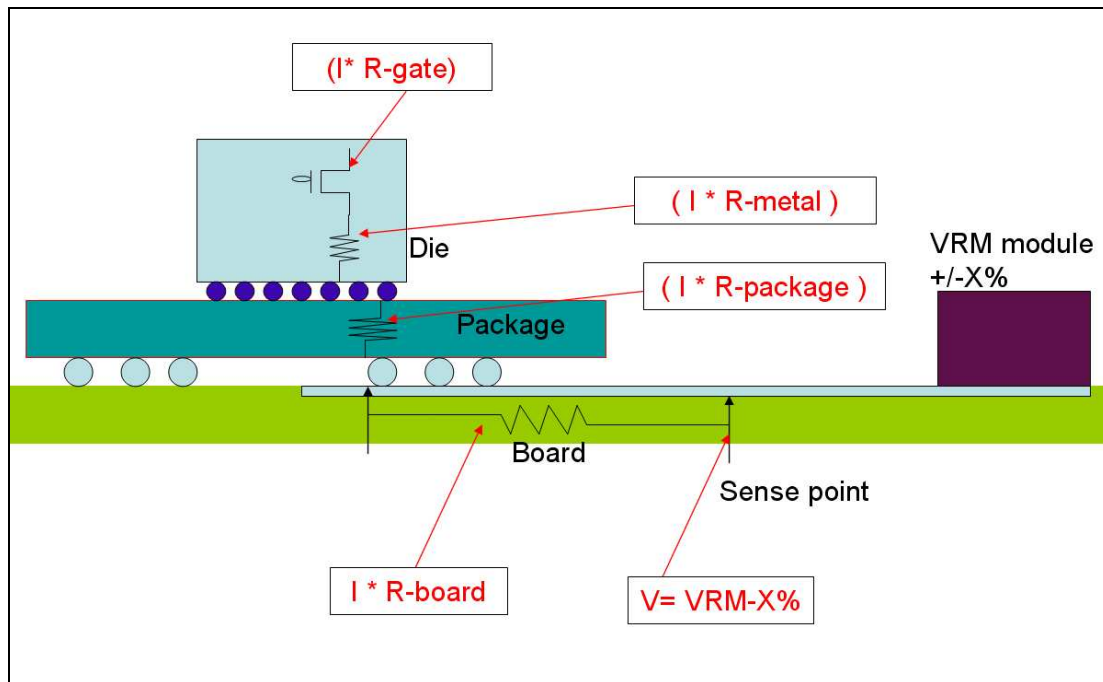


Fig. 2. System-level Power Loss Budget for the power gated PDN

Figure 2 demonstrates the system-level PDN power loss. The VRM regulates and maintains its voltage level to certain tolerance at the sense point location. Every component, such as package, power switches and metal grid, is given certain design budget. The IR drop must fall within the required budget window. In most cases, the package budget is usually less than 1%.

Commercial Package/PCB IR drop simulator is used for the package-board level IR drop simulation. The tool is chosen because it can handle multiple power domains from a large PCB board to every single package C4 bump, as well as has very fast run time without compromising the accuracy. The colorful visualization voltage and current density maps are also very useful because it leads the designer to the current path bottle-neck problem. This enables rapid what-if assessment for the best design tuning.

Figure 3 shows the distribution graph of C4 bump DC level voltage of a package before and after the layout improvement. Package B is before the fix while Package A is after the fix. The Package A's average IR DC voltage is 1.0485V, which is 1.5mV higher than Package B. Package B also has 3X larger standard deviation than Package A. Figure 4 shows the voltage distribution of Package B. The region circled in white is the bottle-neck where those C4 bumps suffering DC voltage below 1.044V. It is always desired to have smaller DC voltage variation across the die because different voltage level at certain logic cell will give different PVT conditions which could complicate the gate logic timing

analysis. The analysis flow shows a significant DC improvement with package layout fix.

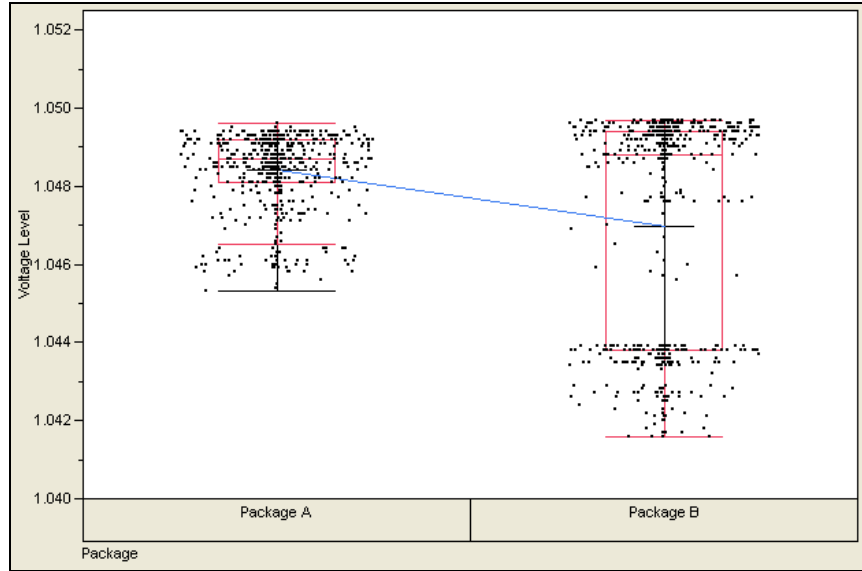


Fig. 3. C4 bumps DC voltage distribution between Package A (after layout fix) and Package B (before layout fix) shows that the layout fix improves the DC margin

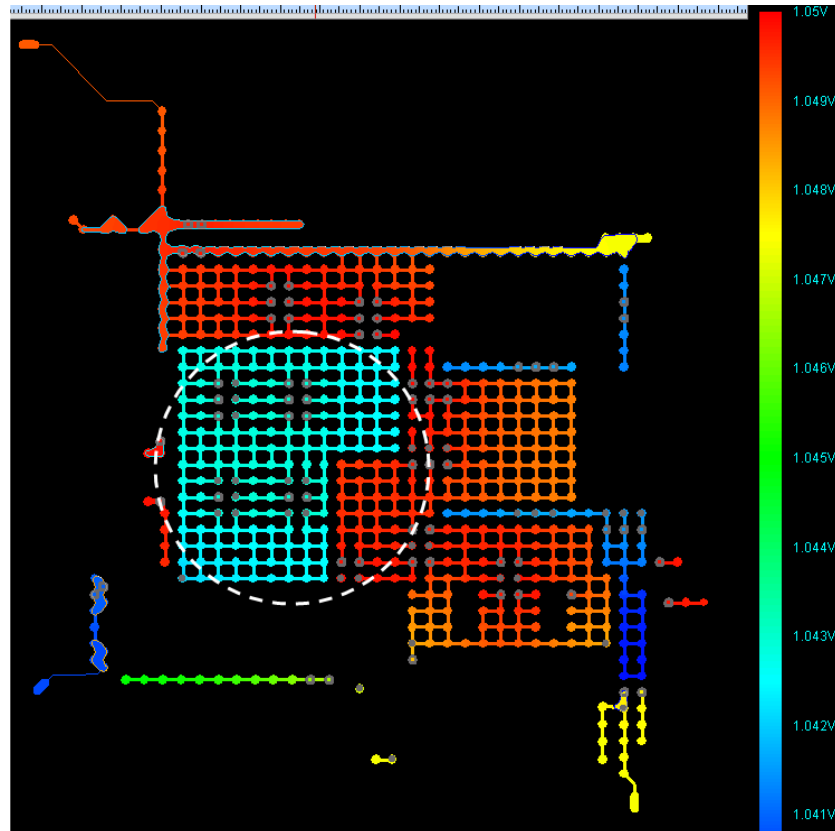


Fig. 4. Before the layout fix, the 2D voltage distribution power maps at C4 bumps shows larger IR drop variance at the circled area

Instantaneous Power Switch Gate Power-Up-Down Modeling and Simulation

In Figure 2, the on-die PFET is used to cut off the power delivery during the suspend mode to save the leakage power. The circuit suffers from both the power switch gate IR drop and instantaneous power-up-down voltage drop. Power-up sequence is emphasized in this section because it always represents one of the worst case current drawn. When the gated power domain is at the off state, its voltage level equals to ground and the on-die decap, which is contributed by the gated logic well die area capacitance, is not charged up yet. When the PFET is turned on, huge amount of current is drawn from the VRM to charge the logic cell up. This phenomenon is illustrated in figure 5 where a simulation test bench was setup to emulate thousands of transistors waking up at the same time, creating large in-rush current. The peak current is at the saturated stage and can be represented by equation:

$$i_{peak} = \frac{\mu_o}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \times PFET_count$$

The gated voltage can be represented by equation:

$$V_{gated} = \frac{1}{C_{gated}} \int_0^T i_{peak} dt$$

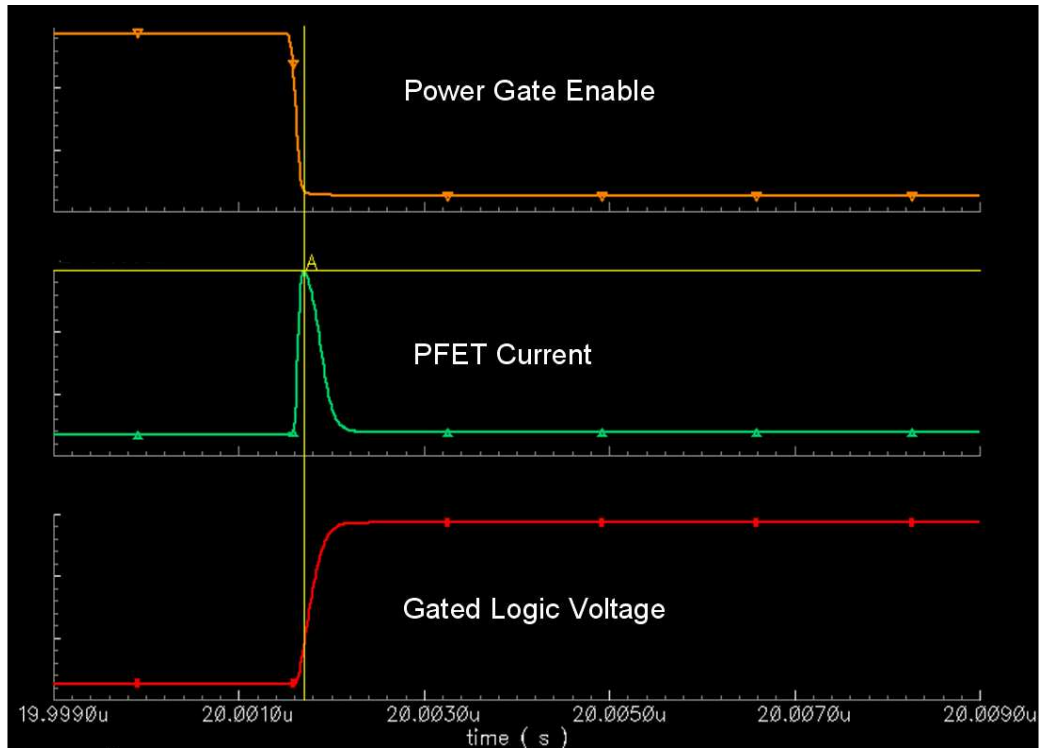


Fig. 5. The simulated PFET characterization without the PDN model

C_{gated} is the on-die decap which is contributed by the suspend logic die area capacitance. T is the decap charge up time. The charge time is hence directly proportional to the number of gates incorporated under the gated power supply.

To minimize the ON stage resistance overhead from the PFET, large amount of PFETs are inserted in parallel. Larger devices obviously allow more current and hence provide least resistance in the on-state of operation of the device. However, this increases the leakage current in the standby mode significantly. Another early design decision focuses on the physical implementation aspect of the placement of these power gates. One approach is to place multiple PFETs in parallel inside the functional blocks close to the associated bumps. Thus, the power switches can be embedded close to or beneath the VCC bumps and can be evenly spread in checker-box formation to have optimal current delivery and distribution over the entire partition [6].

Other considerations when designing ramp up topology include the following:

1. Switching or rush current: A sudden demand of current to charge the internal power network impacts both the battery and the system power delivery network design. The high di/dt associated with this current demand can induce a large Ldi/dt noise which can couple either to other power and ground networks.
2. Ramp up latency: Longer turn-on times from the standby to the operational mode reduce the peak of the rush current needed for the transition. However it can affect its ability to meet the specifications of the design. Also one needs to ensure that all devices reach a certain voltage level when transitioning to the operational mode.

To simulate such impact to the overall system, a close system simulation with accurate PDN extraction from board and package is required where using in-rush current as excitation. Although the rush current might reach to the saturated peak level but the characteristic of the PDN inductance (always responses against to the change of the dynamic current) limiting it from reaching that. Hence, the drawback of PFET implementation can cause very significant voltage droop coupling through the ungated supply rails.

Figure 6 illustrates the dynamic instantaneous power-up simulation setup. The PFET spice model is placed between the un-gated power domain and gated logic cell. The uncharged on-die decap is calculated based on the silicon die floor plan size area estimation. PDN (both PCB and Package) system is modeled using commercial Package/PCB 2.5D EM modeling tool. SPICE circuit simulator is used for instantaneous power-up sequence simulation. Although the early behavior modeling might not reflect the final circuit design, it helps in determining the PDN decoupling capacitor solution.

Figure 7 shows over 600mV simulated voltage droop at the C4 bump of the un-gated power rail. The logic cell blocks can only operate after the gated voltage has stabilized itself after certain oscillation cycles. In this simulation, the un-gated power domains shares the same VRM power supply with other logic cells, Always-Active Power Domain where no power gating is implemented. Although they are separated in the package but

they still share the coupling path through the motherboard PDN. Intuitively, large voltage droop can couple as voltage noise to Always-Active Power Domain through the capacitive and inductive component in the PDN. As a result, it can increase the chances of silicon failure such as setup/hold violation on critical timing paths and increase in clock cycle to cycle jitters.

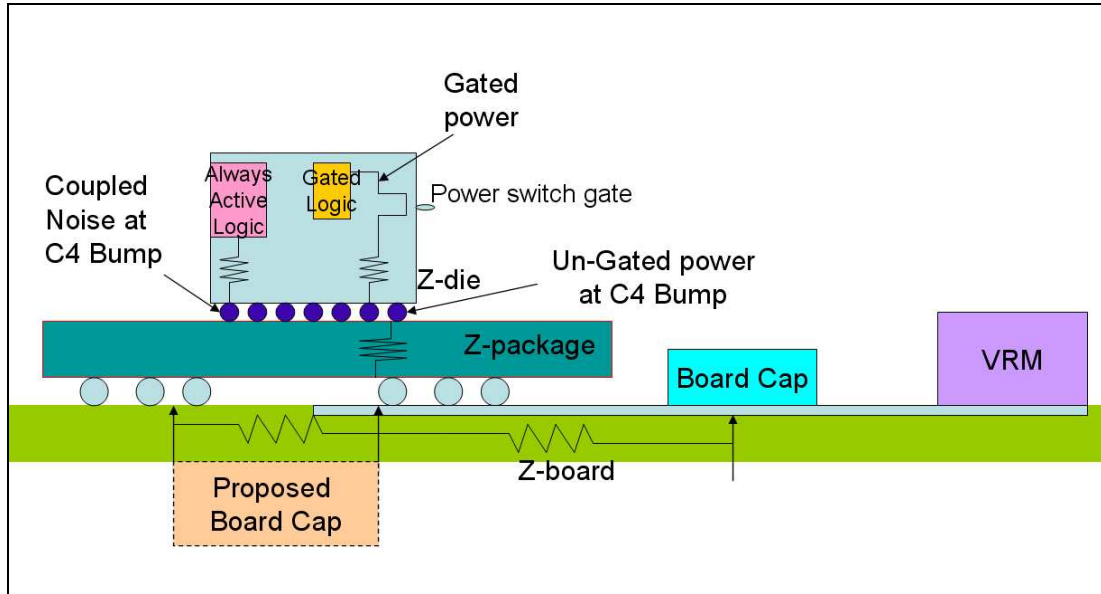


Fig. 6. Both Gated Power and Always-Active Power share the same power supply from the on board Voltage Regulator Module (VRM) and also the coupling path through the motherboard

In Figure 7, the un-gated voltage level is initially 1.05V. The gated logic cell is 0V and the intrinsic capacitance is not charged. When the PFET is enabled and V_{ds} equals to V_{cc} , the rush current shoots up and causes significant instantaneous voltage droop. The V_{ds} equals to voltage difference between V_{cc} and V_{gated} . When V_{gated} gradually increases, PFET current ramps subdue and eventually settle at the ON stage leakage level. Due to the PDN resonance, the voltage will oscillate due to the $-ve$ di/dt effects before it eventually settles down to $V_{cc} - IR_{Gated_Logic}$ level. The voltage noise simulated has seen been coupled over to Always-Active Power domain, for which it also exert an instantaneous droops from 1.05V to 0.87V. These dynamic voltage noises are not favorable since Always-Active logics will only be PV to a V_{CCmin} and V_{CCmax} to guarantee timing over worst case PVT variation, and in this case, it has indeed violated the logic minimal voltage condition. During power gating event where PFETs are turned OFF, similar voltage noise was also observed in simulation due to the power are cut and $+ve$ di/dt created when current from gated region ramp sharply from ON stage to OFF stage leakage [2, 7]. A large voltage overshoot of 500mV (1.55V) was observed which violated the V_{CCmax} condition. Large current spikes are also unfavorable where silicon reliability is a concern with electrical over stressed.

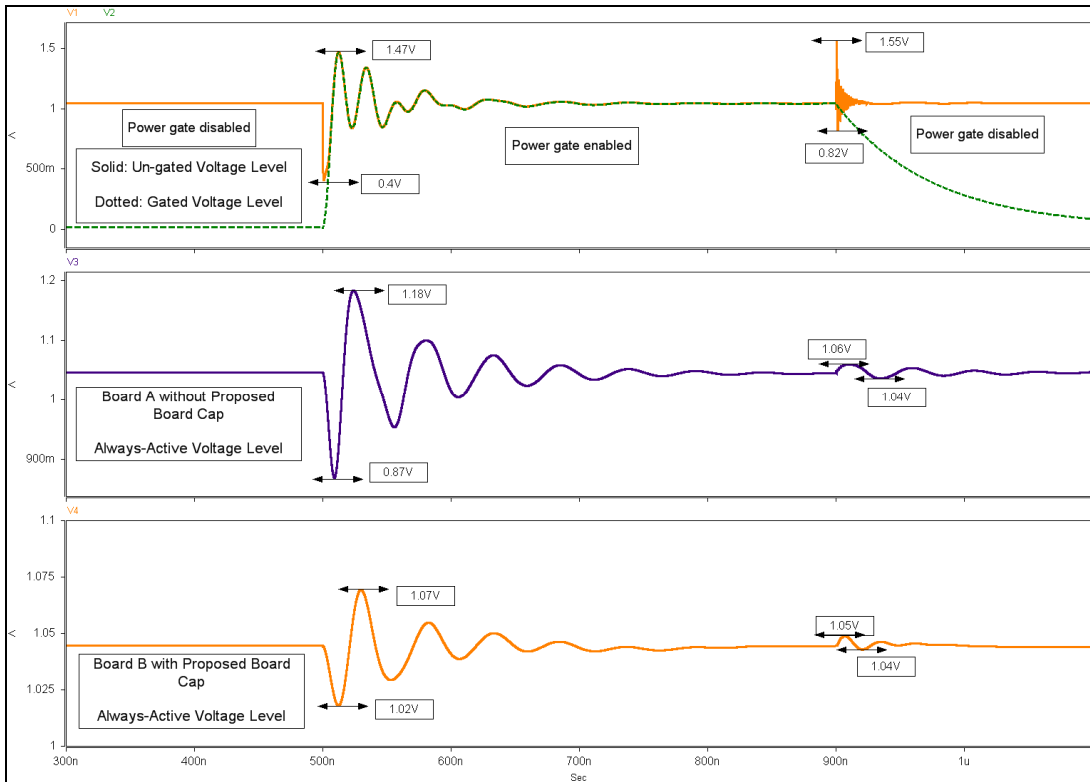


Fig. 7. The gated logic cell is initially in off state. The power gate is enabled at 500ns. Un-gated voltage drops down to 400mV and overshoots to 1.47V. The gated logic cell power is cut off at 900ns. The overshoot is 1.55V and the droop is 0.82V. For Board A without proposed board cap, 310mV coupling noise is observed at Always-Active power domain. For Board B with proposed board cap, the coupling noise at Always-Active power domain is reduced from 310mV to 50mV

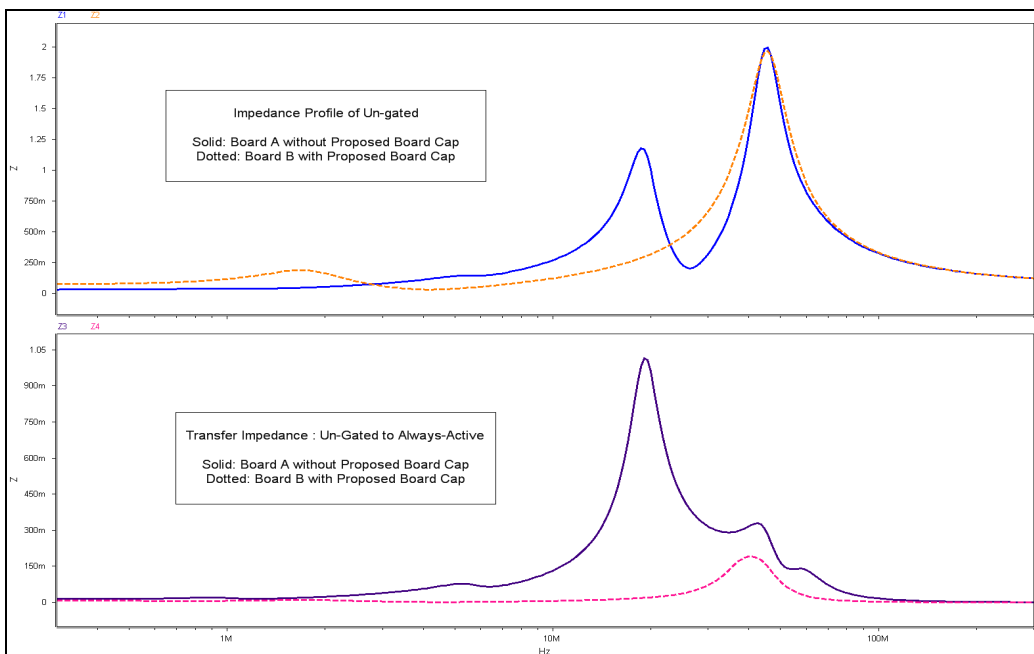


Fig. 8. Although the impedance peak of un-gated power domain does not change much, but the transfer impedance coupling noise to the Always-Active is reduced significantly

In order to resolve this voltage drop, the proposed board cap is recommended to be added on the back side of the board which is just underneath the package.

Figure 8 shows that the transfer impedance from the power switch gate to the Always-Active Power domain can be reduced by using the proposed board cap. In Figure 7, although it does not help much in reducing the un-gated voltage droop and overshoot, it improves the propagated coupling noise to the Always-Active Power domain significantly from 310mV to 50mV. Hence, it is recommended in this case.

Silicon Measurement

To further validate the pre-silicon results, the post-silicon voltage drop measurement has been conducted for correlation purpose. The chipset DUT (Device Under Test) is attached on the motherboard through the socket. The solder resist on package top side is removed to expose the package probe pads. They are placed very close to the silicon die to capture the C4 bump voltage waveform. Microwave probe sets are used to access the tiny package probe pads (~300um pitch) located near to C4 bump. High bandwidth scope is used to perform on-package active voltage noise measurements.

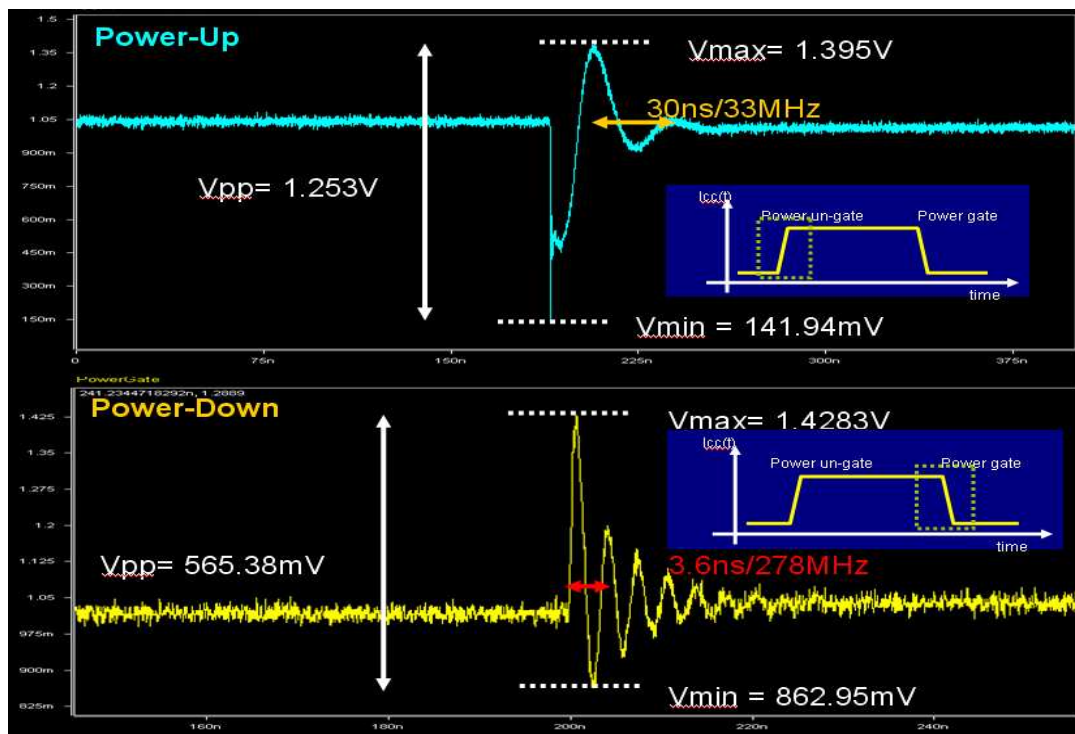


Fig. 9. The noise profile oscillation ringing is observed as 30ns period or 33MHz during Power-Up; and 3.6ns period or 278MHz during Power-Down. The change in the oscillation period is due to the difference of the gated logic capacitance at different power state.

Software to control the power gate is loaded to the target system through the debug card. When the power switch gate is enabled, both the Un-gated Power and Always-Active

Power voltage noise drop is probed simultaneously.

The power gate of all logic cells will diminish the on-die intrinsic capacitance with immediate effect. The sudden lost of on-die intrinsic capacitance on power gating domain will be a threat to the stability of the chip functionality especially to the functioning logics. The characterization of on-die intrinsic capacitance during power-up-down becomes extremely important to help predict an accurate power supply noise.

Figure 9 shows the power supply noise frequency is greatly shifted when a gated cell is power-up and power-down. During Power-Up, the voltage droop registers a 30ns droop period. This is translated to a 33MHz resonance. The power supply droop during the power-down has transformed to 3.6ns oscillation, or 278MHz resonance. This is explained by the diminishing effect of the gated cell intrinsic capacitance when the power goes off. The capacitance during power-up is observed at 6.6nF, while the capacitance has reduced down to 92pF during power-down.

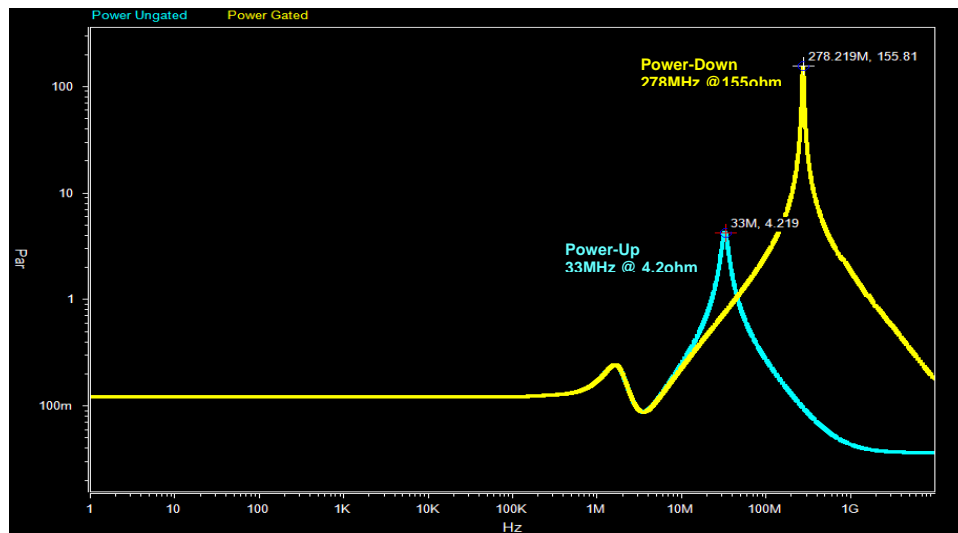


Fig. 10. PDN resonance is shifted to a high frequency when the gated power domain is off; due to the intrinsic capacitance (6.6nF) has diminished (reduce to 92pF) when the gated logic is un-charged to 0V. The resonances correlate to the measured voltage oscillation period as shown in Figure 9

Figure 10 explains how the PDN $Z(f)$ is shifted comparing a full capacitance (power-up) to a diminished capacitance (power-down); whereby the PDN resonance is shifted to the higher frequency; and therefore changing the noise droop oscillation to a higher frequency range.

The capacitance offset observed in silicon measurement during power gating / un-gating event are un-called for. This was not accounted in early simulation and is difficult to be model in SPICE. Figure 11 shows the pre-silicon simulation vs post-silicon measurement side by side. The power gate model has fairly good correlation to the transient voltage measurement. However, the very high frequency oscillation as seen in the measurement data is not projected into the simulated result due to the phenomenon above.

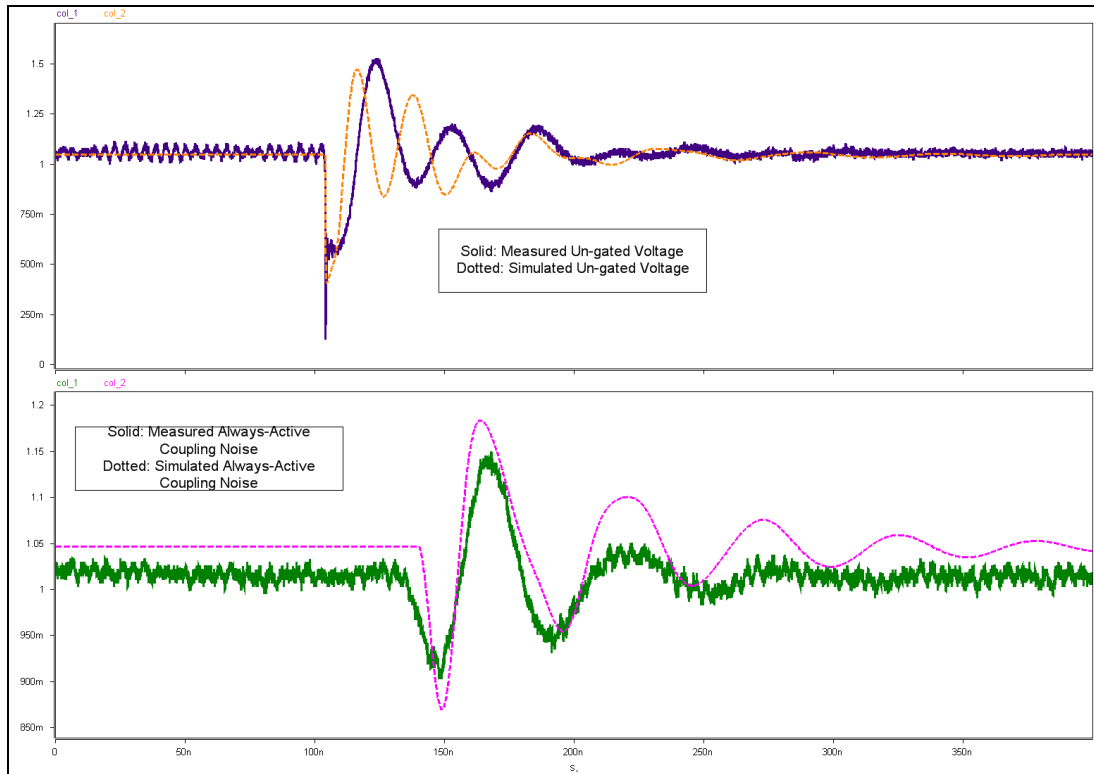


Fig. 11. Fairly good correlation between the measured active voltage noise data and power switch gate model simulation result

Future Solution: Peak Current Control Through Staggered Power-On-Off

From Figure 11, the measured undershoot and overshoot voltages are larger than the earlier expectation. This sporadic and significantly high voltage can degrade the transistor's reliability and create potential EM issue. Furthermore, if the advice of the effective motherboard BSC implementation is not well received by the customers, then their products are exposed to potential functional failure. Due to this, for friendlier customer board design and better reliability, the voltage droop can be improved by limiting PFET gate count to reduce the rush current. This solution sounds better instead of requesting the customer to increasing the real estate decoupling capacitors.

The PFET power gates are divided into Pre-PFET and Main-PFET. Pre-PFET consist of smaller portion of power gates and are used to charge up the gated decap cell so that the Vds does not equals to 0V before the Main-PFET gates turn on charge. Main-PFET consist of most of the power gate, the rush current is minimized when the Vds does not equals to zero.

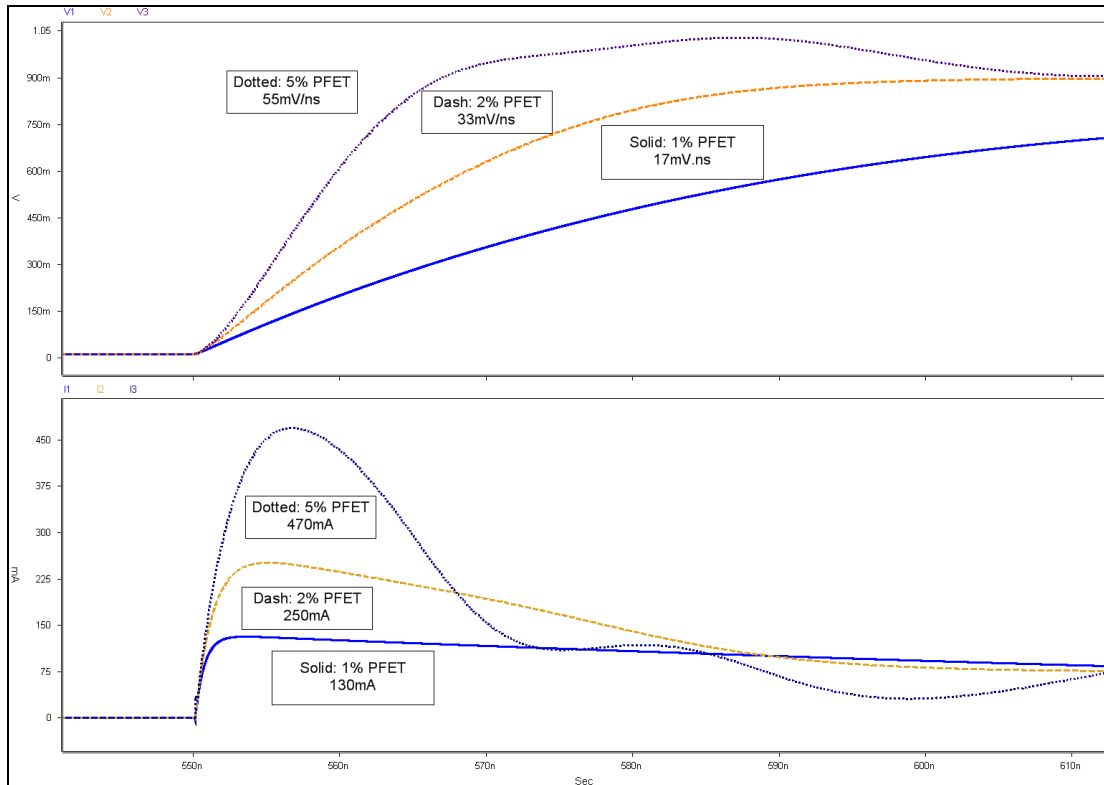


Fig. 12. From 1%, 2% and 5% PFET, the charge time is inverse proportional to the peak current

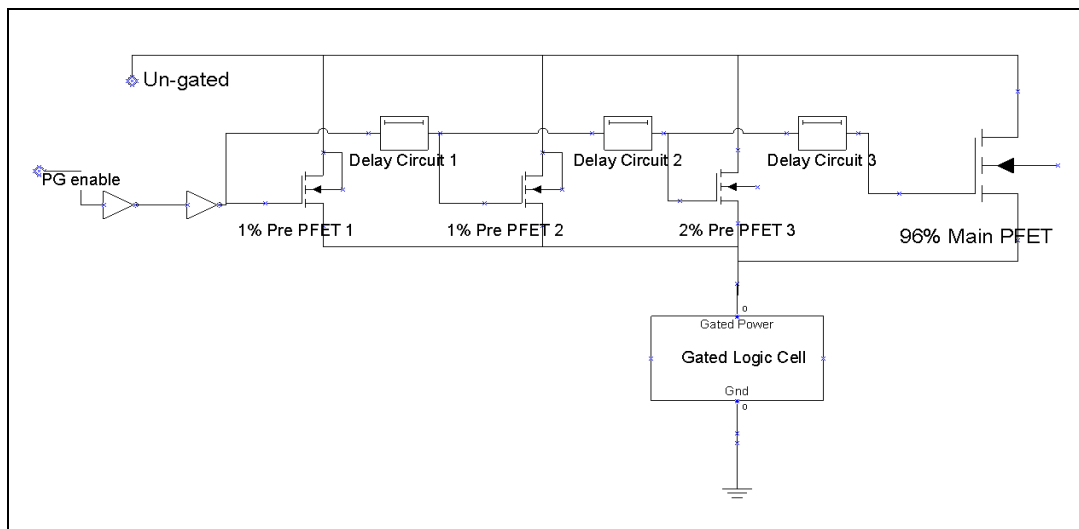


Fig. 13. 20ns delay staggered 3-stage Pre-PFET during Power-Up Sequence

From Figure 12, the charge-up time is inverse proportional to the driving current of the transistor. 1% Pre-PFET charge up time is too slow and might break the timing requirement of power management topology. 5% Pre-PFET is fast enough but the voltage droop is also larger. For optimization purpose, a ‘what-if’ analysis case study a 3-stage Pre-PFET power gates implementation as illustrated in Figure 13 is demonstrated.

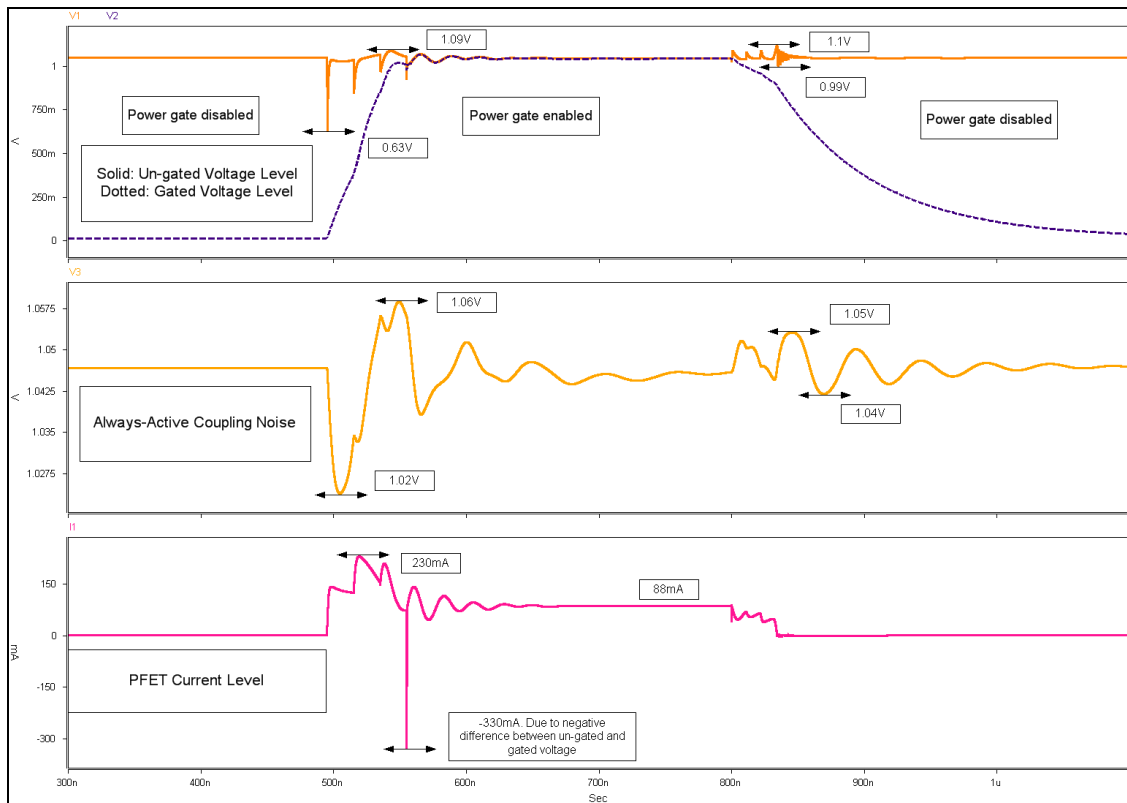


Fig. 14. Simulation result of Board A without proposed board cap with staggered 3-stage Pre-PFET during Power-Up-Down Sequence. The overshoot of un-gated voltage is reduced to 1.1V only and the coupling noise is reduced to 40mV

From Figure 14, during the first stage, 1% of power gates are turn-on. The delay time is set to $\frac{3}{4}$ of the PDN resonance oscillation period to minimize the voltage droop. At second stage, 2% power gates are turn-on to speed up the charge time further. With the same delay time, at stage 3, 4% Pre-PFET charged up the gated logic cell closer to V_{cc} . Then at the next stage, the rest of the total Main-PFET gates are enabled. In this case, the total power-up sequence delay is around 100ns only while the un-gated voltage overshoot is 1.1V only. The timing delay is reasonable without creating coupling noise and reliability concern.

Summary and Conclusion

The implementation of power switch gate into the PDN tightens up the package IR loss design budget and introduces the instantaneous switch gate turn-on voltage drop. By doing full-path DC IR drop analysis from silicon to the package and PCB, the bottle-neck of the current path can be identified and fixed to improve the average DC level and reduce the voltage distribution variance.

A simple behavior power switch gate model with estimated C_{die} value is used to simulate the instantaneous power-up-down voltage droop. It has good correlation to the lab measurement results. Difference of gated capacitance at different power states is also

measured and correlated well to the simulated prediction.

The proposed board cap can be used to effectively reduce the coupling voltage drop to the shared power domain neighbors. An alternative is implementing a staggered stages power-up-down sequence to reduce the instantaneous voltage noise is also discussed. Low power design target through power gate can be achieved by considering these design parameters carefully.

Acknowledgement

The authors want to acknowledge Ho Yoon San, Lim Han Wooi, Singh Sarbjit and Yoon Chee Kheong, Marcus Chan and See Tau Yee Hung from Intel Penang Design Center in defining the IR loss budget and lab validation activities.

Reference

- [1] F.N. Tan, K.Y. Wong, C.L. Ng, S.G. Pang, Ricky Lee, "SRAM Core Modeling Methodology for Efficient Power Delivery Analysis", *IEEE International SoC Design Conference*, 2009.
- [2] LK. Yong, "OFF Stage Leakage Analysis from Power Gating Application In Deep Sub-micron Technology", 1st Asia Symposium on Quality Electronics Design, June 2009.
- [3] Jin Zhao, Raymond Chen "A Review of PCB-level Power Delivery System," *EE Times, Asia China Korea*, May/June 2006.
- [4] S. P. Vishram, H. R. Woong, P. Kirupa, R. Sankalp, F. Farag, "Simulation and Characterization of GHz On-Chip Power Delivery Network", *DesignCon 2008*, 2008.
- [5] L. Landers, T. Virutchapunt, "The DC Design Squeeze", *Printed Circuit Board Design and Fabrication*, February 2009.
- [6] LK. Yong, SG. Phang, FN. Tan, "Power Gated Design Optimization and Analysis with Silicon Correlation Results", DAC User Track Demo, August 2009.
- [7] LK. Yong, "Design For Power Down – Strategy Vs. Performance Consideration", ISOC 2009, November 2009.