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Time and Frequency Analysis of Signal and Power Noise of a Microcontroller (μ C) plus its Packaging (LQFP+PCB)

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Abstract

In this paper an application of an integral analysis technique is demonstrated to determine the strong interaction between different Power Systems, supplying the circuitry on an IC and its Packaging.

A complex u-Controller (uC) and its wire-bonded Package plus its Test-PCB have been selected for our study, which is focused in the chosen case on the frequency and time-domain analysis methodology of Conducted Emission Noise. In particular the possibility to evaluate Power-Noise influenced Power-Supplies, including distributed on-chip and packaging decoupling capacitors, is highlighted.

Following the Spectrum Analyzer (S.A.) measurements available, the coupled interaction of the 1.5V power distribution system with the 3.3V power distribution was analyzed on the IC as well as on the PCB. Both power distributions supply simultaneously switching circuit groups of glue logic, operating at different clock cycles of 20, 40 and 80 MHz.

The S.A. measurement procedure were conducted according to BISS-ICEM2-rules.

The accuracy of the analysis is shown in comparison to the available experimental data. The short CPU run times achieved and the ease-of- use of the analysis tools to analyze such complex systems are indicated.

The shown method to determine the Power-Integrity (PI) of ICs plus their Packaging can - one to one - also be applied to determine corresponding I/O Signal Integrity (SI) situations of complex electronic designs.

Authors Biography

Ekkehard Miersch (Dipl. Phys.1963) received the Ph.D. degree in Applied Physics in 1970 from the University of Heidelberg, Germany. Joining IBM in 1970 he has worked in the Development Lab of IBM Germany and in IBM Research, USA on many different projects, including the introduction of CMOS in the IBM Boeblingen Development Lab in 1982, physical circuit design for IBM's first CMOS Main Frame Micro-Processor as project leader and the development of a planar thin-film process for High Speed Packages. He published many papers on circuit design, cooling of packages, packaging design and the electrical characterization of high speed packages and connectors. Since 2000 he works with Sigrity as scientific consultant.

His interest is High Speed Packaging design, Spice and non-ideal GND based Signal(SI)- and Power(PI)- Integrity characterization of planar and 3D PCB and Chip Packages (CP) as well as PI-analysis of IC+CP entities. E. Miersch has been IEEE member since 1985.

Mehmet Goekcen received his Diplom degree in electrical engineering at Ruhr-University Bochum/Germany in 1986.

He worked during his professional career on topics like PC-based embedded system design, high speed PCB design and analog circuit design.

He joined the Infineon Technologies AG in 2003. He is currently working on HF-Model of microcontrollers, High Speed PCB Design & Simulation, Signal- & Power-Integrity analysis of IC-Packages and PCBs and EMC-characterization of microcontrollers.

Thomas Steinecke studied technical computer science at the Technical University of Darmstadt, Germany and in 1984 he joined the "Siemens Semiconductor Group" in Munich, which in 1999 became independent as "Infineon Technologies".

He spent several years working on CMOS design and tests of 8-bit microcontrollers, PC chip sets and 32-bit RISC processors before taking over the responsibility for electromagnetic compatibility of automotive microcontrollers in 1997.

Since then, Mr. Steinecke worked on chip and package design improvement for EMC as well as on emission, susceptibility measurement techniques, EMC modelling and simulation of microcontrollers.

His work was accompanied by several test chips with on-chip voltage and current measurement sensors and the partnership in several national and international funding projects.

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Introduction

The high speed switching of large commonly clocked IC-Circuits generates large Power (P)- and Signal(S)- Noise, which increasingly endanger low voltage circuit design, where the currents and the connection inductances do not scale down the same way as the supply voltages are scaled. The other observation is, that the quality of Signal (SI)- and Power- (PI) Integrity of Signal- and Power- Distributions are tightly coupled.

One can basically categorize three types of P/S-Noise problems:

- 1.) P/S-Noise can cause Functionality problems with regard to
 - a.) reducing the anticipated speed of circuits
 - b.) or even initiate circuit failures and
 - c.) eventually lead to latch-up effects in CMOS circuitry.
- 2.) The other form through which P/S-noise causes trouble within a design is the Conducted Emission. Conducted Emission noise leaves the IC through the Chip-Package (CP) and disturbs the switching of the other circuits on the same IC-Package or circuit components on the PCB.
- 3.) The third problem the Radiated Emission, which is also caused by the originally on the IC generated Conducted Emission. Leaving the IC as high frequency Conducted Emission noise, this noise radiates off longer PCB-lines, which act as antennas..

In all cases additional costly design efforts are required to preventively minimize such noise problems. But there is always the big unknown , which magnitude of actually occurring P/S-Noise can be expected. The only way to get this information before building hardware is to perform a noise simulation which has to investigate the complete design, which means ICs +Package + Board.

Why is there a need to incorporate the complete IC-Packaging into the IC- PI/SI- Analysis?

- It is clear that P/S-noise propagates from one on-die location to another.
- However P/S-noise often propagates more easily to other locations of the chip through the package signal- , power- and ground- structures, rather than directly through the IC power/signal grid itself. Reason is that the propagation attenuation on the IC with its Silicon substrate carrier is much higher than on the low loss packaging units.
- Additionally the Electromagnetic Interactions/Resonances inside the Package Structure affect IC P/S-noise. See Fig.3.

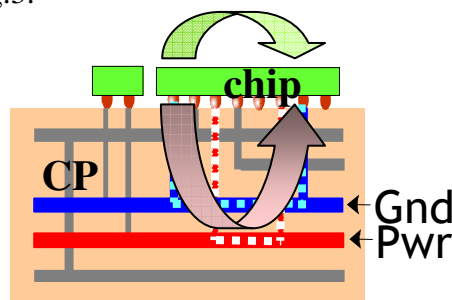


Fig.3. On-IC-P/S-noise can propagate within the IC and also through the IC- Packaging from one on-die location to another .

Background to the performed Simulation Analysis

The strategic task of this paper was to first concentrate the analysis mainly on the Power Noise, transferred on defined power nets into the PCB power system of the u-Controller packaging setup . One of the reasons is that precision Spectrum Analyzer measurements are available, with which the simulation results can be compared.

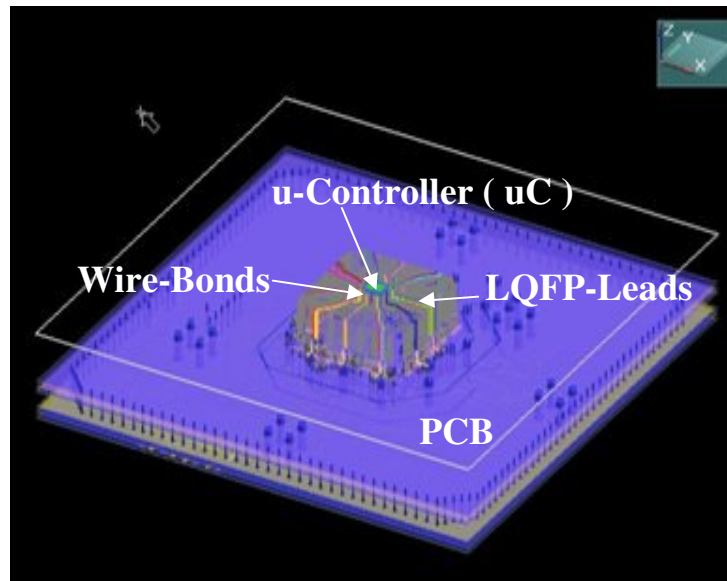


Fig. 1. Fig.1 shows the u-Controller under Test and the main parts of its Packaging

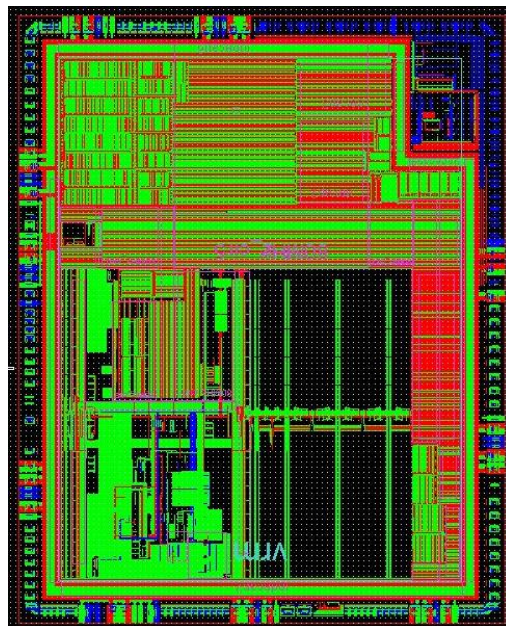


Fig.2. The investigated u-Controller and the two Power Voltage Distributions 1.5V (red), 3.3V (blue) and the common Ground Return System (green) plus the IC-I/O Pads are shown. All Metal Layers are activated simultaneously in this Fig.2

In the case of the μC under test two power distribution systems with 1.5V and 3.3V exist and supply the Glue-Logic. By their nature they are separated on the IC.

However an on-IC coupling between the two power-systems cannot totally be suppressed. Reasons are still remaining areas of direct coupling and the common IC-substrate. Additionally the two power distribution systems of $V_{DD} = 1.5\text{V}$ and $V_{DDP} = 3.3\text{V}$ share the same Ground (current return) system.

To understand the influence of the switching-noise of the individual Glue-Logic parts with 20MHz, 40 MHz and 80MHz onto each other and between the two Power Distribution Systems, the total $\mu\text{C}+\text{Package}+\text{PCB}$ structure has to be analyzed.

And the $\mu\text{C}+\text{Package}+\text{PCB}$ structure needs for several reasons to be analyzed as an entity in the Frequency- and Time- Domain environments with regard to the P/S Noise and the Power Integrity required. Also the decouplers on the μC and on the Packaging have to be considered as key elements and possibility to minimize P/S-noise generation and transfer. Both, the Frequency- and Time- Domain simulation concepts are using Spice notations.

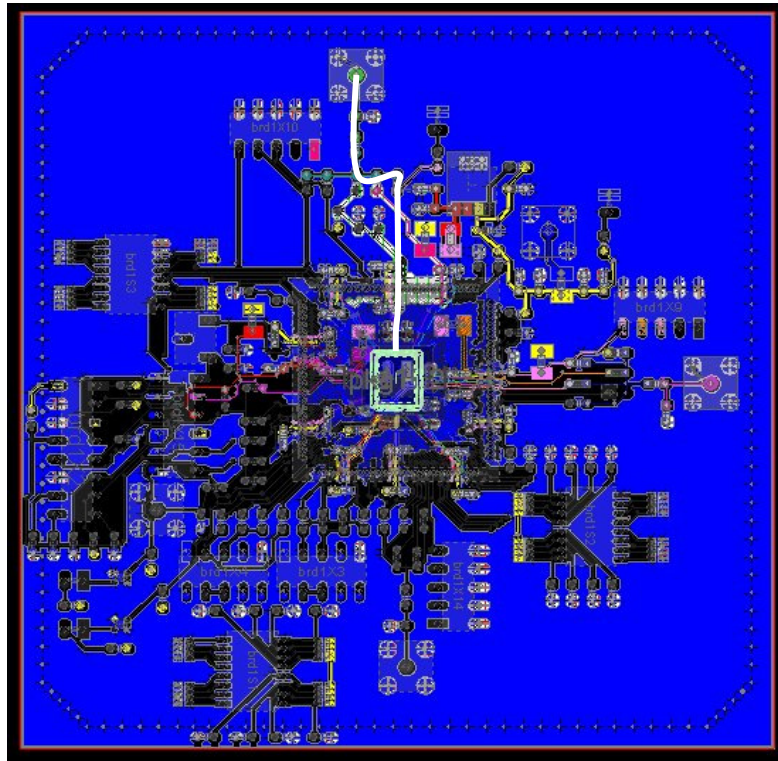


Fig.4. In Fig.4 is a PCB power net shown, which supplies the u-Controller with 1.5V. The PCB-net is on one side connected to the u-Controller via LQFP leads and Wire-Bonds. The other end of the PCB-Net contacts a SMB Connector to which the Spectrum Analyzer is connected.

The BISS Concept

The performed Spectrum Analyzer measurements followed the BISS (Ref. 1.), Ref. 2.)) rules and consequently the simulation analysis followed these concepts, also described in Ref. 2.) as ICEM2 approach.

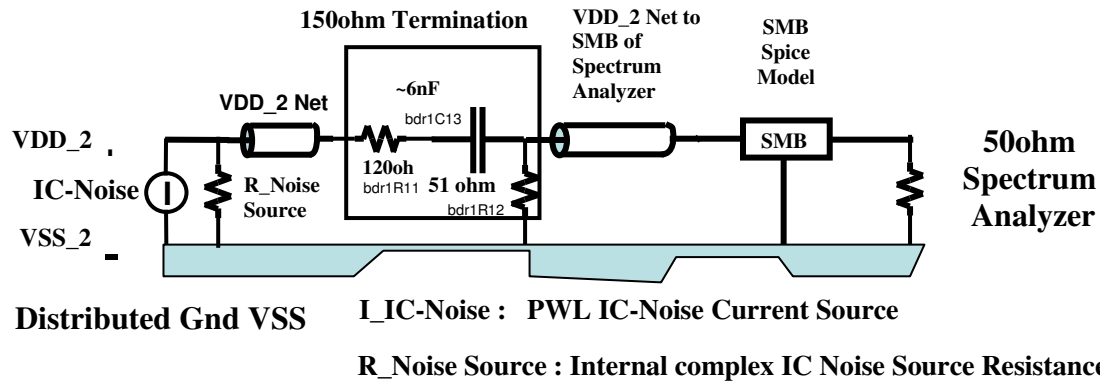


Fig.5. The implementation and the modeling of the Spectrum Analyzer measurements is shown.

Analysis Techniques to simulate the Conducted Emission on Power Nets in Time- and Frequency-Domain

General Remarks

In the Sigrity Program Flow-Charts of Fig.6 and Fig.7 the individual simulation steps for the Time-and Frequency- Domain Programs are shown, which provide after successful simulation-runs time- and frequency- dependent voltages within the Chip Power-Distribution-Nets, at the Power- and Signal-I/Os of the IC, and at all locations of the Packaging which are of interest. Ref. 7.) , Ref. 8.).

The used programs can include the I/O-circuitry in BSIM form, but they presently do not provide detailed internal IC-circuitry information, describing the time dependent behavior of individual internal circuits e.g. on transistor level.

The IC internal circuits are characterized as groups and in form of Current Signatures, describing the currents which are switched by the individual circuit groups e.g. during a single operation clock cycle.

The shown analysis techniques can therefore provide Signal Integrity for I/O signals only. Carrying I/O-signals is basically the nature of most of the nets in Packaging.

Time-Domain Calculation Concept #1

The Conducted Emission of the in Fig.4 and Fig.5 shown 1.5V power supply net VDD_2 and its Gnd.net VSS_2 was determined with commercial Sigrity tools.

For the Time Domain analysis two methods were applied.
 Method #1 : The 3D full wave FDTD tool XcitePI –TD (TD = Time Domain) can be used, which mainly extracts the R,L,C,k behavior of the on-IC power distribution grids. Actually XcitePI-TD is a Spice based R,L,C,k extraction tool on IC-level which can provide packaging model inputs for Spice engines. Electrically the current signatures of the circuitry applied to the R,L,C,k power-net grids cause power voltage changes (power noise).
 Sigrity’s FDTD tool Speed2000, describing the electrical behavior of the Packaging (IC- Package + PCB), is then automatically combined with XcitePI-TD with the help of the third Sigrity-tool CoDesign. The program CoDesign can calculate the voltage behavior $V(t)$ at all Packaging location of interest.
 Spice-based time-domain calculations which are performed by XcitePI-TD together with the Spice-based Speed2000 FDTD-calculations require large computer resources with regard to main memory and computing time when applied to complex Packaging geometries. This is a practical disadvantage of solution concept #1 compared solution concept #2 described below. To determine the VDD_2 of Fig.5 at the output of the SMB connector, nearly 2 days run-time was required on a 64b machine with a 64b Intel 3.2GHz-processor and 8GB main memory. See also Fig.8.

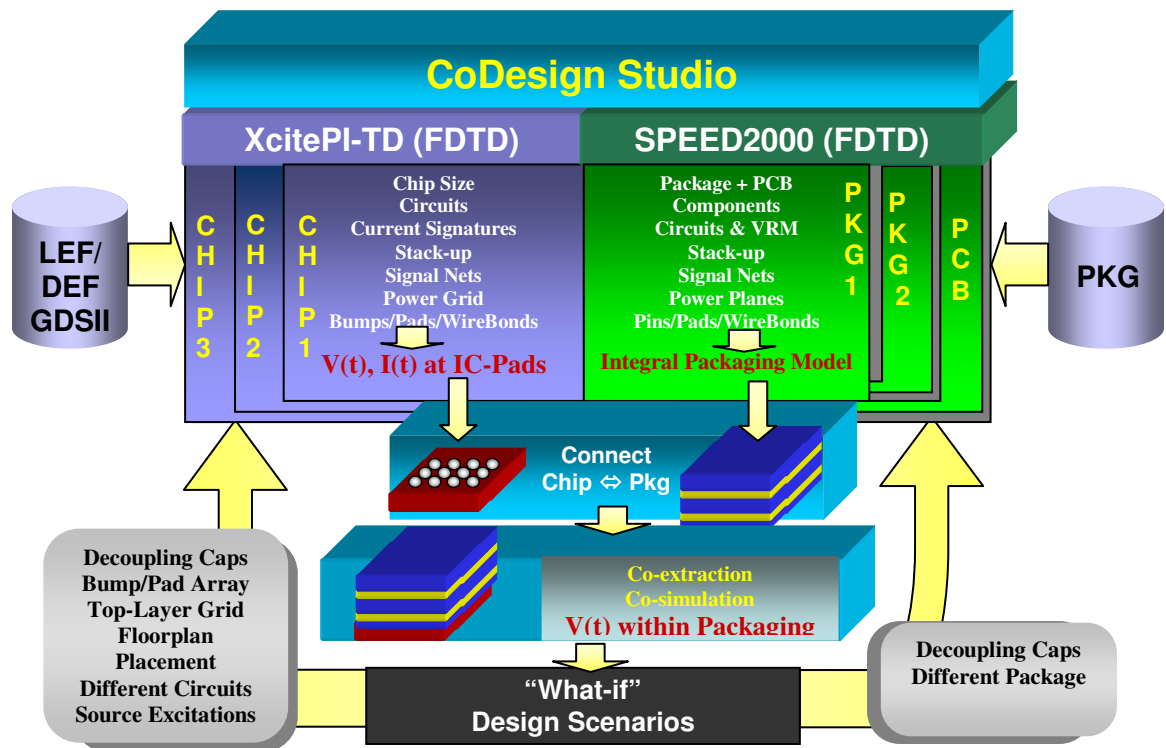


Fig.6. The Sigrity Program Design Flow for the Time-Domain Analysis and R,L,C,k Parameter Extraction of ICs plus attached Packaging (Chip Carrier plus PCB) is shown.

Frequency-Domain Calculation Concept

For the frequency analysis Sigrity's tool XcitePI-FD (FD = Frequency Domain) was used. See Fig.7. Several calculation steps are required.

In a first step XcitePI-FD calculates the S-matrix, based on the description of the u-Controller (uC) with 50ohm Ports, at the uC-Power-Pads and at observation points, defined by the current-signatures of the on-IC circuit-groups under test.

In a second step the Packaging has to be modeled by Sigrity's frequency-domain tool PowerSI. PowerSI is here operated in Spatial-Mode (PowerSI-sm), calculating the voltage behavior as a function of frequency $V(f)$ at Packaging locations of interest.

In a third step the uC-S-Matrix, generated by XcitePI-FD, is then combined with the PowerSI-sm run, describing the uC-Packaging. Within PowerSI-sm the uC-S-Matrix, representing the frequency behavior of the uC, stimulates the frequency behavior of the uC-Packaging and the individual $V(f)$ behavior of the uC-Packaging can be simulated at locations of interest.

In a fourth calculation step again in PowerSI, the $dBuV(f)$ are calculated from $V(f)$. The $dBuV$ simulation results can directly be compared with the results obtained through Spectrum Analyser measurements. See Fig5. and Fig.7 below.

In PowerSI the LQFP is merged with the PCB a to complete Packaging model, where also the model of the SMB connector was added in Spice format.

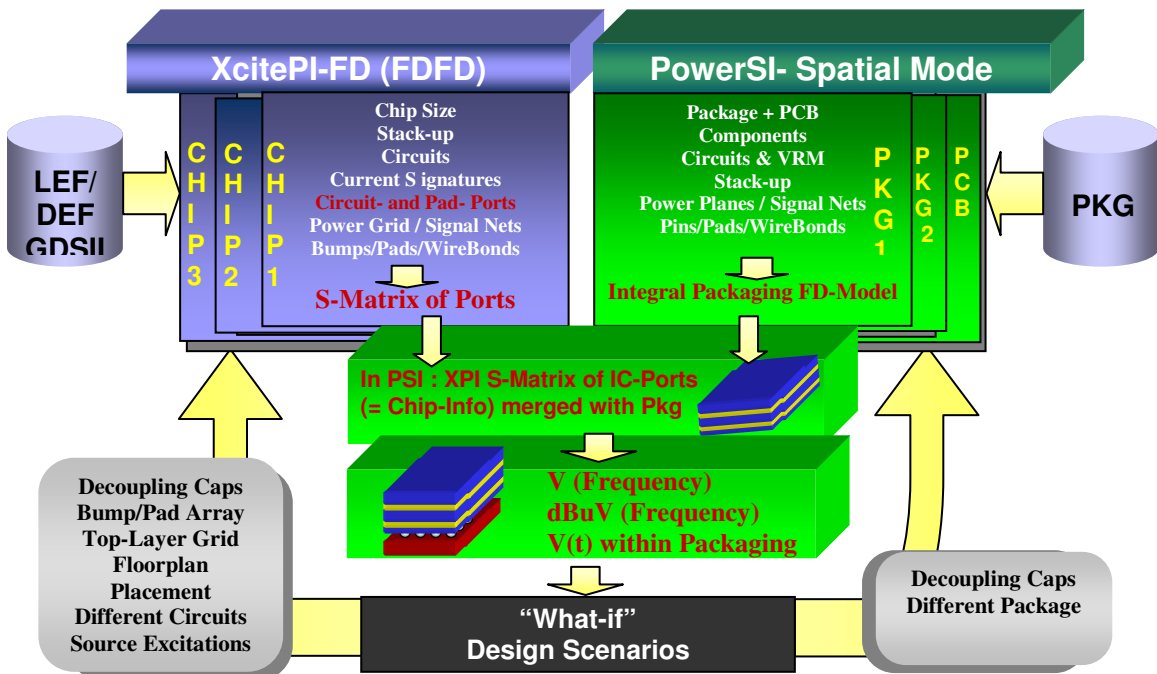


Fig. 7. Additional to the analysis of the original design the analysis method naturally allows to improve the performance of the design through an "What-if" design scenarios.

Time-Domain Calculation Concept #2

As mentioned above, with the frequency behavior of the uC in form of an S-matrix plus the uC-current signatures, the frequency behavior of the uC-Packaging can be stimulated and also simulated in PowerSI-sm. at all locations of interest. The current signatures of the glue logic analyzed are defined for a clock cycle and have therefore periodical character.

Consequently the periodic $V(f)$, generated by PowerSI-sm, can be converted by discrete inverse Fourier Transform idFT into a $V(t)$.

The first time domain CoDesign analysis with a slightly smaller VDD-power grid reduced the computer run time from Days to Minutes. See Fig. 8. below.

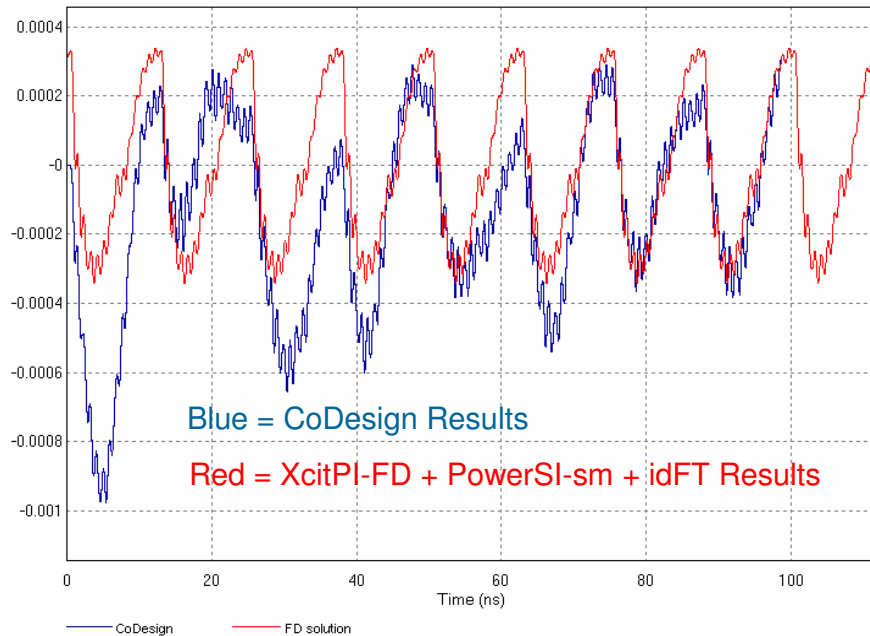


Fig.8. XcitePI-FD extraction engine used 948MB and 178 sec CPU time
Discrete inverse Fourier Transform needs 10 sec, total 42min PC-time
CoDesign takes about 42 hrs to finish 100ns of simulation: ~ 60 times slower.
Computer used: 64 bits Windows, 8 GB memory, 3.2 GHz CPU

Results

Representative for many analysis results, the comparison between Spectrum Analyzer Measurements and the Simulation of the Conducted Emission Noise is shown in Fig.9. The noise is generated by groups of Glue Logic sitting on an u-Controller. The circuits switch simultaneously at 20MHz, 40MHz and 80MHz and are also differently supplied by 1.5V and 3.3V. The noise is measured at the end of one of the 1.5V rails, supplying the u-Controller with power of a VRM, which is positioned on the u-Controller's PCB. Of interest are the high amplitudes of the Harmonics of 20, 40 and 80MHz, which can cause beside the Conducted Emission Noise also considerable Radiated Emission Noise.

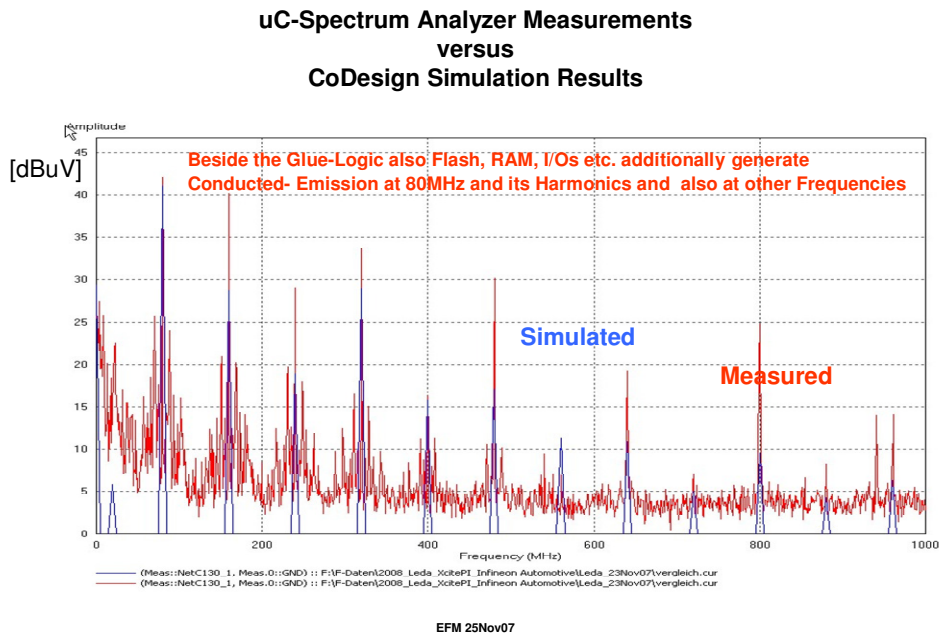


Fig.9 . The Conducted Emission, reaching the SMB (Fig.5), is shown in dBuV as a function of Frequency . The Harmonics of 80MHz are dominant, because the bigger part of the glue logic switches with an 80MHz clock cycle.

Summary

It could be shown, that with the applied FD-techniques the electrical analysis run-times of complex integrated IC-designs can be reduced to very efficient simulation times. Even more complex designs can now be simulated with computer run times below 1 hour and with acceptable good accuracy. The achieved accuracy is a function of the completeness of the Circuit signature inputs. In the shown example large parts of the u-Controller circuitry are not considered in the simulation. See Fig.2. It turned out that very valuable design information be obtained from an analysis which considers only defined circuit parts of the total u-Controller circuitry.

References

- 1.) Generic IC EMC Test Specification Version 1.0 , 2004, Bosch, Infineon, SiemensVDO (BISS)
- 2.) Emission Models for VLSI-ICs , Thomas Steinecke (Infineon), EMC Zürich 2005
- 3.) Signal and Power Integrity Analysis of large complex PCBs :
Theory, Implementation, Simulation and Result Verification by Measurements ,
Ekkehard Miersch, PIERS 2004, p.164
- 4.) Power Integrity Analysis of a Microcontroller plus its Chip Package.
Dr. Ekkehard Miersch (EFM Consulting), Thomas Steinecke,
Mehmet Goekcen (both Infineon Technologies AG)
EMCCompo Nov.2005, Munich, Germany
- 5.) EMI Modeling and Simulation in the IC Design Process
Thomas Steinecke (Infineon), Dirk Hesidenz (Infineon), Dr. Ekkehard Miersch
EMC Zurich-Singapore, 2006
- 6.) Application of Integral Analysis Technique to Determine Signal- and Power
Integrity of Advanced Packages.
Nebojša Nenadović (NXP) , Ekkehard Miersch (EFM), Martin Versleijen (NXP), Sidina
Wane (NXP) , EPEP 2007
- 7.) Sigrity Inc. SOCcentral.com, "On-Chip Power Integrity, Including Package Effects"
- 8.) Sigrity Inc. "PowerSI User's Guide", "CoDesign Studio User's Guide",
"XcitePI User's Guide", "Speed 2000 User's Guide"