System IO Planning and Design Feasibility – Challenges and Solutions

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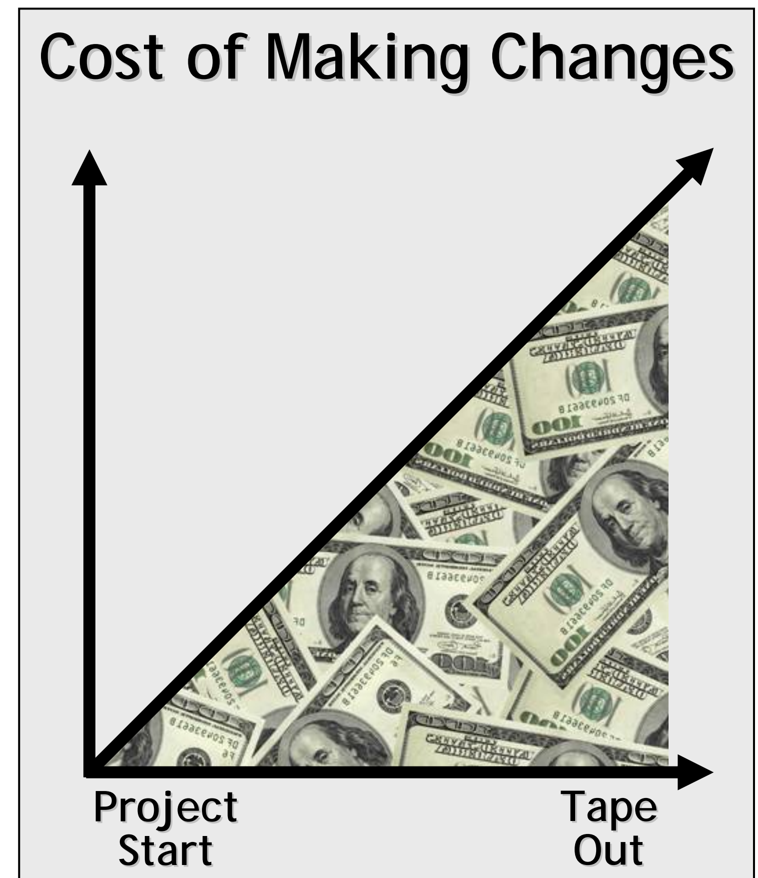
Objectives of System IO Planning

- Coordinate device placement with associated pin and net assignments across the chip-package-board system
- Find and fix cross domain issues while in early stages of design planning
- Minimize overdesign and associated cost impact



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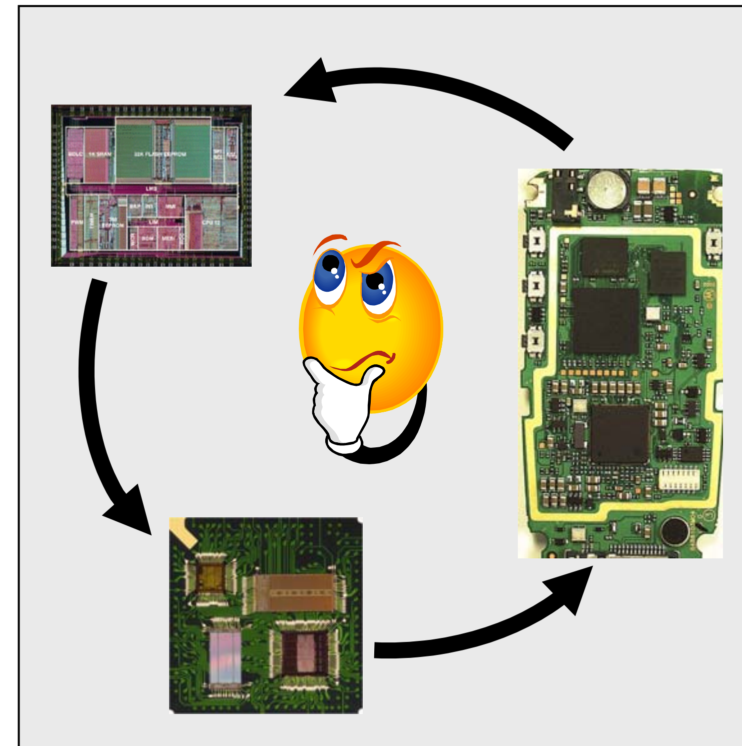
Trends and Considerations for IO Planning

- Geographical separation of design teams
- Greater interdependency between domains
  - High speed interfaces
  - Die size and IO configuration
  - Multiple voltage domains
- Increasing design cycle time
  - Complex interactions requiring more iterations and taking longer to complete



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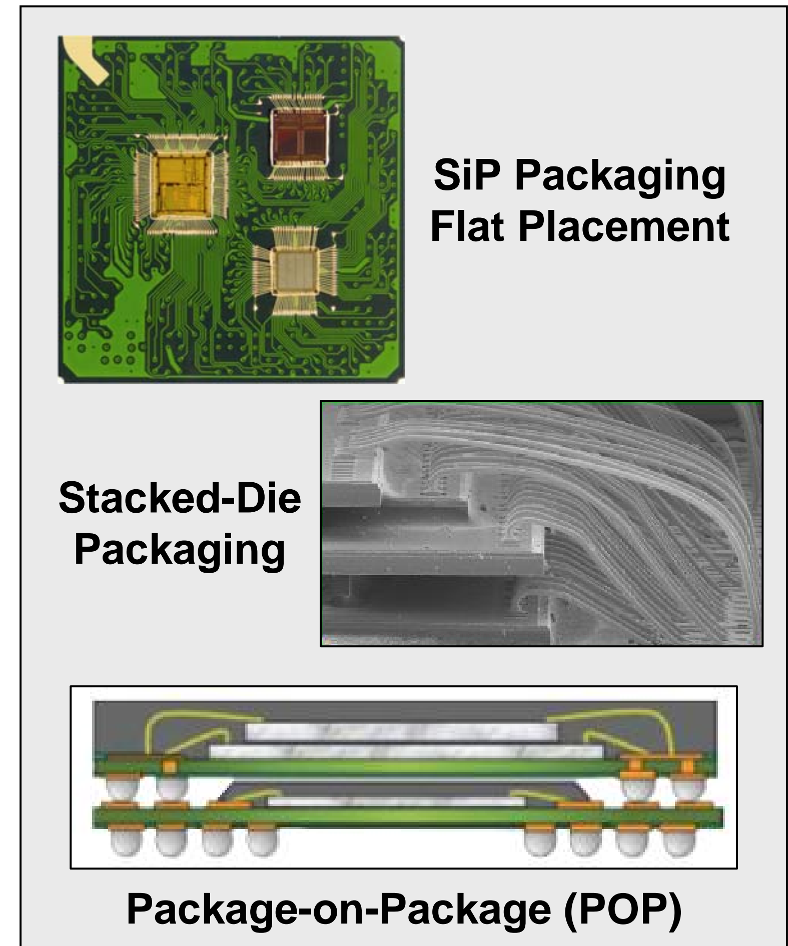
Increased Integration at the Package Level

- 3D and multi-die packaging
  - SiP or package-on-package
  - Thru-Silicon-Via (TSV) packages
- Die to die connectivity
  - IO optimization between fixed and free devices
  - Impact of attachment technology
- Application specific packaging
  - Package variants
  - One die into multiple packages



Traditional Approach to IO Planning

- How do you communicate between design domains and databases?
  - Spreadsheets
  - Proprietary tools
  - ASCII files
  - Scripts
- Excel is the most common IO planning tool, but…
  - It's error-prone
  - Uses static data

	A	B	C	D	E	F
1	SIDE	PIN_NUMBER	PADSTACK	x	y	rotation
2	ARRAY	105_12_6	BUMPPAD_80x80	3850	1951.4	0
3	ARRAY	106_13_6	BUMPPAD_80x80	4150	1951.4	0
4	ARRAY	107_14_6	BUMPPAD_80x80			
5	ARRAY	108_15_6	BUMPPAD_80x80			
6	ARRAY	109_0_7	BUMPPAD_80x80			
7	ARRAY	110_1_7	BUMPPAD_80x80			
8	ARRAY	111_2_7	BUMPPAD_80x80			
9	ARRAY	117_12_7	BUMPPAD_80x80			
10	ARRAY	118_13_7	BUMPPAD_80x80			
11	ARRAY	119_14_7	BUMPPAD_80x80			
12	ARRAY	120_15_7	BUMPPAD_80x80			
13	ARRAY	121_0_8	BUMPPAD_80x80			
14	ARRAY	122_1_8	BUMPPAD_80x80			
15	ARRAY	123_2_8	BUMPPAD_80x80			
16	ARRAY	129_12_8	BUMPPAD_80x80			
17	ARRAY	130_13_8	BUMPPAD_80x80			
18	ARRAY	131_14				
19	ARRAY	132_15				
20	ARRAY	133_0				
21	ARRAY	134_1				
22	ARRAY	135_2				
23	ARRAY	141_12				
24	ARRAY	142_13				
25	ARRAY	143_14				
26	ARRAY	144_15				
27	ARRAY	145_0				
28	ARRAY	146_1				
29	ARRAY	147_2				
30	ARRAY	153_12				
31	ARRAY	154_13				
32	ARRAY	155_14				
33	ARRAY	156_15				
34	ARRAY	157_0				
35	ARRAY	158_1				
36	ARRAY	159_2				
37	ARRAY	165_12				
38	ARRAY	166_13				
39	ARRAY	167_14				
40	ARRAY	168_15				
41	ARRAY	169_0				

TOP view

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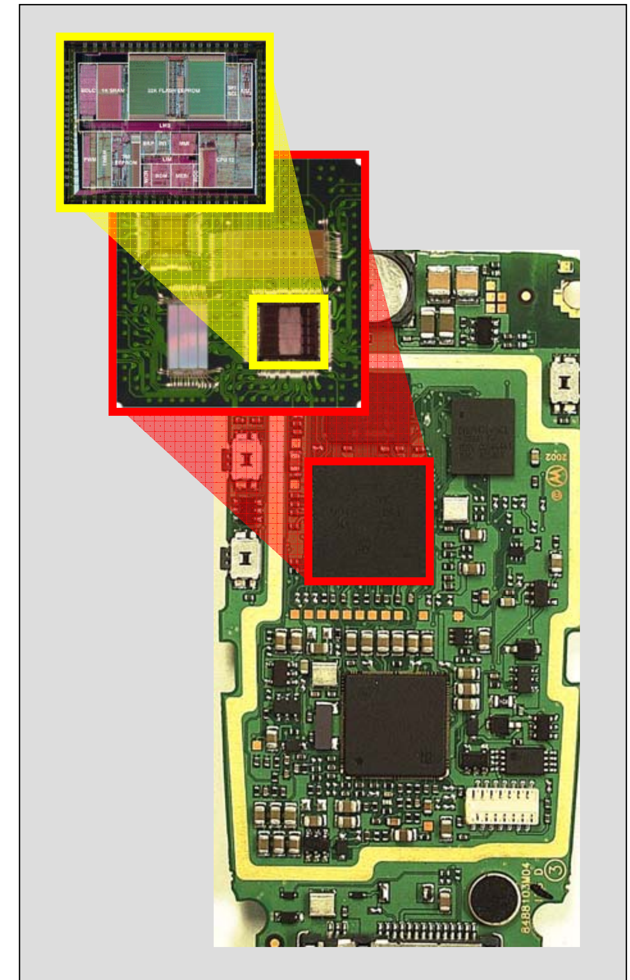
First Generation of Codesign / IO Planning Tools

- Most are a hybrid of IC and PCB tools with no dynamic interaction
  - IC tools are single die oriented
  - Package/PCB tools lack silicon visibility
  - “Connectivity Manager” wrapper

- Drawbacks / shortcomings
  - Poor management of virtual data
  - Lack of feasibility tools – detailed only
  - Multi-die pad-ring planning
  - Support for 3D packaging



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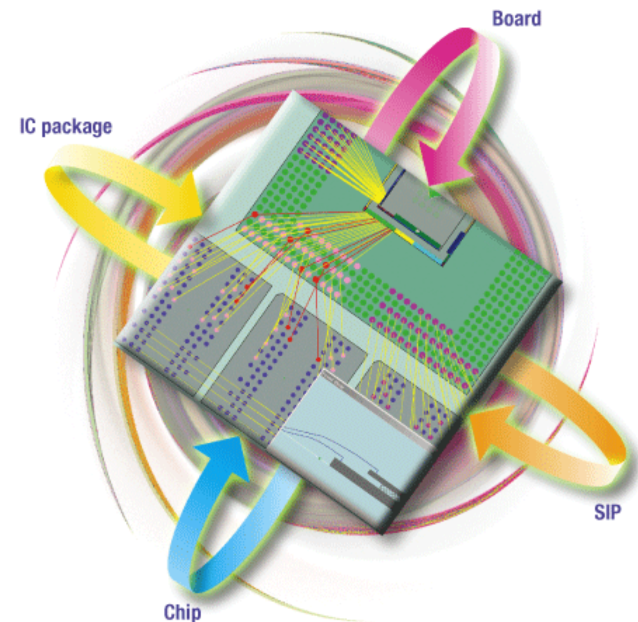
The New Generation of IO Planning

- See the complete picture - chip, package, and board design planning in a unified environment
- Dynamically optimize and evaluate gate to board level connectivity
- Model detailed design aspects using powerful feasibility functions
- Start at high levels of abstraction and easily transition to detailed design content



- 3D aware to support TSV, PoP, and stacked-die

Reduce iterations, cost, and complexity!

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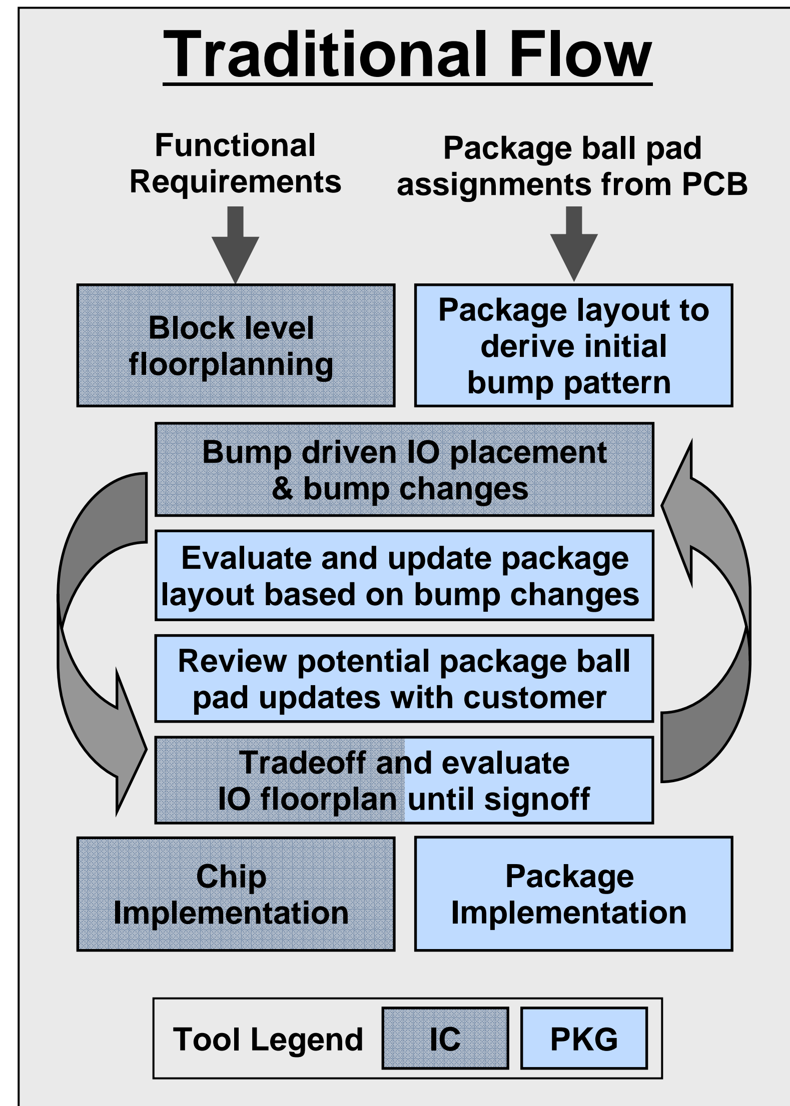
Flip-Chip Flow - Traditional

- Scenario
  - Medium sized fabless
  - Socket compatible design
  - Flip-chip ~1400 bumps
  - Package is half of finished device cost
- Results (traditional flow)
  - 8 die size iterations for cost
  - 30 different bump maps
  - 40 iterations of the package
  - 20+ weeks to converge on IO design plan



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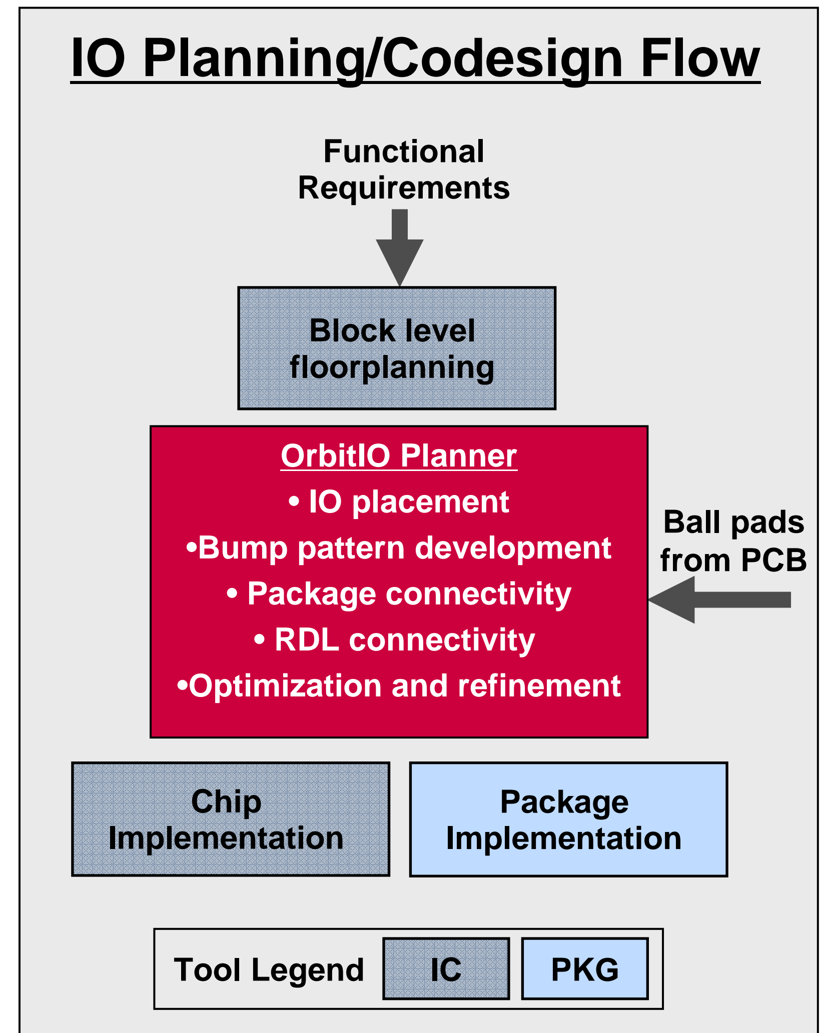
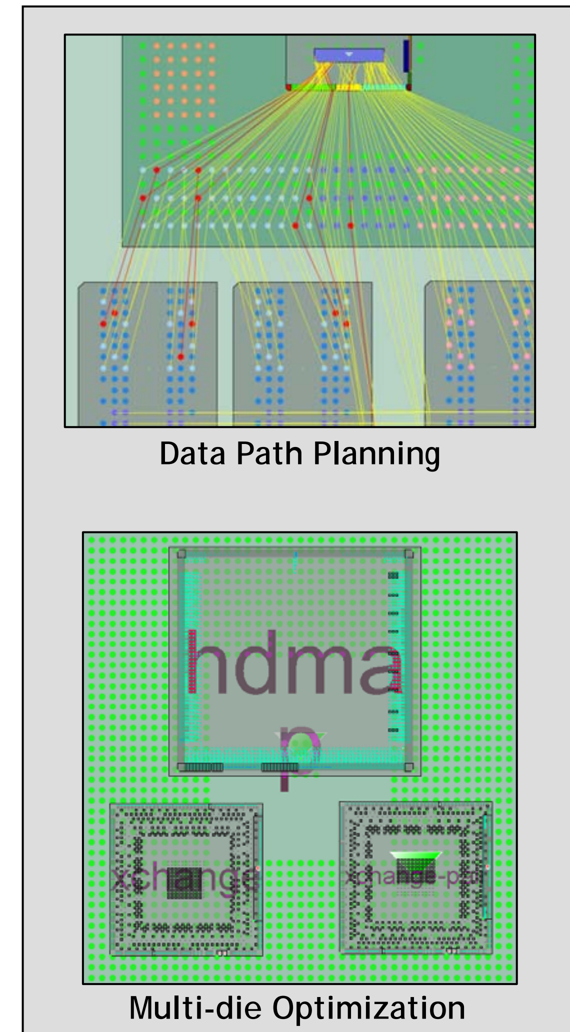
Flip-Chip Flow - Codesign

- Results (codesign flow)
  - Package layout does not need to be completed prior to IO place
  - Evaluate package bump connectivity without layout
  - Evaluate RDL connectivity prior to chip implementation
- Benefits
  - Faster convergence on IO plan
  - Fewer and faster iterations
  - 40% reduction in cycle-time



Applications of System IO Planning

- Data path planning and optimization from macro level to PCB
- Determine minimum die size based on required IOs - RFQ
- Drive IO pad-ring placement based on package requirements
- Evaluate flip-chip or wirebond design feasibility
- Optimize net list and placement for multi-die packages



Data Path Planning

Multi-die Optimization

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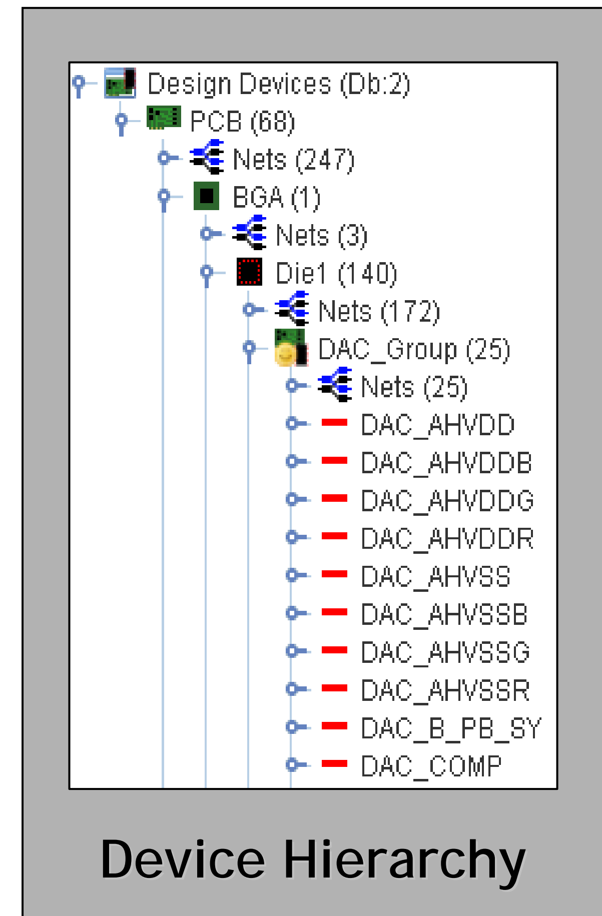
Key Components of an IO Planning System: Data Management and Integration

- Unified data model
  - The foundation for dynamic interaction
- Hierarchy management
  - Relationships between domains
- Import / export mechanisms
  - Compatibility and communication
- Data mapping
  - Managing differences and equivalences
- Virtual data and ECO management
  - Work through incomplete and changing information



Device Hierarchy

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Key Components of an IO Planning System: Device Placement

- Automatic and interactive placement tools
  - Transparency and adaptability
  - Substrate specific or region based rules
- Flexible pad-ring construction
  - Spreadsheet driven
  - Instantiate on-the-fly
  - Sequence based placement
- Multi-die optimization
  - Simultaneous device placement and pin assignment

```
    <Device selector = "name" value
    <Device selector = "name" value
</Sequence>
<Sequence name = "GPIO">
    <Device selector = "name" value
    <Device selector = "name" value = "gpFill"/>
    <Device selector = "name" value = "gpVSS"/>
    <Device selector = "name" value = "gpVDD" postspace =
</Sequence>
<Sequence name = "staggerWirebondPad3">
      <Device selector = "name" value = "W"/>
```

Sequence Based IO Cell Placement

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Key Components of an IO Planning System: Design Feasibility

- Impact of feasibility
  - Validate quality of placement
  - Influence on connectivity
  - Speeds design decisions
- Feasibility engines
  - Ease-of-use, rules driven
  - Fast, highly automated
- Evaluate
  - Wirebond configurations
  - Flip-chip and RDL routeability

RDL & Bump Route Feasibility

Evaluating Wirebond Feasibility

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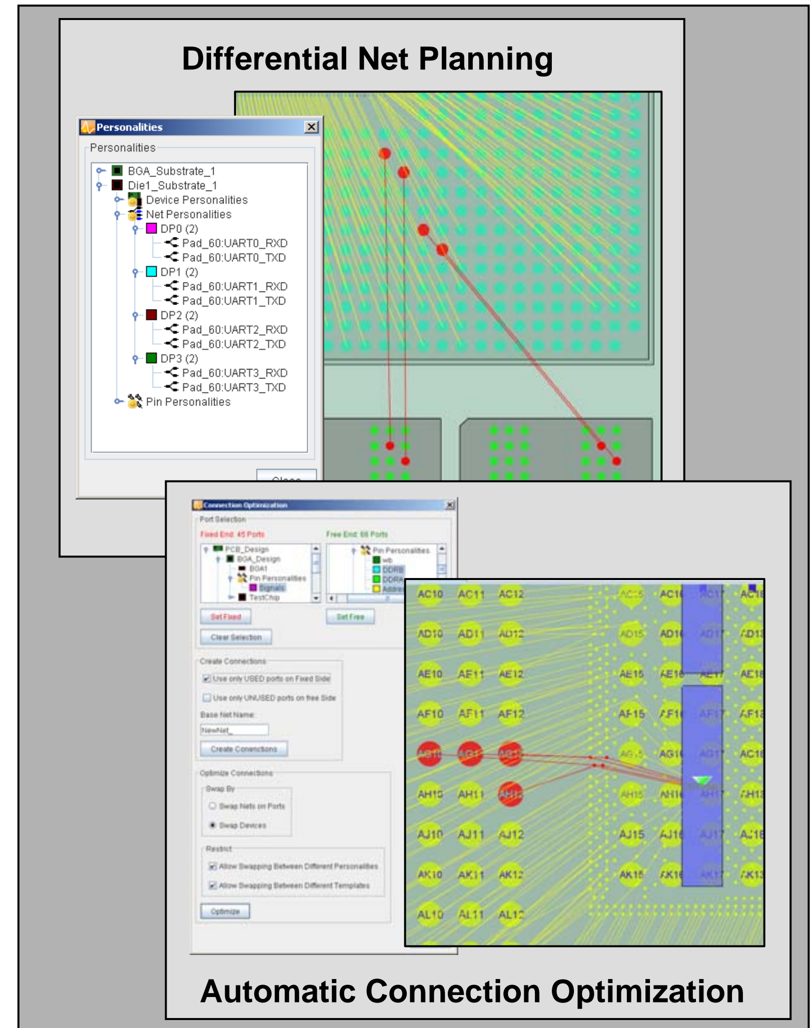
Key Components of an IO Planning System: Connectivity Planning and Assignment

- Defining and optimizing connections between devices
  - Driving connectivity from one domain to another
  - Adaptability, top-down, bottom-up
- Constraining the problem
  - Grouping of design objects
  - Diff pairs, layer use, SPG ratio
- Automatic and interactive tools
  - Must work in conjunction with placement and feasibility functions
  - Iterative optimization to balance multiple objectives



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Benefits of System IO Planning and Design Feasibility

- Reduce iterations and shorten cycle-time
  - Easily evaluate chip/package/board tradeoffs within a single tool early in the design process
  - Identify and fix problems sooner
  - Reduce issues with outsourced design services by better communicating design intent
- Better manage cost and package complexity
  - Minimize over-design due to poor planning
  - Maximize the value of SiP by achieving the best configuration through multi-die optimization

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Conclusion

- Thank you for your attention

- To learn more…
  - Stop by the Sigrity booth #613
  - Contact Kevin Rinebold: rinebold@sigrity.com
  - Visit www.sigrity.com