DesignCon 2009

The Effects of Chip and Board Behavior on Package-Centric, System-Aware Power Delivery Design

Virendra Adsure, Intel Corporation

Long Wang, Intel Corporation

Jiang Li, Sigrity Inc.

Abstract

A package Power Delivery System (PDS) design is examined to determine the effects of both chip and board electrical behaviors. PDS performance variations amongst four package design states are considered: (1) no knowledge of chip or board, (2) board-aware, (3) chip-aware, (4) both chip- and board-aware. Optimization of the package PDS decoupling design is performed for each state. Variations amongst these design implementations are compared for performance, number of decoupling capacitors, and manufacturing cost. The benefits of pursuing system-aware package design and quantitative impacts of not having access to package-external data are demonstrated.

Author(s) Biography

Virendra Adsure has been with Intel for the past three years working on chip package design, prior to that he worked with Eastman Kodak on platform signal and power integrity. He has a MSEE from Binghamton University and a BEEE from Maharaja Sayajirao University, India.

Long Wang has been with Intel for 10 years in Electronic packaging, signal and power integrity field. Prior to Intel, he worked with Hewlett Packard and Japanese Electronic Material America Corp, respectively. He has been working in the industry for 16 years. He received BS, MS and Ph.D. degrees in E.E, 1986, 1989 and 1998 respectively.

Jiang Li got Ph.D. degree in electromagnetic theory and microwave engineering from University of Electronics Science and Technology of China in 1988. For the last 10 years, she's been working on signal integrity and power integrity related issues, mostly in HP's high-end system Lab. She joined Sigrity in 2007, and is currently Sr. application engineer.

Overview

An IC package provides electrical connections between chip and system board for both signals and power. With increasing data rates, switching currents and reducing supply voltages, the need to characterize the package as part of a larger chip-package-board system is growing. A typical chip-package-board configuration is shown in Figure 1. High performance power delivery system (PDS) on package has become essential due to its impact on SSN and other ill effects to signal integrity. However, few package designers have ready access to electrical performance data for chip and board to enable a system-aware package-centric simulation or system level co-simulation. Also, often times, the quality and quantity of the chip and board data available to the package designer changes as the design progresses. At the beginning of the package design cycle when the chip design is also just starting it is difficult to get reliable data about the chip. The same is true about the board data which many times comes when the package design is at a very advanced stage.

In this paper we optimized the decoupling on the package based on the level of the available information and studied its impact on the system.

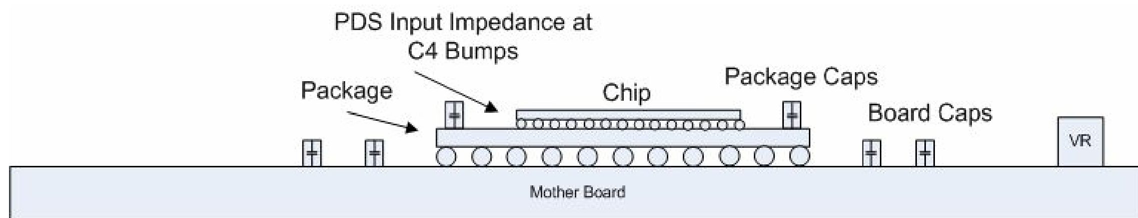


Figure 1: Package in System

The nominal package design examined in this paper is a 12 layer flip-chip BGA. The power supply rail examined in detail for this design has 44 on-package die-side capacitors (DSCs). The chip and board models are in general represented as multi-terminal SPICE equivalent circuits or as S-parameter data. In this paper, the chip and board models are spatially-distributed but electrically pin-grouped two-terminal models.

To judge system-level PDS performance, the frequency dependent input impedance at the chip-package domain boundary (C4 bumps) will be examined as a primary criterion. We have divided the paper into four states depending on how much information is available to the designer.

- In **state 1** both the chip and board information is unavailable. The chip is modeled as an open circuit and the board as a small 5mΩ resistor, as shown in Figure 2.A.

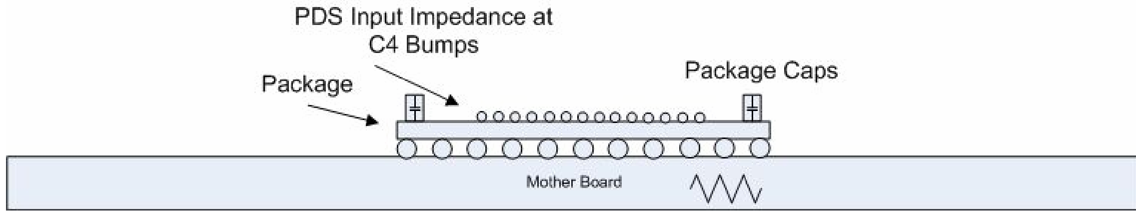


Figure 2A: State 1: No chip or board data available

- In **state 2** the die information is unavailable but the board information is available. The die is modeled as open circuit and the board is represented by its s-parameters (broad band SPICE circuits could also be used), as shown in figure 2B.

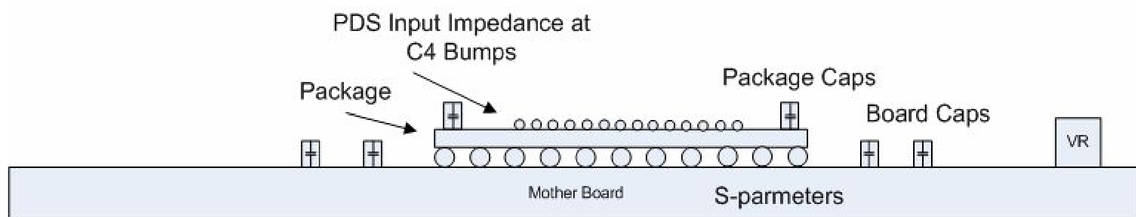


Figure 2B: State 2: Chip data unavailable, board data available

- In **state 3** the chip information is available but the board information is not available. The chip is then represented by its equivalent SPICE circuit (any commercially available on-chip extractor tools can be used) and the board is represented by a 5mΩ resistor, as shown in figure 2C.

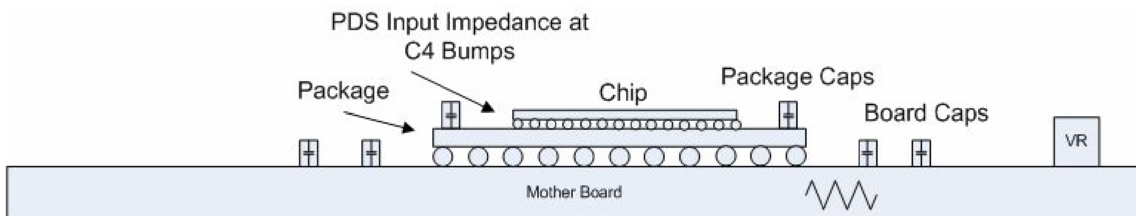


Figure 2C: State 3: Chip data available, board data unavailable

- Finally, in **state 4**, both the chip and the board data are available. The chip is represented by its equivalent SPICE model and the board is represented by its s-parameters.

The impedance of the PDS is examined at each of the four states. This would show us the impact on the package PDS implementation in the absence of reliable system-level information from the system design partners.

PACKAGE AND DECOUPLING CAPACITORS DESCRIPTION

The package used in this study has 12 layers. The power rail of interest has 44 decoupling capacitors on the package. Of which, 14 are 0805 4.7uF, 14 are 0306 2.2uF and 16 are 0402 2.2uF, as shown in Figure (3). The colored squares in figure 3 indicate the original placement of the decoupling capacitors. This configuration of the decoupling capacitors is referred as original decoupling design, and used as performance and cost baseline to compare with all of the optimized decoupling implementations.

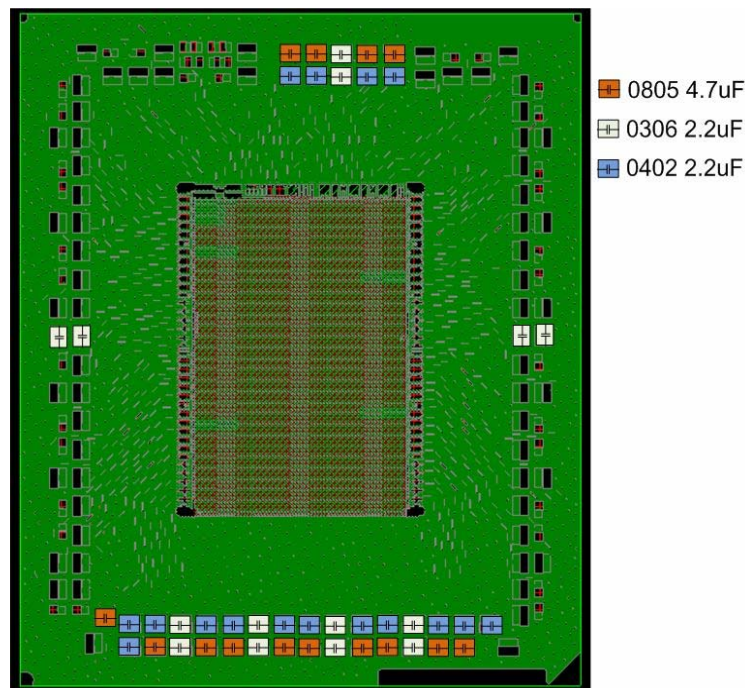


Figure 3: Original capacitor placement on package

In order to achieve better impedance with lower cost, in addition to the original 3 decaps used in the pkg design, we added the following 2 alternative decaps

- 1uF, 0306
- 1uF, 0402

As shown in Figure 4, the decap library now has 5 decaps. Capacitor #1- #3 are original capacitors in the package design. Capacitors #4 and #5 are alternative capacitors for optimization. The capacitors are represented by their equivalent SPICE circuits in the simulation. Compared with the original decaps, the alternative decaps have smaller capacitances, different self-resonance frequencies, and cost less. The cost information shown is scaled by a factor x, to protect proprietary capacitor pricing information.

ID	Part No.	Unit o...	Size	Model Type	Cnom (nF)			Component Cost
1	C0306_2_2uF	English	0306	SPICE Model	2200			6.92 * X
2	C0402_2_2uF	English	0402	SPICE Model	2200			4.65 * X
3	IDC0805_4_7uF	English	0805	SPICE Model	4700			30.33 * X
4	C0306_1uF	English	0306	SPICE Model	1000			2.548 * X
5	C0402_1uF	English	0402	SPICE Model	1000			X

Figure 4: Original and alternative decaps

PACKAGE PDS OPTIMIZATION CONDITIONS

We used Sigrity's OptimizePI as the optimization engine for the PDS. In the simulation:

- The board PDS design information is represented by an s-parameter file connected to the BGA pads on the bottom layer of the package or a 5mΩ resistor.
- Available die PDS information is represented by an equivalent SPICE circuit or by an open circuit at c4 bumps.

The optimization conditions are set as follows

- Optimization frequency range 10KHz – 1GHz
- Optimization criteria: best performance for a given cost, which means find the decap implementation that results in the lowest impedance at a given cost
- Optimization cost range: 35% - 105% of the original cost.
- Alternative capacitor rules: each original capacitor on the pkg can be replaced with any capacitor of same or smaller size from the capacitor library.

A state-independent target impedance is applied based on the original design performance, with a lower bound of 1mΩ. It is also possible to put a target or threshold Z(f) in the optimizer to limit the number of outputs from the optimizer and to set a certain performance as the optimization criterion. Another way is to give it a cost constraint to get decoupling solutions (this is the path we choose for this paper). It is also possible to constrain for both cost and performance.

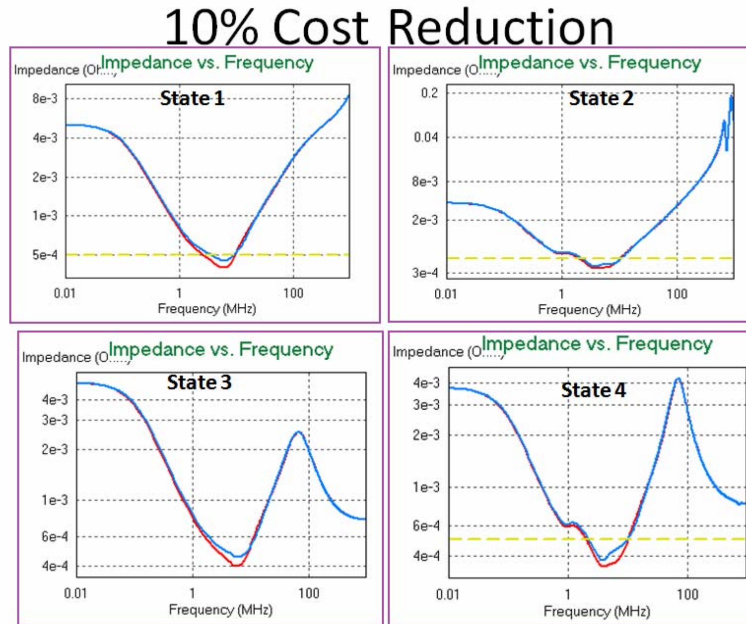
OPTIMIZED IMPEDANCE AT REDUCED COST

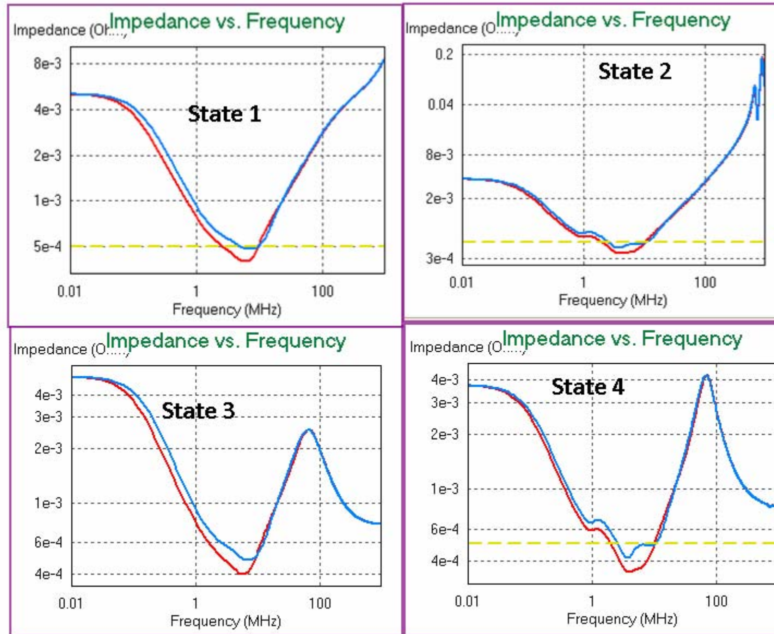
For each state, the optimization simulation outputs many alternative decoupling design schemes in the pre-specified cost range. Each scheme represents the lowest impedance at a given cost. For each scheme, we have the corresponding

- Cost.
- Impedance profile.
- Number of capacitors and their placement.

After analyzing the optimization results we found that, within the constraints described in the previous section, we could not get lower cost and better performance at the same time. That is due to the fact that there are only 2 alternative capacitors in the library. However, in some cases, the impedance degradation is small for even for substantial cost savings.

The plots in figure 5 show the impact of the cost reduction effort on the impedance profile for 4 different states. The red curve in each plot is the impedance profile for original capacitor implementation, while the blue one lowest impedance profile with 10%, 30% and 50% cost reduction. These are plotted for each of the four states.





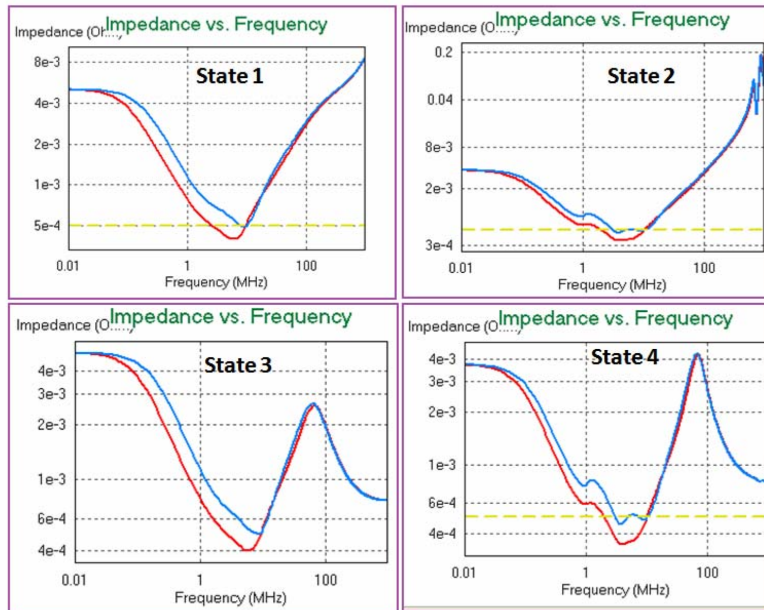
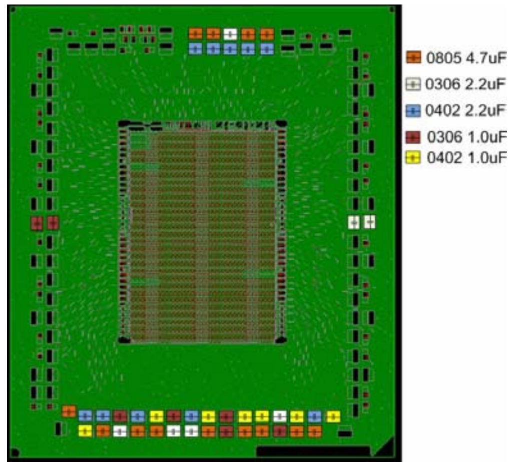
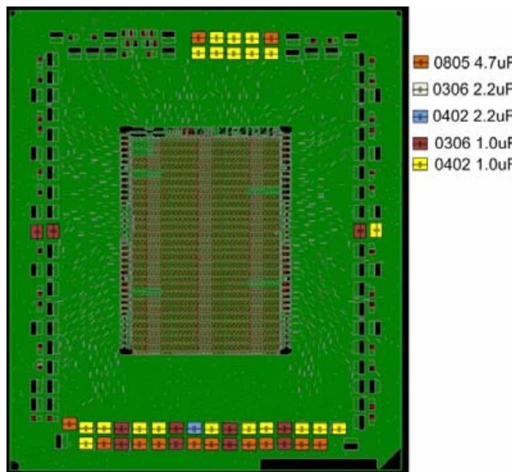


Figure 5: Impact of capacitor reduction on Z-profile for different states

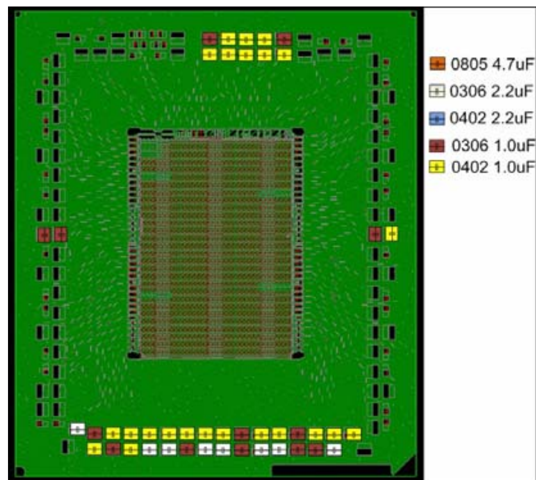
The color coded capacitor placement maps for state 4 are shown in Figure 6.



(a) 10% cost reduction



(b) 30% cost reduction



(c) 50% cost reduction

Figure 6: Capacitor placement maps for state 4 optimization

Figure 7 shows the distribution of the number and type of capacitors for different cost savings. The x-axis in the figure represents the cost savings where 0% is the original scheme and 10% is 10% savings compared to original scheme and so on. The Y-axis is the capacitor count.

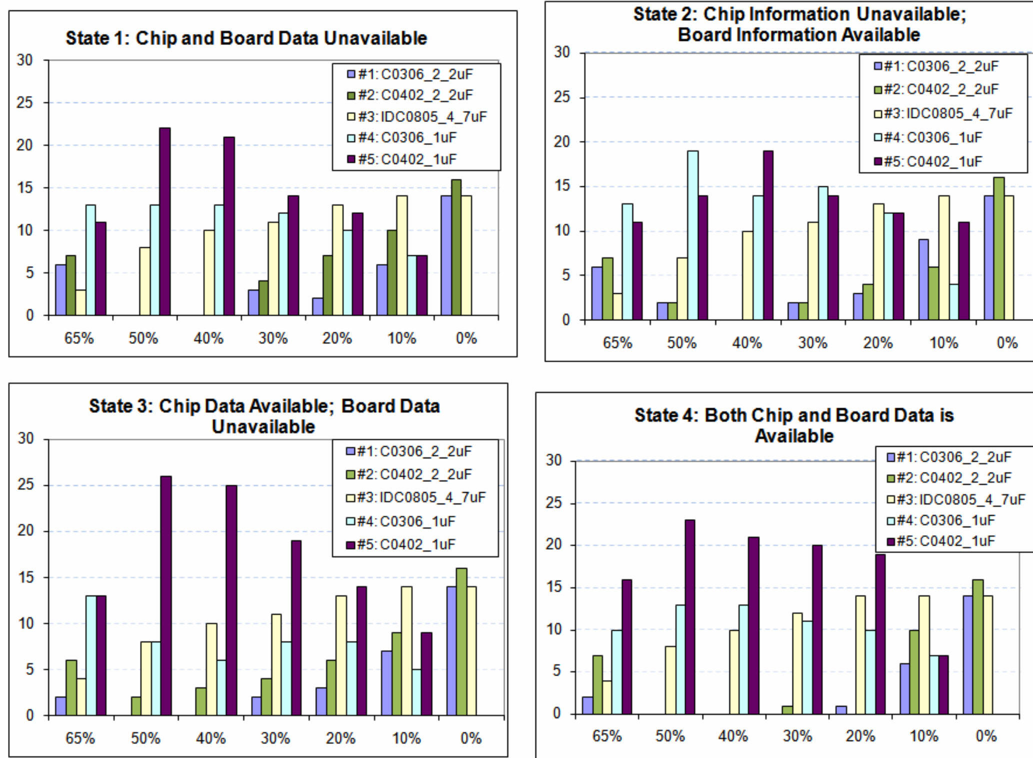


Figure 7: Distribution of capacitor types for different cost savings

OBSERVATIONS AND CONCLUSIONS

It can be seen that the cost reduction impact across the different states is pretty constant, in this case, and only the portion of the impedance profile attributed to the DSCs changes. Thus if we consider the impedance profile as the main design criterion for the PDS then even approximate models of the die and platform can put us on the right path for the design. As we see in this case even designing the DSCs and package in state 1 and 2 would give results that would be good enough for a direction check and lead in the right way. The state 4 design would obviously still be the most accurate.

We optimized the package PDS for each of the four system-aware states in sequence. Four characteristics were examined for the optimization: performance, capacitor count, area and cost. Since we started with a basic capacitor configuration we focused on cost as the main optimization target. In each design state whether the complete chip and board information is available or not, using an optimization engine quickly gives a number of solutions from the available capacitor library to pick a cost effective one. Figure 7 summarizes the capacitor distribution for different ranges of cost savings for the four states mentioned earlier. It can be seen from the charts that for all the states the optimizer tries to reduce the use of the most expensive capacitor (0805) and tries to use

more of the cheapest capacitor (0402- 1uF). This kind of data would give the package PD designer information on which capacitor to select and which to avoid in order to meet the Z requirements at the minimum cost. Lastly this type of analysis is based purely on the frequency domain simulations and it would be prudent to verify the final solution in the time domain too.