

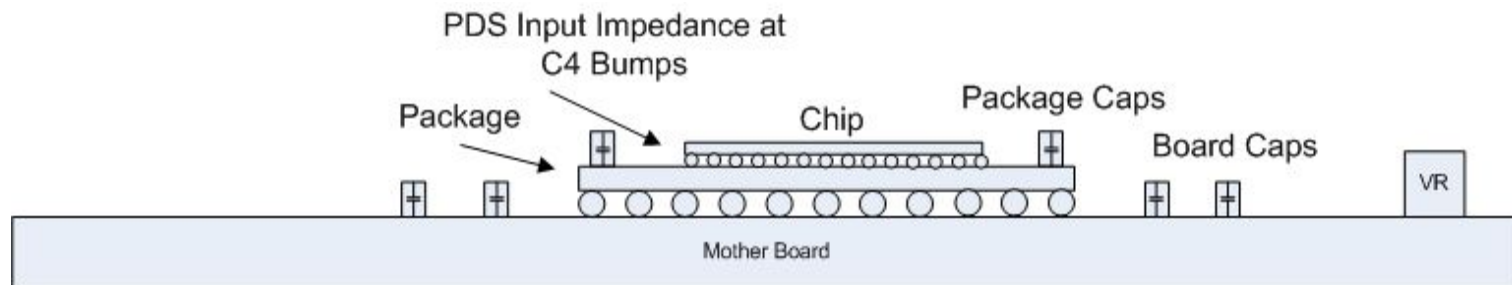


The Effects of Chip and Board Behavior on Package-Centric, System-Aware Power Delivery Design

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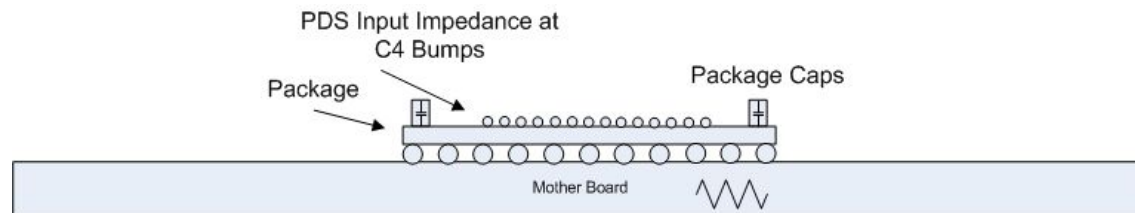
Overview

- Power delivery design impacts performance and SI.
- Package centric power delivery system design.
- Quantity and quality of chip and board data changes.

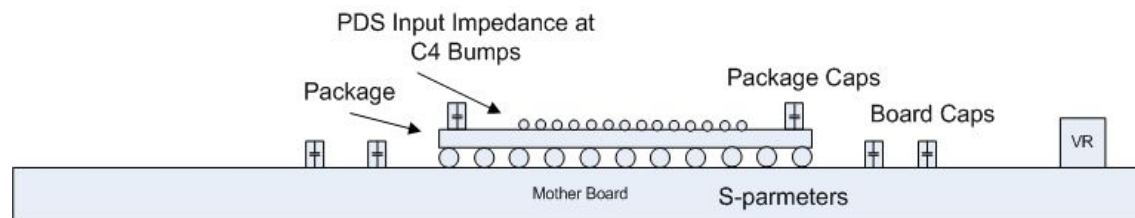


Different States of PD Design Examined

- **State 1: No info available for either chip or board.**
 - Chip is modeled as OC.
 - Board is modeled as a small resistor

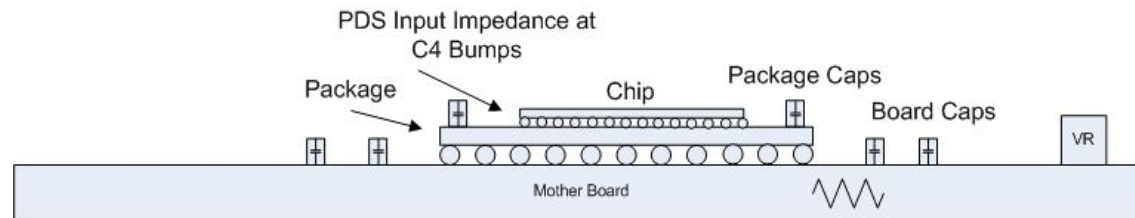


- **State 2: Chip info not available; board info available.**
 - Chip is modeled as OC
 - Board is represented by s-parameters

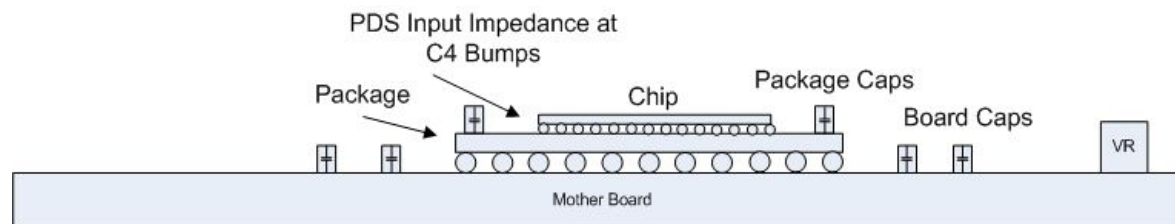


Different States of PD Design Examined (cont'd)

- State 3: Chip info available board info not available.
 - Chip is modeled as equivalent SPICE ckt.
 - Board modeled as small resistor.

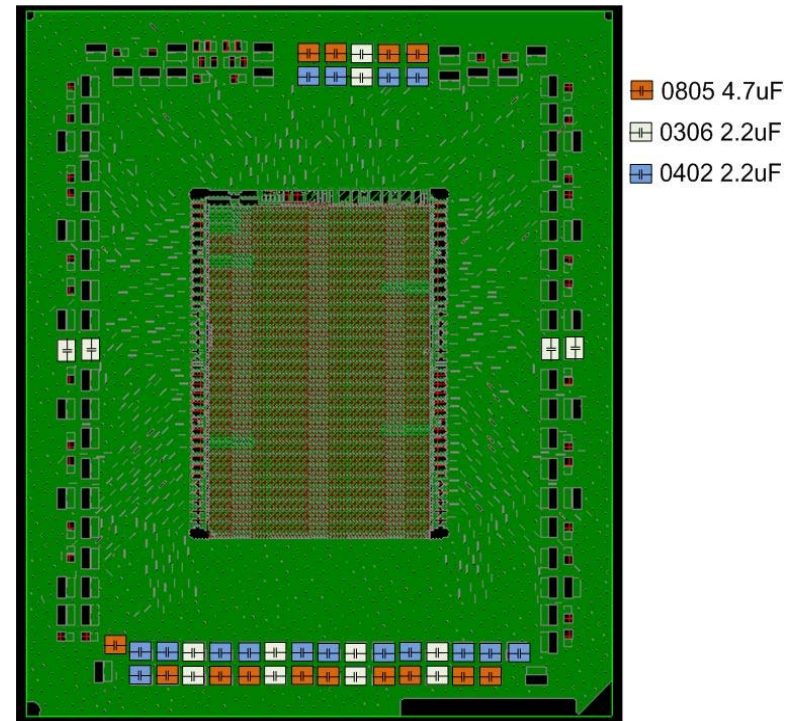


- State 4: Both chip and board info available.
 - Chip is modeled as equivalent SPICE ckt.
 - Board is represented as s-parameters.



Test Vehicle Description

- 12 Layer package
- 44 Decoupling capacitors
 - 14, 0805 4.7uF
 - 14, 0306 2.2uF
 - 16, 0402 2.2uF



- Additional decoupling capacitors considered
 - 0306 1uF
 - 0402 1uF

Decoupling Capacitors Used for Optimization of $Z(f)$

ID Δ	Part No.	Unit o...	Size	Model Type	Cnom (nF)		Component Cost
1	C0306_2_2uF	English	0306	SPICE Model	2200		6.92 * X
2	C0402_2_2uF	English	0402	SPICE Model	2200		4.65 * X
3	IDC0805_4_7uF	English	0805	SPICE Model	4700		30.33 * X
4	C0306_1uF	English	0306	SPICE Model	1000		2.548 * X
5	C0402_1uF	English	0402	SPICE Model	1000		X

PACKAGE PDS OPTIMIZATION CONDITIONS

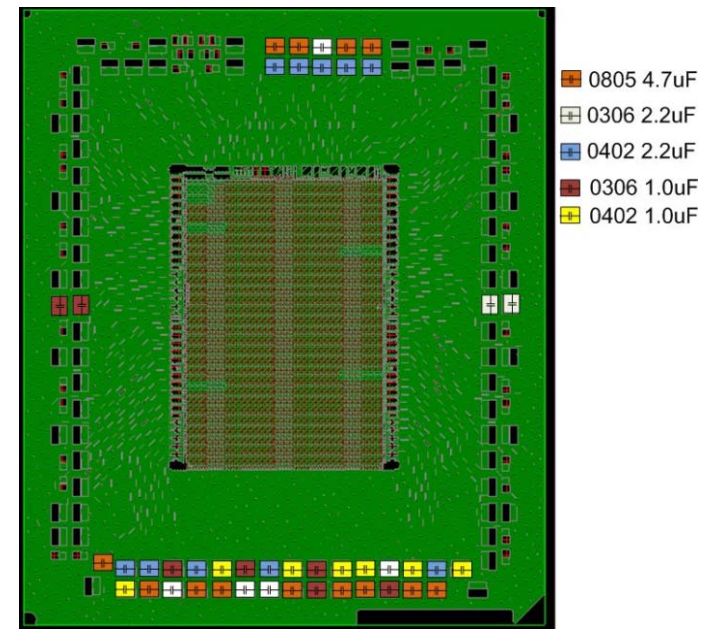
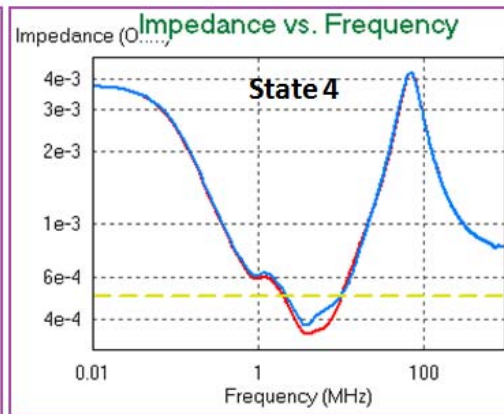
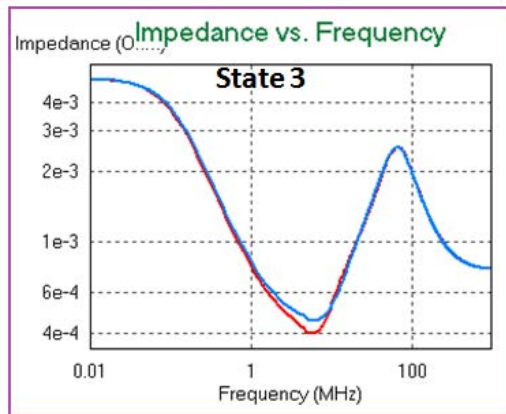
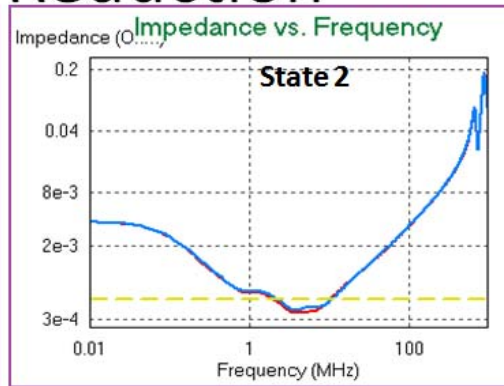
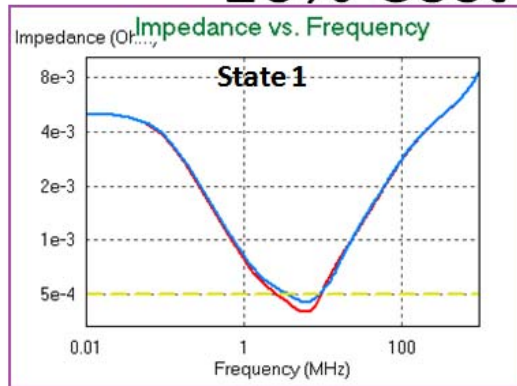
- Used Sigrity's OptimizePI for optimization.
- Optimization frequency range 10KHz to 1GHz.
- Optimization criteria: best performance for given cost.
- Optimization cost range: 35% - 105% of the original cost.
- Alternative capacitor rules: each original capacitor on the pkg can be replaced with any capacitor of same or smaller size from the capacitor library.
- Optimization target: $Z(f)$ of $1\text{m}\Omega$

OPTIMIZED IMPEDANCE AT REDUCED COST

- For each state we have
 - Cost
 - Impedance profile
 - Capacitor count, value and placement

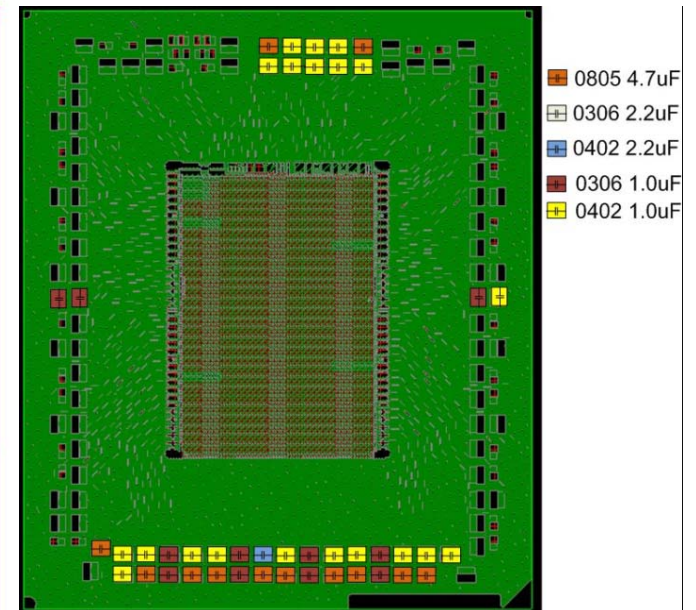
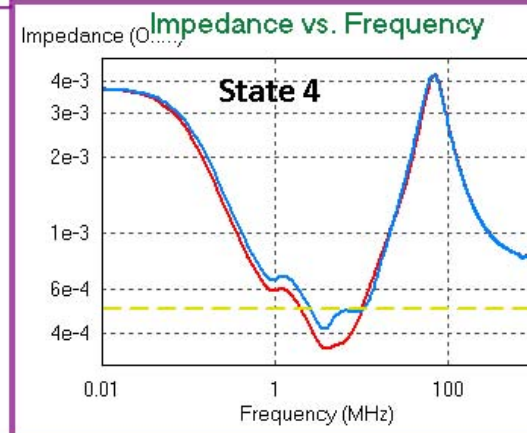
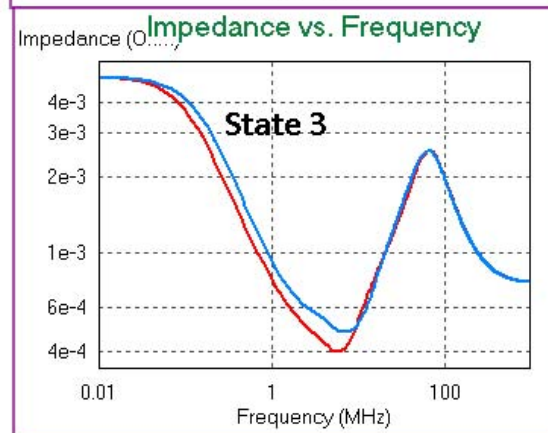
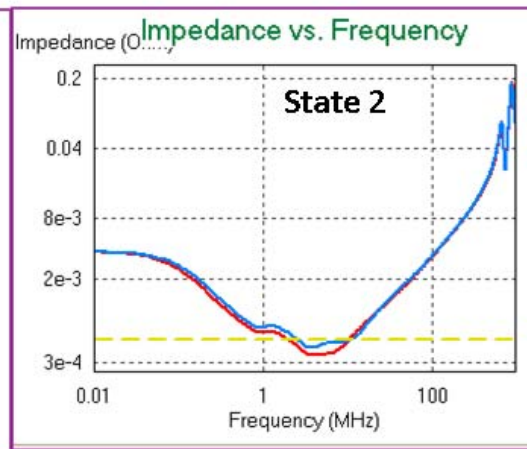
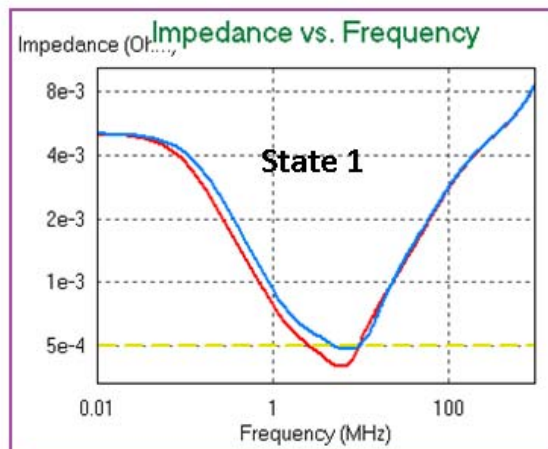
Optimized at 10% Cost Reduction

10% Cost Reduction



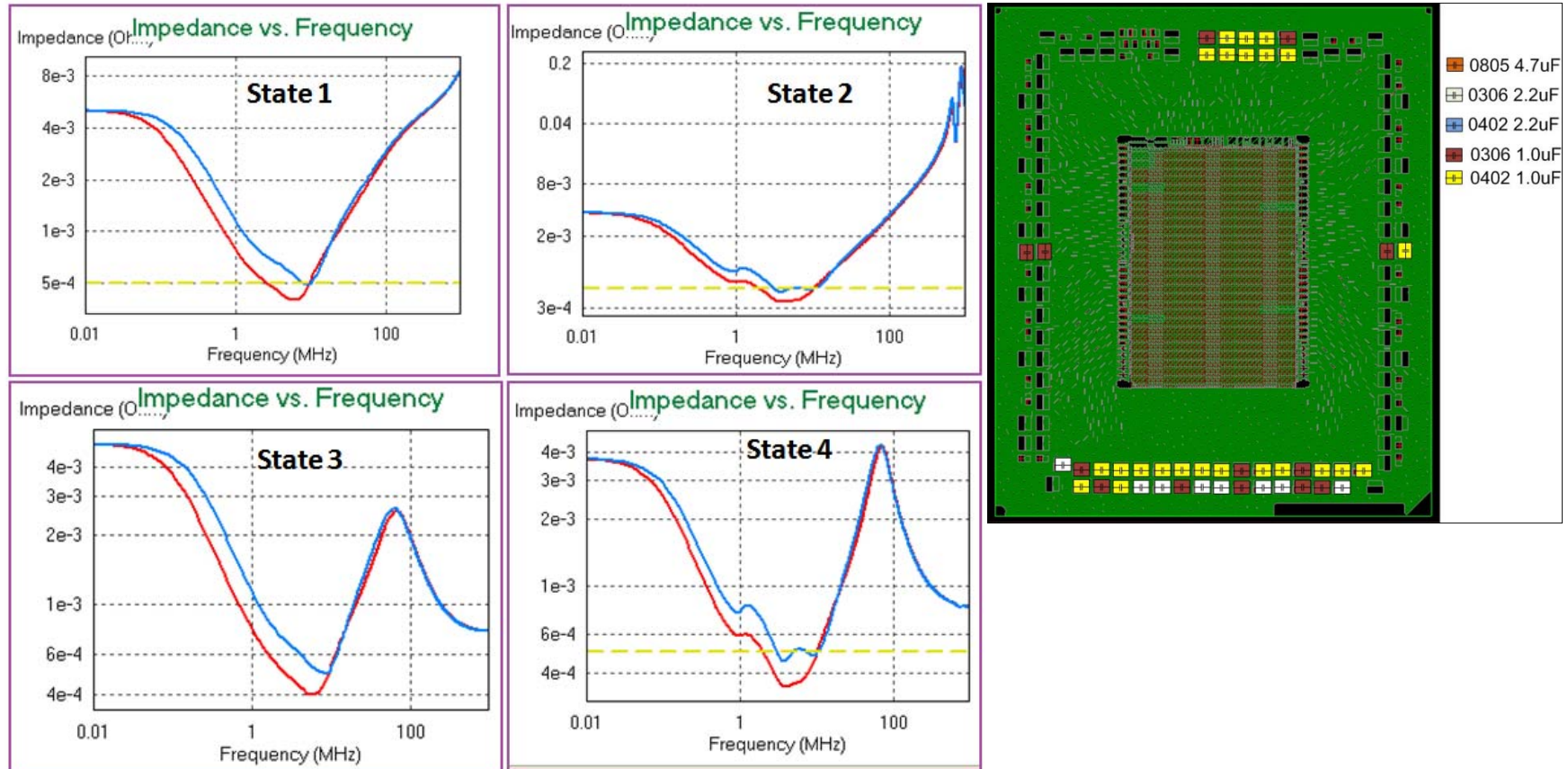
Optimized at 30% Cost Reduction

30% cost reduction

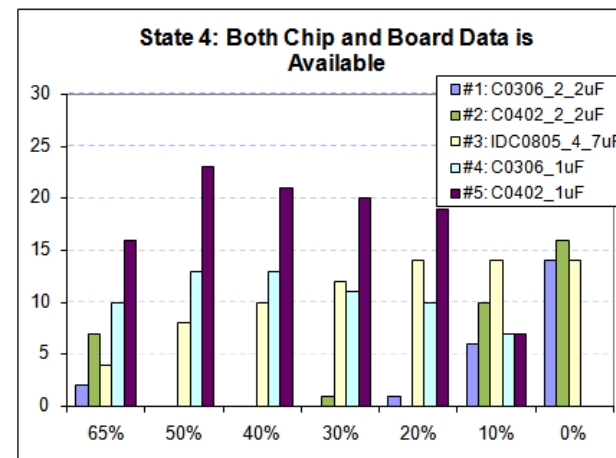
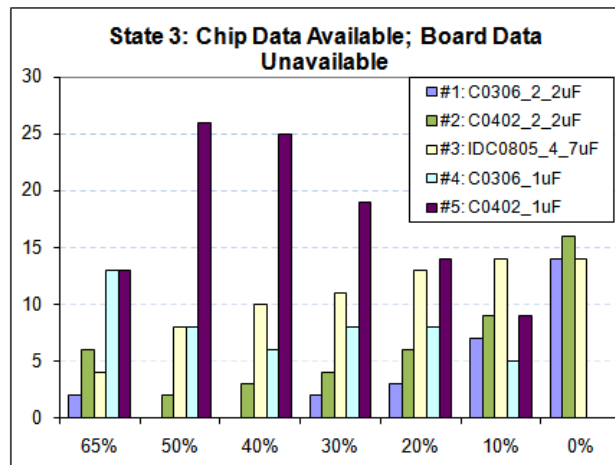
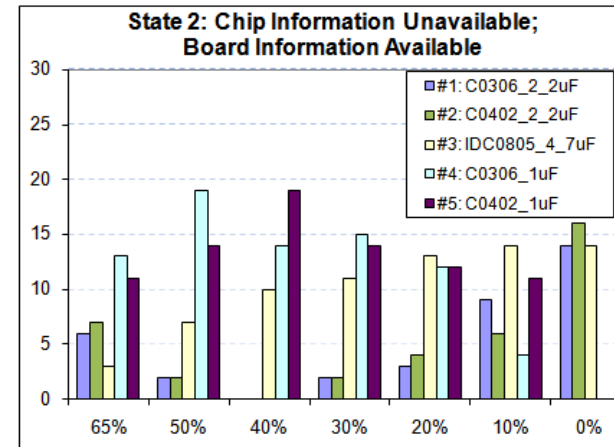
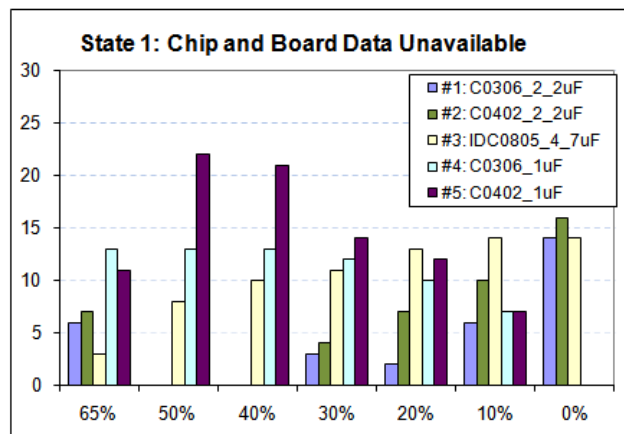


Optimized at 50% Cost Reduction

50% Cost Reduction



Capacitor Distribution for Cost Savings



Conclusions

- Impact of cost reduction on $Z(f)$ is pretty constant across different states.
- If $Z(f)$ is main design criteria then even approx models of chip and board put us on the right track.
- State 4 (both chip and board data available) gives the most accurate results.