Mobile Package Design and Simulations

21/March/2009

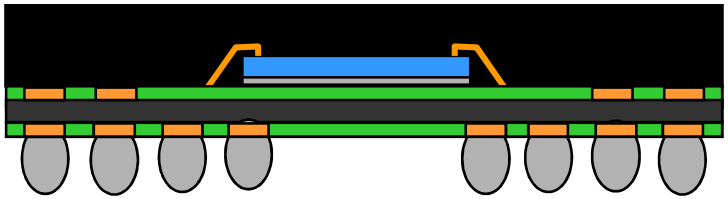
Applications

Smart phone market is fast increasing:

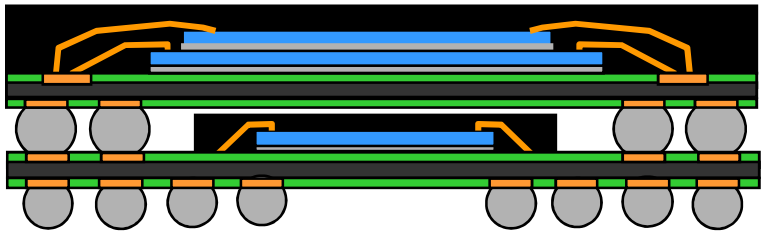
Technical challenges

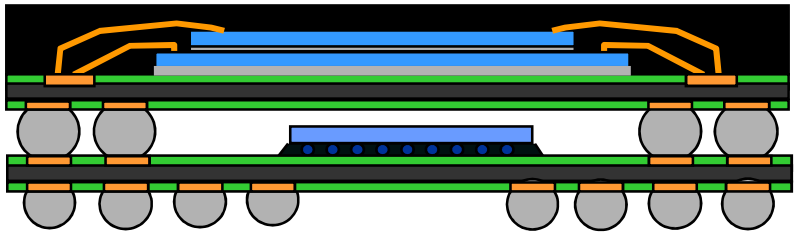
- Small Size
- Thin Height
- High-Performance

Packages

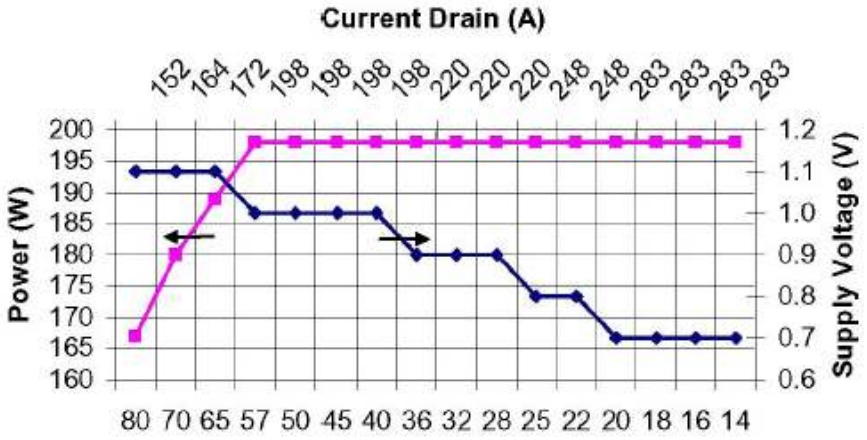


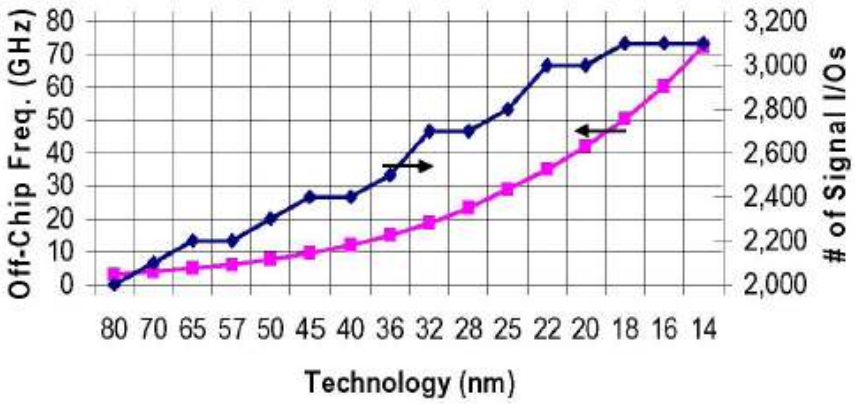
Discrete





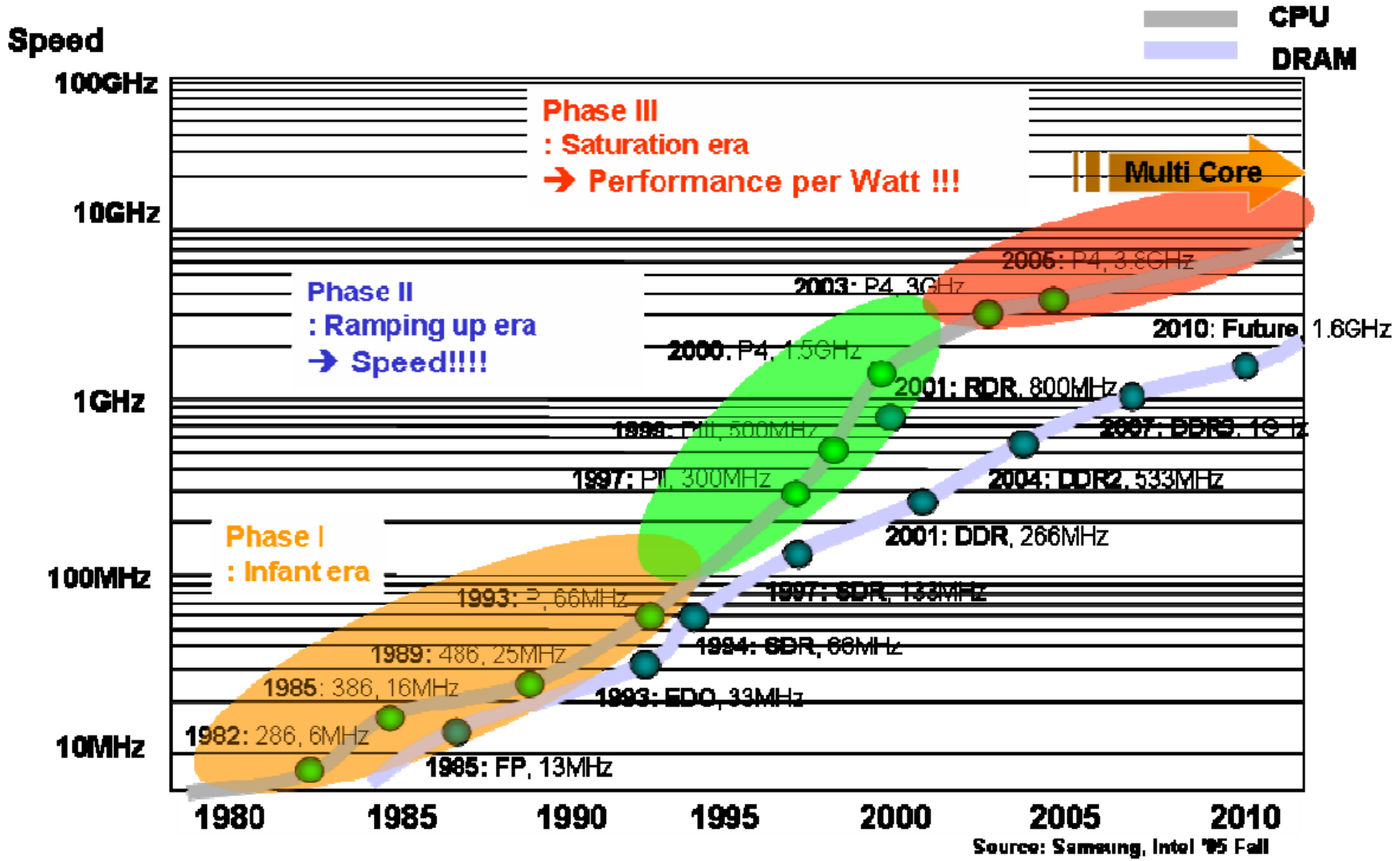
WB-POP & FC-POP



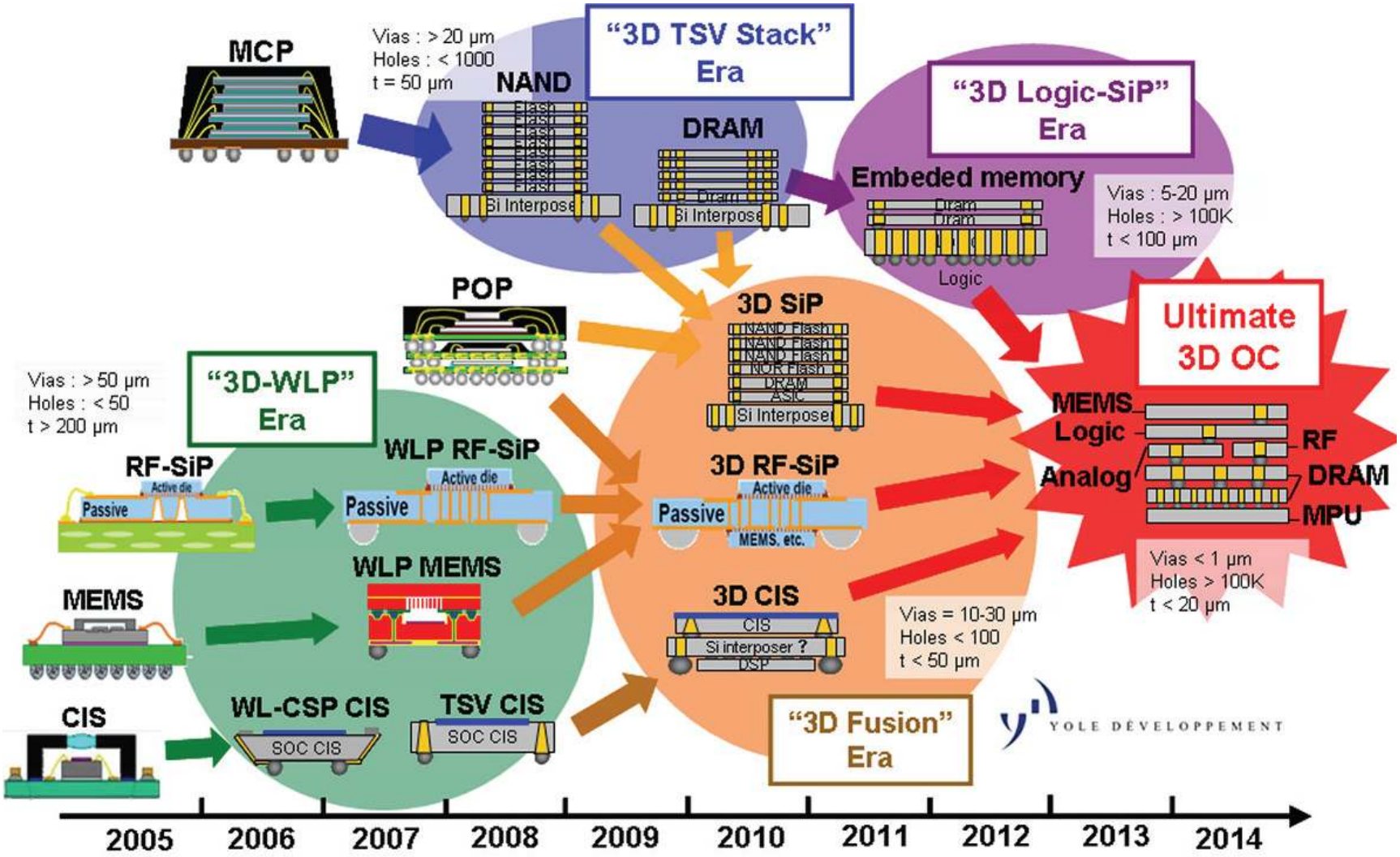


Muhannad S. Bakir, CICC, 2007

Packages – CPU VS DRAM



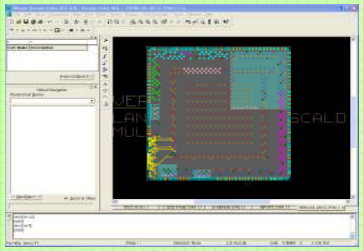
Packages Roadmap



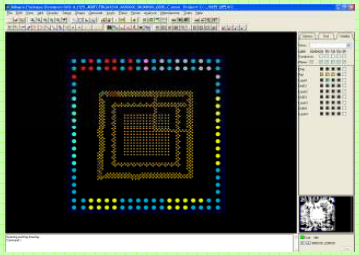
ITRS 2007 (ASSEMBLY AND PACKAGING)

Package Design Flow

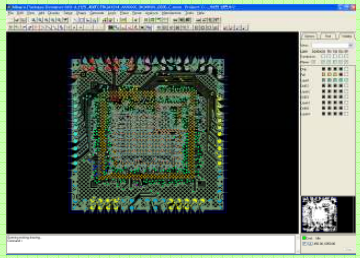
Feasibility Study | **Initial Package Design** | **Package Design** | **Simulation**



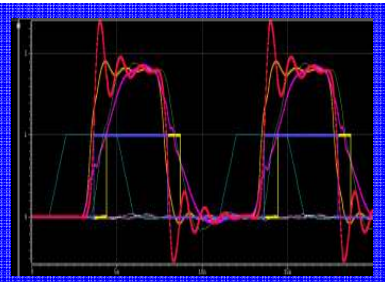
- Basic Package Structure & Possibility Check



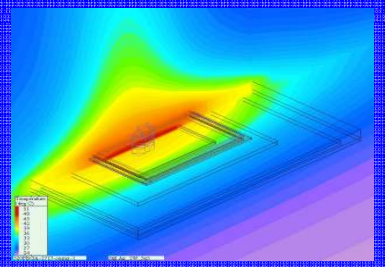
- SI/PI/TI Review



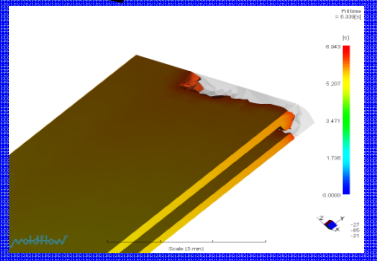
Design Fix



Electrical

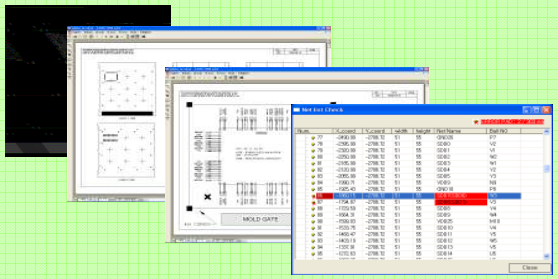


Thermal



Mechanical

DFM Review



- Manufacturing Specification

Design/Simulation Flow

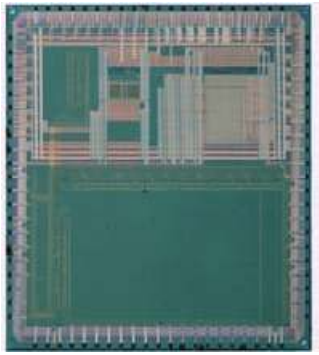
Exploratory stage
- Feasibility Exploration

Initial Design Stage
- Understand Devices
- Decide package technology

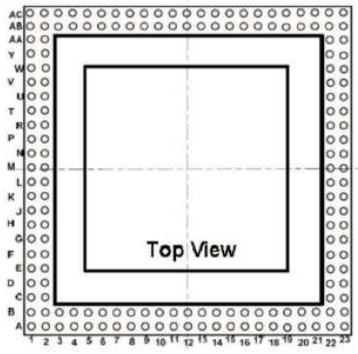
Design Iteration Stage
- Package layout completion

Design Closing Stage
- Manufacturing reviews

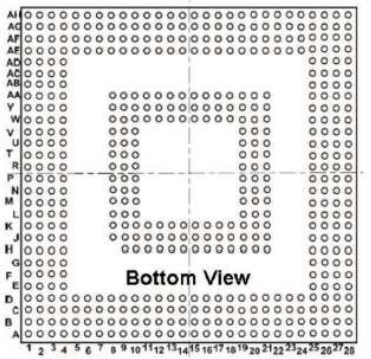
PCB Order



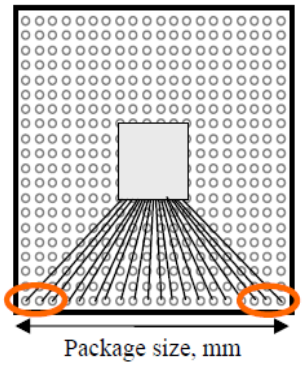
Floor-Planning



Top Package

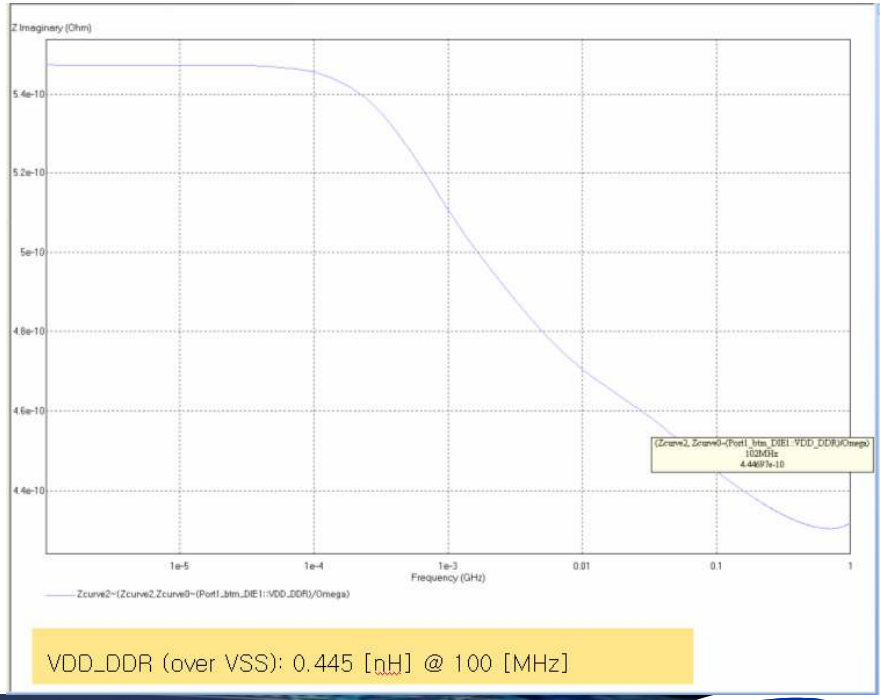


Bottom Package

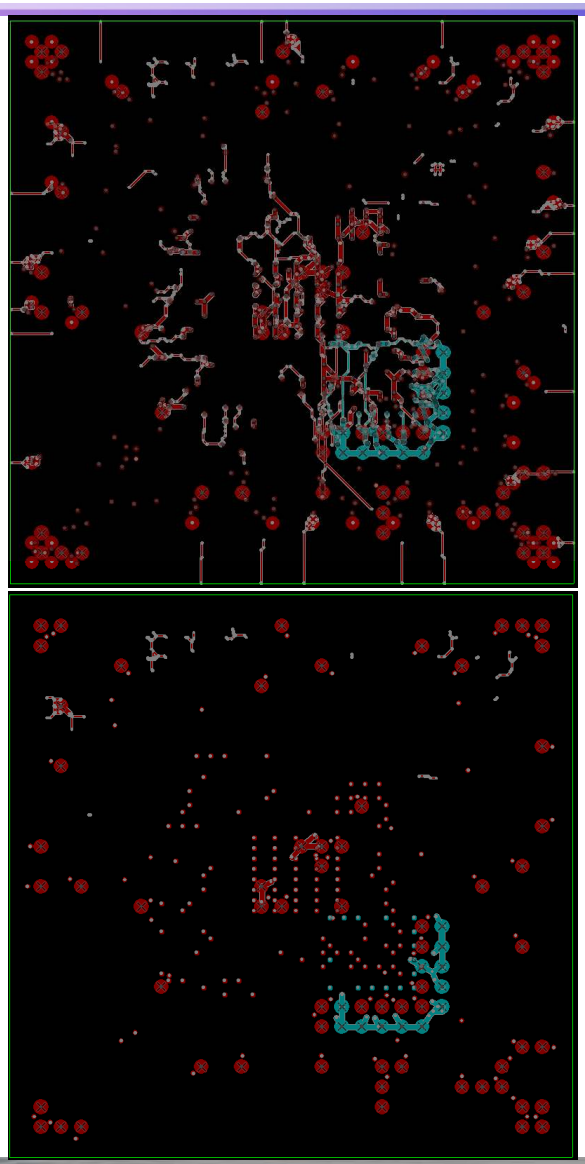


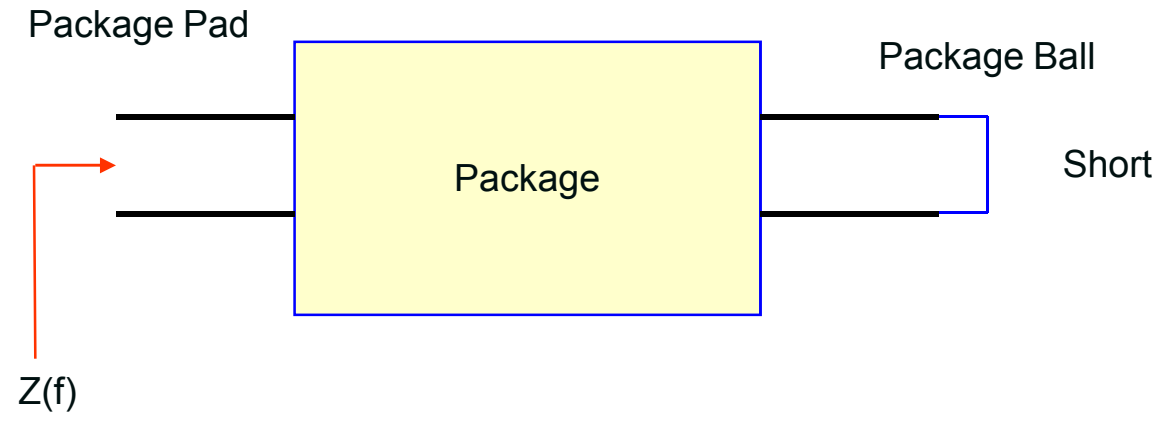
Initial routings

Netlist	R [Ohms]	L [nH]	C [pF]
DDR_DM0	1.71433E-01	2.57537E+00	5.74586E-01
DDR_DM1	2.73357E-01	4.41767E+00	6.96277E-01
DDR_DQ1	2.16783E-01	3.91931E+00	6.89912E-01
DDR_DQ1	2.25670E-01	3.92604E+00	7.52607E-01
DDR_DQ2	2.14322E-01	3.69011E+00	7.90655E-01
DDR_DQ3	2.30514E-01	3.99220E+00	6.66244E-01

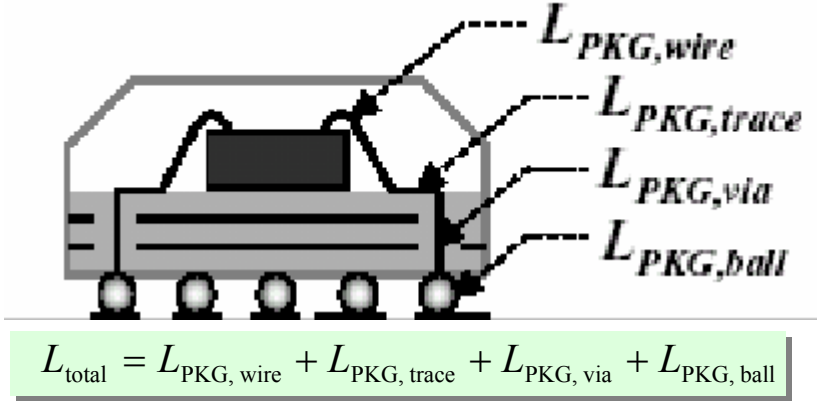


Power Delivery



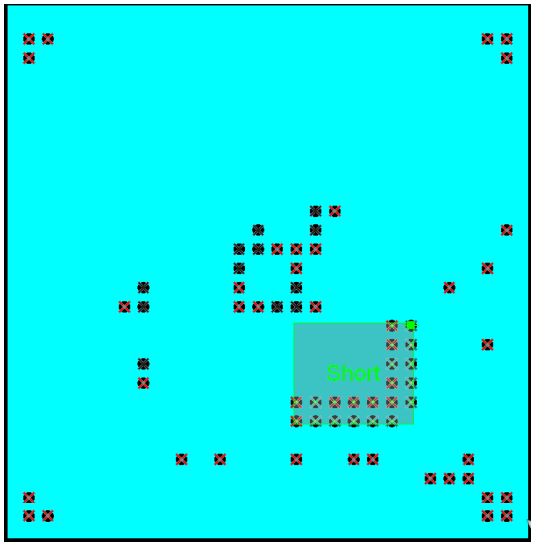


L(*f*)= Imag[Z(*f*)] / (2* π*f*)



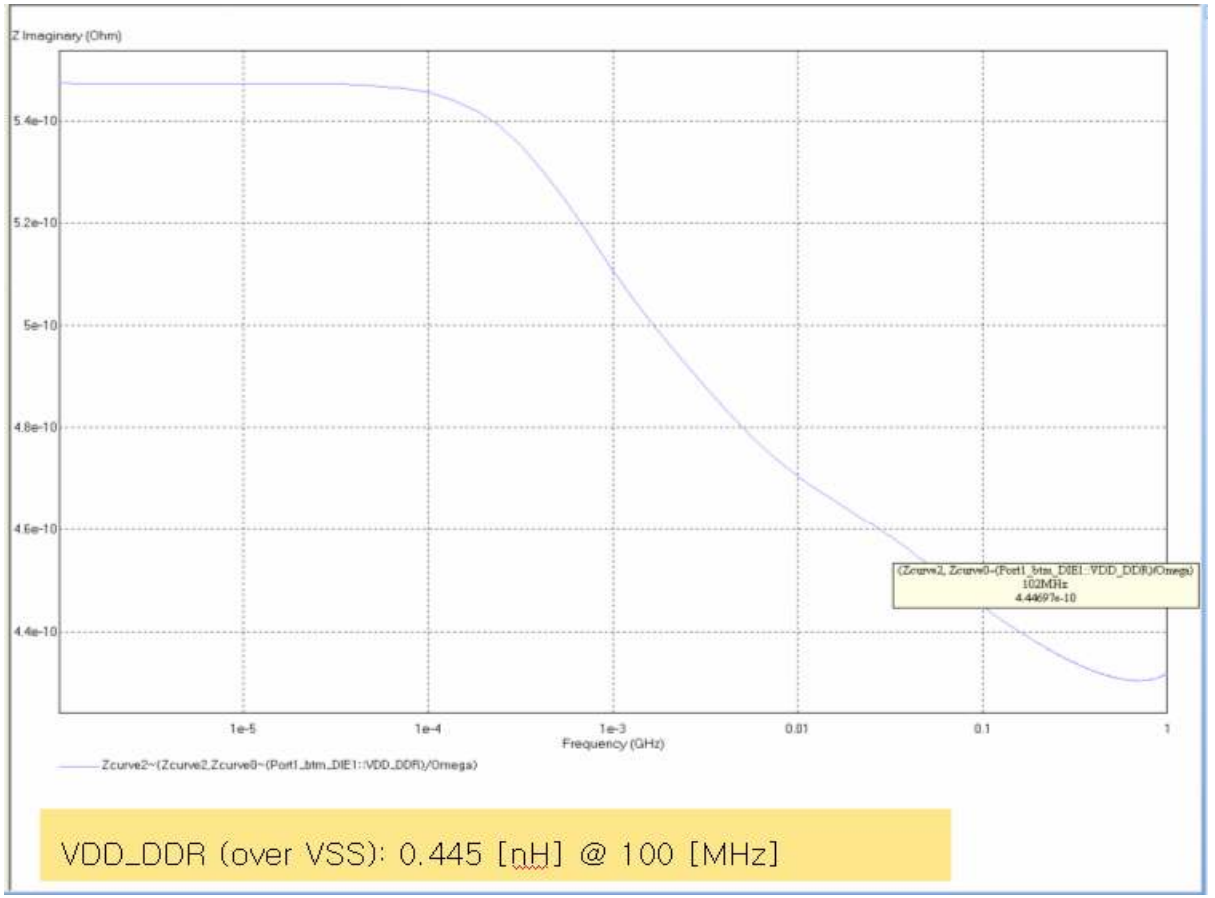
$$L_{total} = L_{PKG,\,wire} + L_{PKG,\,trace} + L_{PKG,\,via} + L_{PKG,\,ball}$$

Power Delivery [cont.]



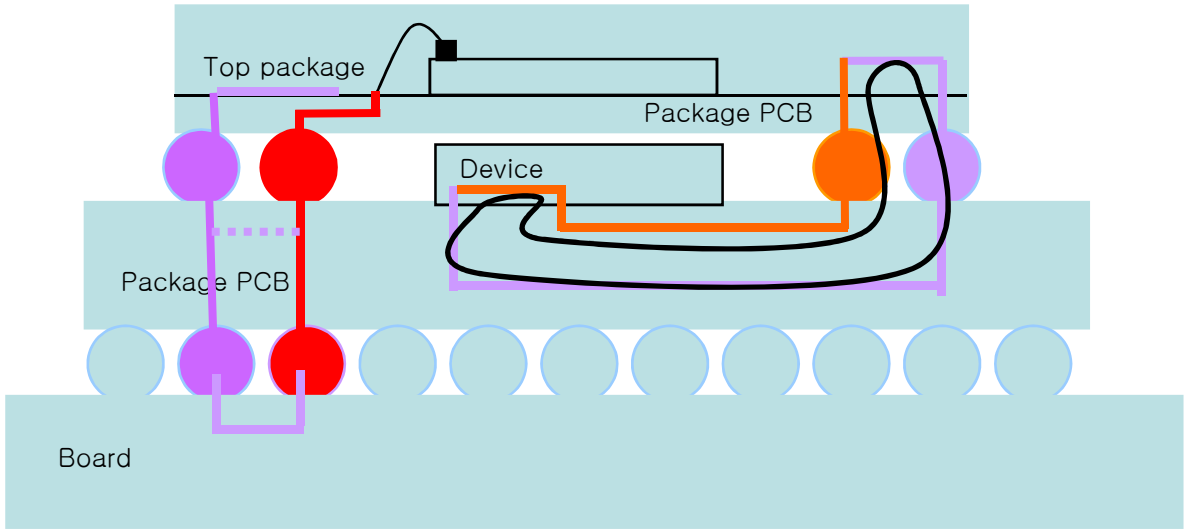
Layer Icon	Layer Na...	Thickness(um)	Conductivity(S/m)	Color	
	Signal$TOP	1.0000e+001	4.300000e+007		1
	Medium01	1.0000e+002			
	Signal$L...	2.0000e+001	5.959000e+007		1
	Medium$...	4.0000e+001			
	Signal$L...	1.8000e+001	5.959000e+007		1
	Medium$...	1.0000e+002			
	Signal$L...	1.8000e+001	5.959000e+007		1
	Medium$...	4.0000e+001			
	Signal$B...	2.0000e+001	5.959000e+007		1
	Medium0...	2.5000e+002			
	Signal01...	3.5560e+001	5.800000e+009		1

Total Thickness: 6.5156e+002 um



Design Rile: Minimization of Loop Inductances of each Signal &PWR/GND pins to minimize Inductive Noise

Power Delivery



Power delivery increases by optimizing grounds at bottom package.

Design	Inductance [nH]
Split Ground	0.24 ~ 0.9
Wider Ground	0.16 ~ 0.38

33 [%] Improvement (decrease)

Why S-parameter ?

- S-parameter
  - Relate to familiar measurements
    - Gain, Loss, Reflection Coefficient
  - Relatively easy to measure
  - Can cascade S-parameter of multiple devices to predict system performance
  - Can compute Z, Y, or H-parameters from S-parameters
  - Possible to convert to SPICE-compatible Network model

- Z, Y, and H-parameter
  - Hard to measure total voltage and current at DUT ports at high frequencies
  - Active devices may oscillate or self-destruct with shorts or opens

Double Data Rate (DDR) DRAM Design

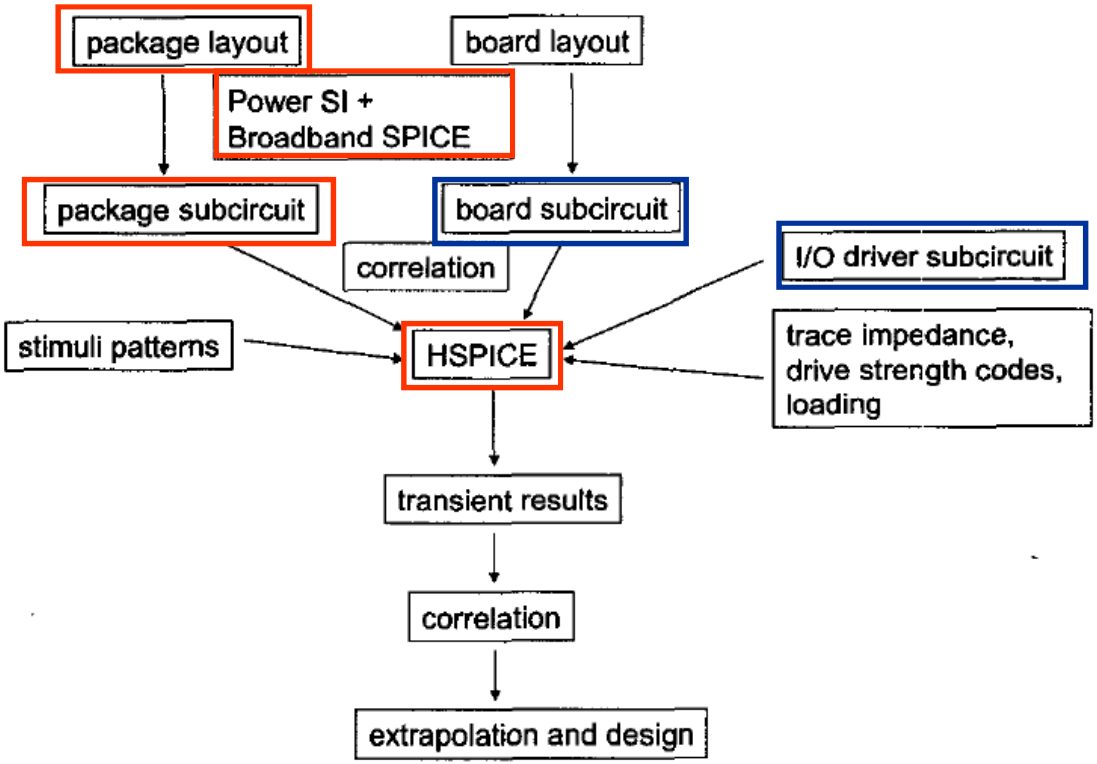


Figure 2. Flowchart of the analysis methodology.

Performance = f(Length from Die to System Board)

= f(Die Size, Package Size)

= f(Die Pitch, Package Pitch, I/O Counts)

Figure 9. The attributes that affect the package performance.

DDR(200,266,333,400 [Hz])

DDR2(400,533,667,800 [Hz])

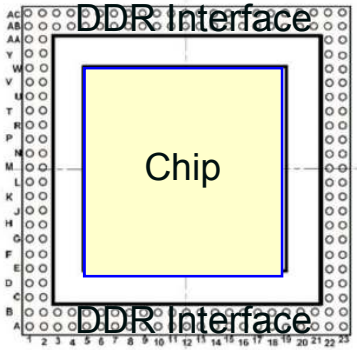
DDR3(800,1066,1333,1600 [Hz])

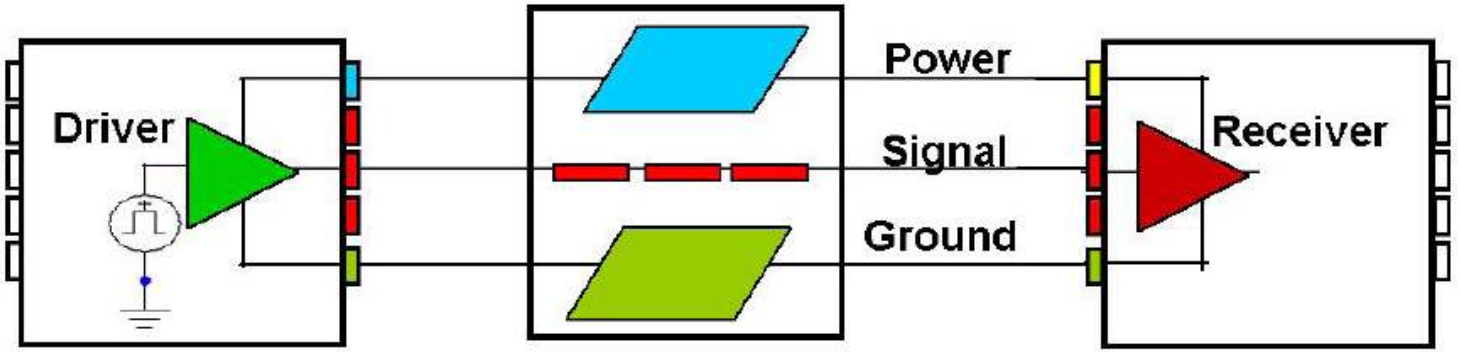
∴ Both IO count & Frequency increase

E. Chan, "High-Speed DDR Performance in 4 vs 6 layer FC-BGA package design," ECTC(2004)

Y. Wen, "The package bandwidth limitation of high-speed broadband products," ECTC(2001)

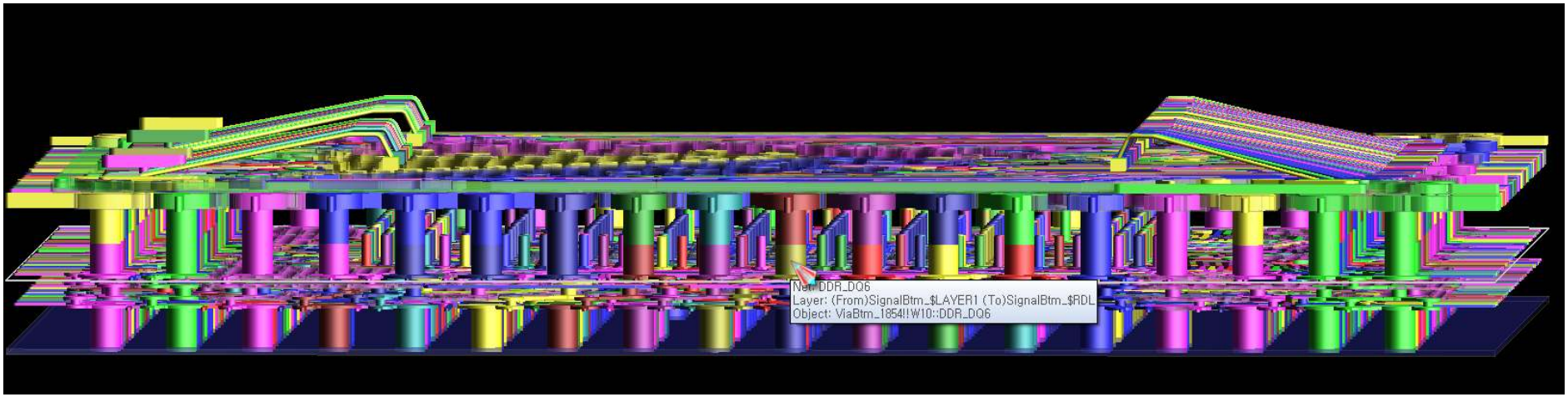
Double Data Rate (DDR) DRAM Design



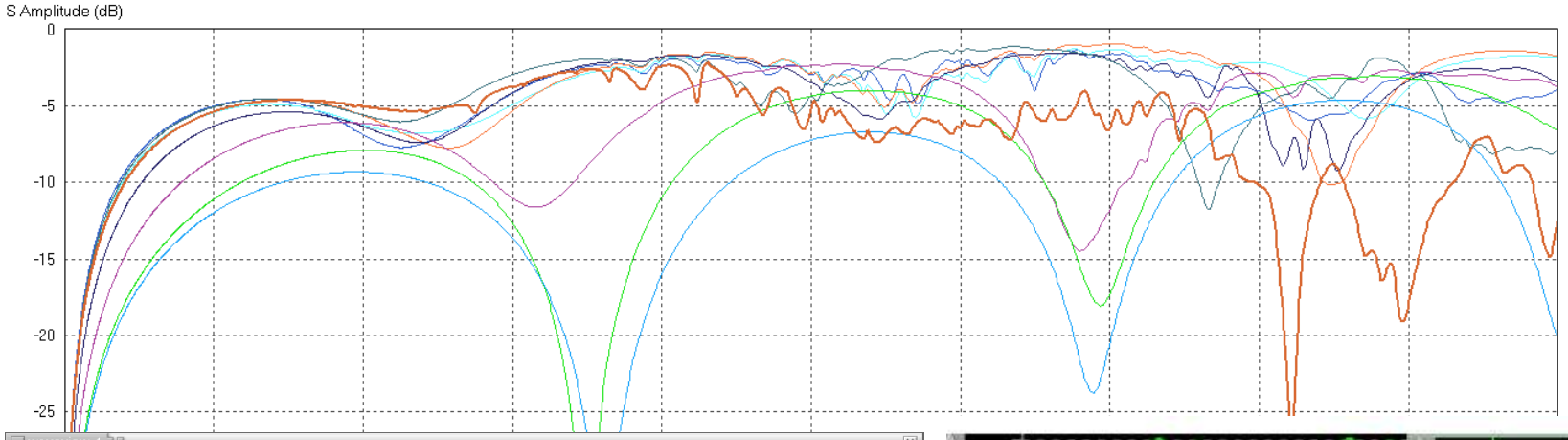


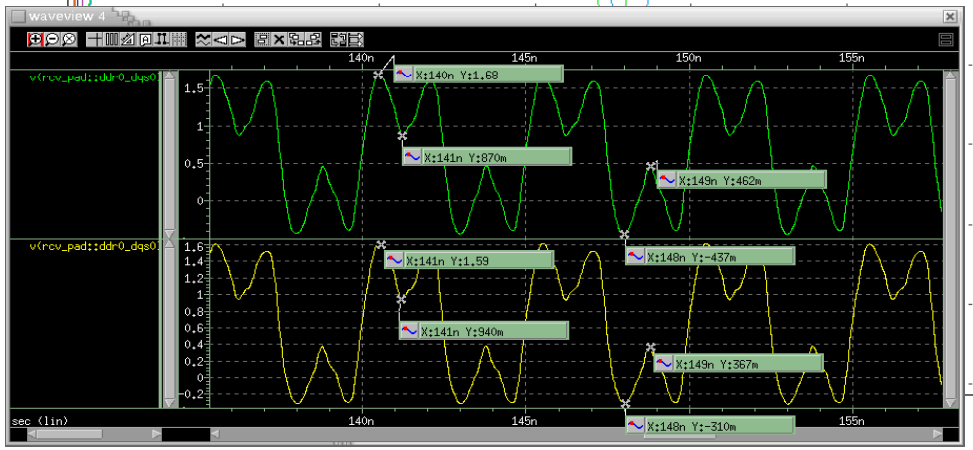
S-parameter(Top & bottom)

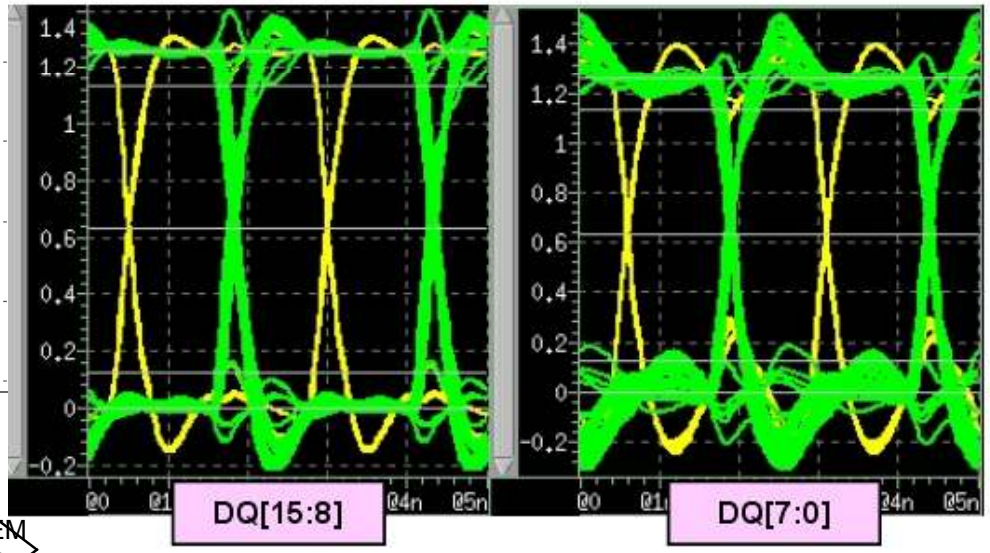
➔ Max. 200 ports (file size = 2 Gbyte)

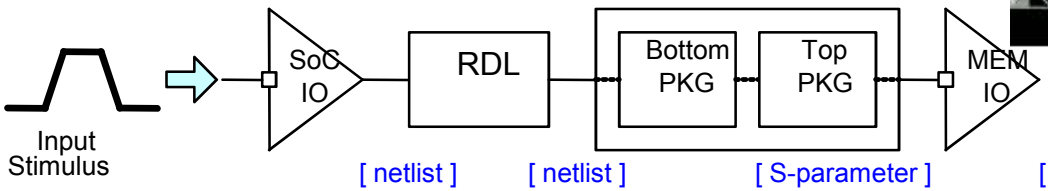


Double Data Rate (DDR) DRAM Design

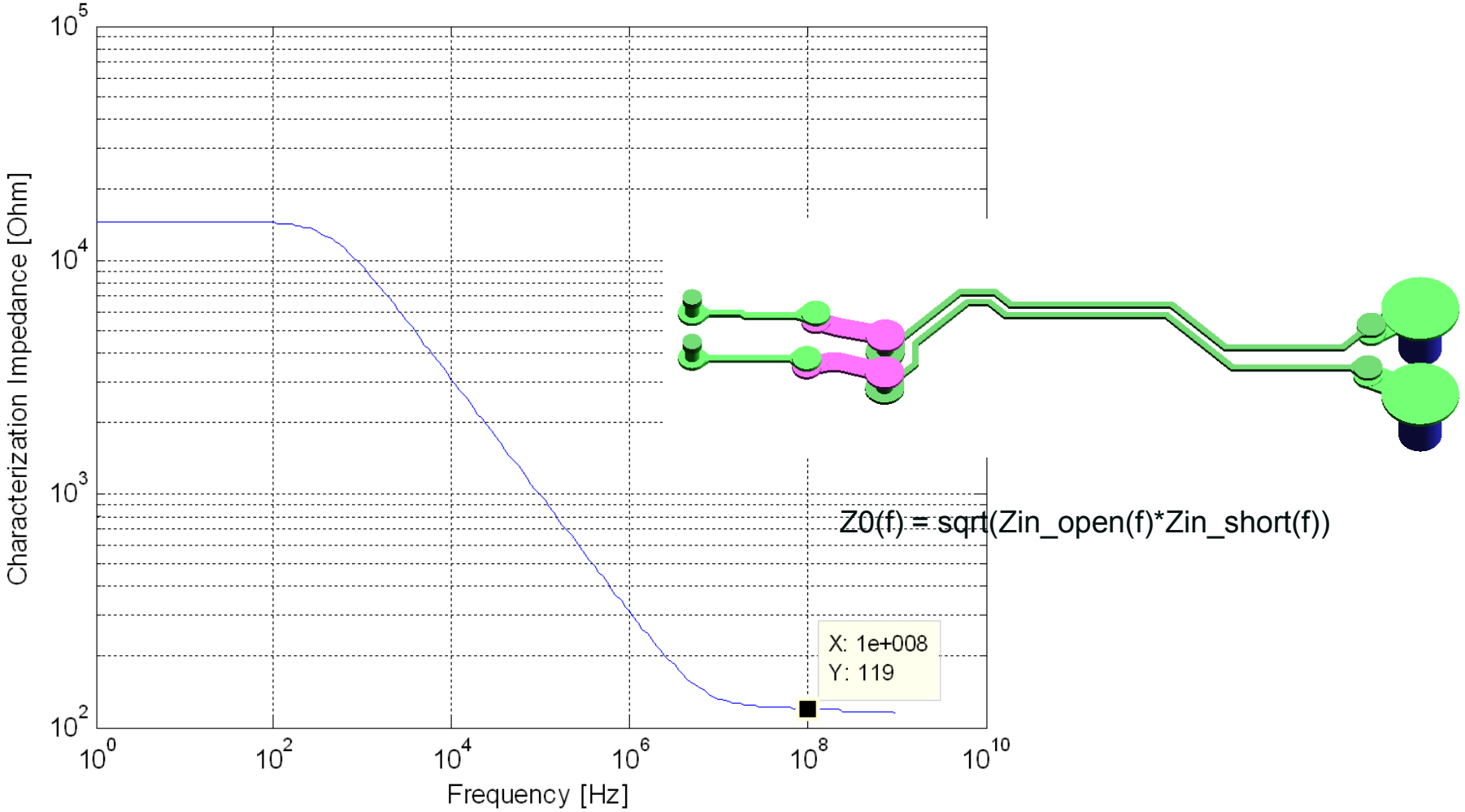








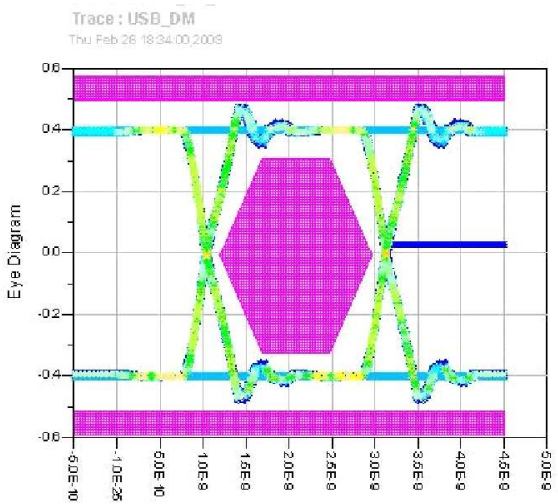
High-Speed IO Simulation

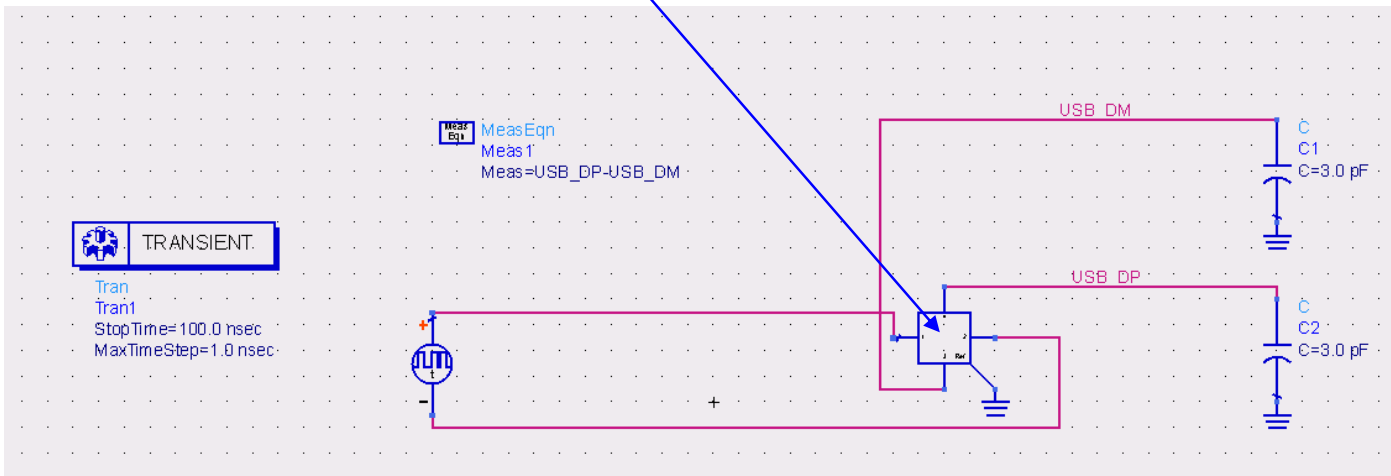


Z0(f) = sqrt(Zin_open(f)*Zin_short(f))

High-Speed IO Simulation

From PowerSI





Conclusions

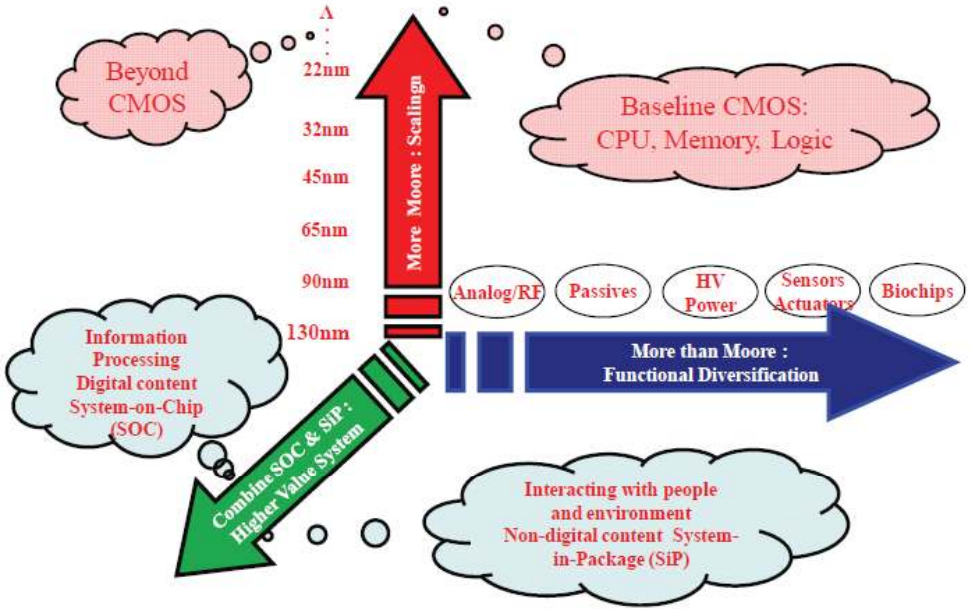


Figure AP14 Beyond CMOS Scaling

+ Package Technology

New opportunities & challenges. Hence Simulation tools, like PowerSI & Speed2000, are indispensable