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A novel methodology to handle the layout constraints for designing an optimal Power Delivery Network

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Abstract

PDN [Power Delivery Network] design flow includes optimization of the given network to meet a target which could be in frequency domain as Z(f) or in time domain as noise or jitter margin. Optimization faces many constraints such as KOZ [Keep Out Zone] limit, narrow power shapes and mesh like structure on the power planes. This paper provides a novel methodology to address these constraints, insights into how a mesh can significantly help a PDN and its limitations and also simulation and lab data are provided for designing a good reference plane.

Authors Biography

Praveen Pai is working as a power delivery design engineer with Intel India since 2005. He has an M.S. degree from Carleton University, Canada. His areas of interests include motherboard and package power delivery. Parthasarathy Ramaswamy obtained his Ph.D. degree from IISc., Bangalore, India and is working with Intel Technology India Pvt. Ltd., Bangalore. He is responsible for signal integrity and power-delivery solutions for the Mobile Platforms Hardware & Development group. His areas of interests include high-speed PKG/Board designs, power and signal integrity studies, etc. Julius Delino is a Principal Engineer at Intel Corp., where he is based at Folsom, CA. After graduating from San Diego State University, he did Electrical Design for Unisys Corp. (formerly Burroughs Corp.); working on mainframe computers. After 10 years, he joined Intel Corp., where he applied electrical design and analysis to 4-way servers, chipsets and, now, on next generation CPUs.

Section 1: Introduction

At Intel, we have been embarking on developing high end silicon and package solution with smaller footprint. This poses numerous challenges associated with real estate, flexibility in design etc. During the package design cycle there will be many changes to the assumed parameters like KOZ [Keep Out Zone], stack up etc which will affect the quality of the PDN [Power Delivery Network] designed. Efficacy of common perceptions a designer has during the package design are discussed and new insights into them are provided. This paper has a collection of three problems that were faced as part of product design cycle and tries to provide insights into each of them and possible mitigations. These mitigations have been verified on successful products and this paper provides an outline of them.

PDN design flow includes optimization of the given network to meet a target which could be in frequency domain as Z(f) or in time domain as noise or jitter margin. Designing our system to meet noise or jitter margins may be more complex compared to designing a network to meet a given Z(f). Since a Z(f) would finally translate to some noise or jitter we would translate a given noise target to Z(f) and design our network in frequency domain. This methodology is more intuitive in identifying the key parameters for optimizing the given design to meet the system performance. Key parameters to optimize the network include connectivity to capacitor pads, u-via count and their distribution, solid wide power corridors, good power and return path referencing. These parameters are varied to design the network for a given target impedance, noise or jitter margins. However while optimizing we hit upon many constraints, some of them are due to complexity in layout and sometimes due to manufacturing/assembly/testing driven design rule requirements. The following sections cover each of the problems and their mitigations.

Section 2: Effect of Power Mesh vs. Solid plane

Silicon driven constraints and shrinking package layers could result in bump pattern and package stack up as shown in Figure 1. For the stack up shown, it is evident that the signal routing takes place on 2F layer while power and ground plane routing is on 3F and 1F layers respectively. The signal routing on 2F is based on signal integrity requirements to have strip line routing for high speed signal traces. Figure 2 depicts one possible way of connecting power plane and the inner row of bumps. Please note that the connection to the power plane is through skinny traces as shown but conventionally a solid plane is preferred.

A solid plane offers very little resistance for the current flow. However a mesh would introduce a finite amount of resistance. Please refer to Figure 3 showing a typical PDN from VR [Voltage Regulator] to sink. The low frequency path extends from VR to sink as shown and the high frequency (AC) load demand is met by the HF path. Figure 4 shows the impedance seen from the sink towards the VR. Note that the LF impedance is relatively flat compared to HF impedance which shows a resonance behavior. This resonance is the result of inductance of the HF loop [L-loop] and capacitance [Cdie] of the silicon (Figure 3). Any resistance along the HF loop will dampen the resonance

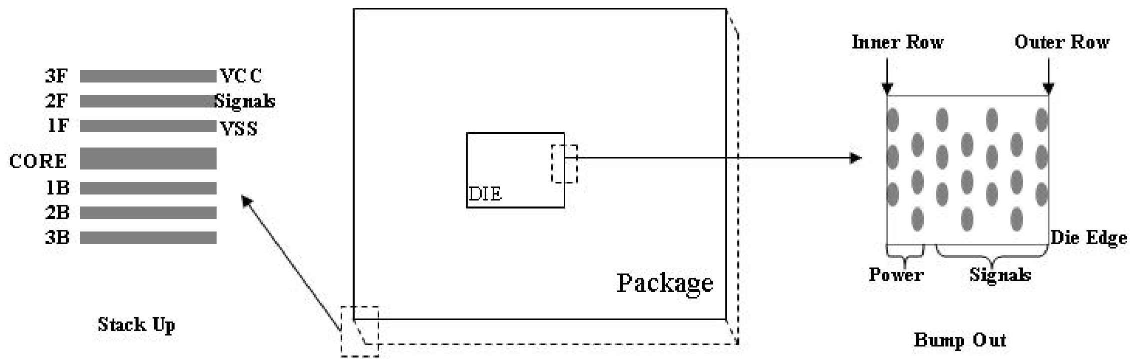

Figure 1: Showing a typical stack up and bump out

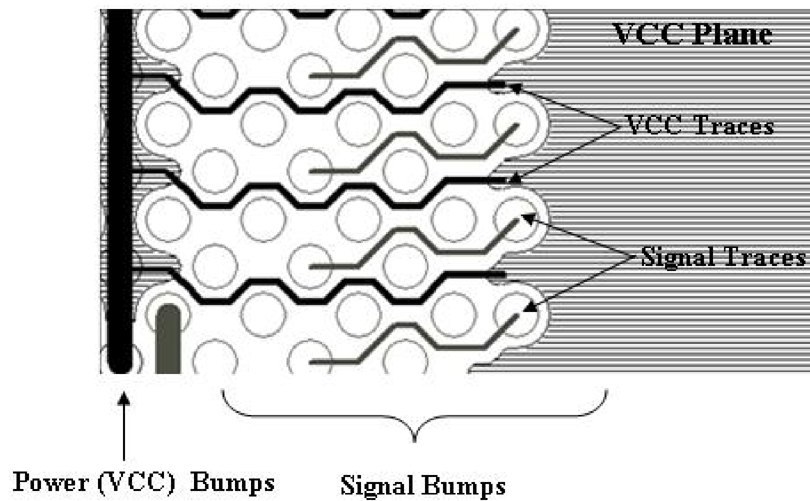

Figure 2: A Power Mesh

impedance. The mesh along the power plane can be seen as a resistance introduced along the loop which can dampen the resonance impedance of the network. Figure 3 shows resistance due to the mesh (R_mesh) affecting a PDN network. A mesh will introduce a finite resistance but will also contribute to the overall loop inductance. The impact to the impedance is as shown in Figure 4. The net impedance value has reduced with higher loop inductance. This is due to dampening effect of the mesh resistance. This trend would continue to certain point after which the increase in loop inductance would nullify the advantage the mesh resistance (R_mesh) offers. From Figure 3 we see that R_mesh comes in HF path only and not along the DC path, hence there will be no DC IR drop due to R_mesh. The entire DC drop will be across R_DC. Typical value for R_mesh is in the range of 5-10mOhms for a 6mm wide power plane with 30 mesh traces of 20um width. In cases where Rdie and R_mesh values are comparable, the impact of R_mesh would be less significant. Hence it is important to estimate Rdie values accurately before implementing R_mesh method.

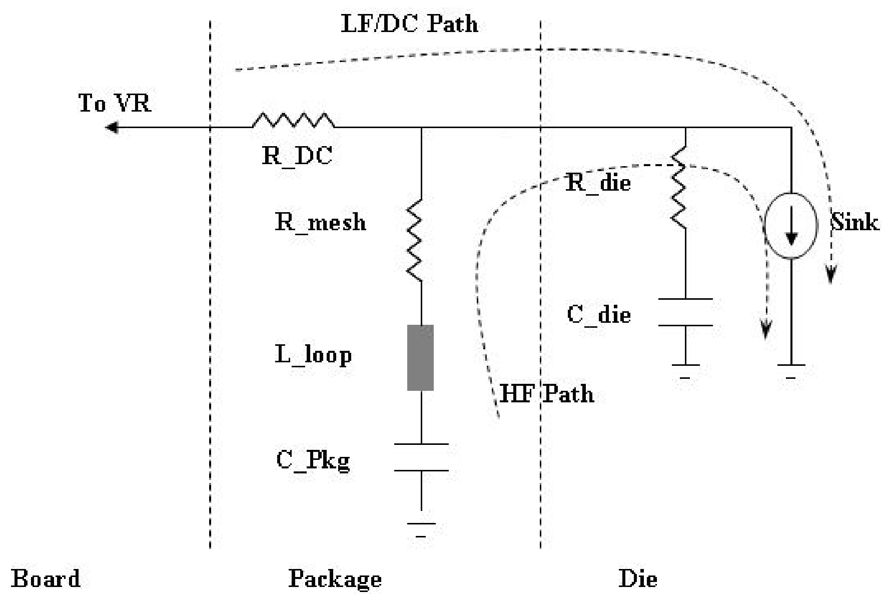

Figure 3: A PDN network and R_mesh

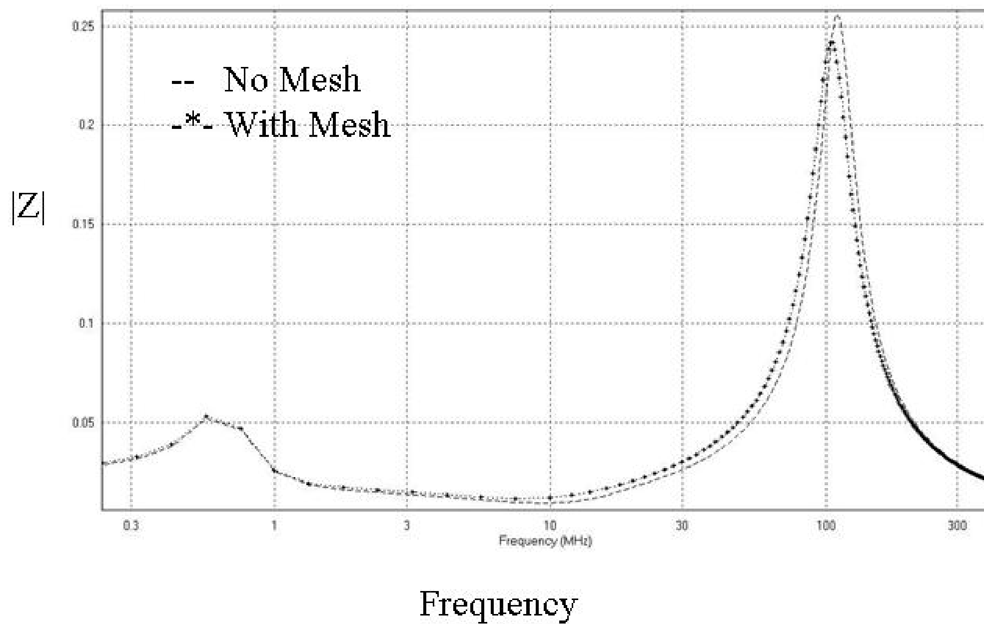

Figure 4: Impedance plot with and without mesh

In a slightly lateral application, R_mesh can be included in the DC path. Figure 5 shows a quiet rail (rail 2) derived from noisy rail (rail 1). The two rails are shorted on the bottom layer of the package as shown. Quiet rail current requirement is very low with strict noise targets. This requires isolating noise getting coupled form the noisy rail. Here R_mesh can be used to attenuate the AC noise coupled from rail 1 as shown in Figure 5. This is will however impact DC, but since the current requirement of the rail 2 is low it

would not result in significant DC drop. In one such application, the noise on the rail -1 was 207mVpp. The coupled noise on the quiet rail was 107mVpp [Target =100mVpp]. A series resistor [lumped] of 10mOhms was introduced between the two rails. The noise on the quiet rail reduced by ~ 10% to 95mVpp, meeting the target spec.

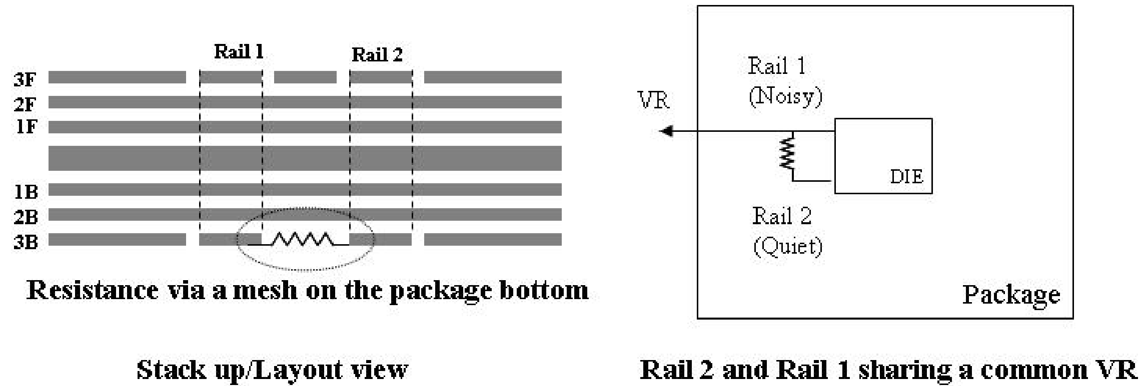

Figure 5: An application of mesh to isolate quiet rail from the noisy rail

Section 3: Return Path Effects

With packages shrinking with generations, the real estate to route power planes is also reducing causing narrower power planes. The narrow power shapes increases the inductance along the HF [High Frequency] path resulting in sub optimal PD performance. This motivates us to identify an optimal methodology for power and ground referencing which utilizes minimum real estate to achieve a given PD performance. During multilayer package design, it is required to reduce the inductance of the power planes wherever possible. The total inductance across a loop can be depicted as per equation 1, where L is the total loop inductance, L1 and L2 are the self inductances of the power and ground plane respectively and M is the mutual inductance between the two planes. From Equation (1) we see that to keep the overall loop inductance low we need to have small self inductance (L) and also have a large mutual coupling inductance (M).

$$L = L1 + L2 - 2M \qquad (1)$$

During the package design, the designer will be faced with several options to connect the decoupling capacitors. Two possible scenarios are shown in Figure 6. The options should be evaluated for the least amount of inductance which depends upon various parameters such as trace width, stack up etc. To asses the effectiveness of the two options we chose several geometries by varying the width of VSS plane (length is kept constant at 10mm) and the loop inductance is evaluated. The results are noted in Table 1. The evaluation was done using PowerSI with the following assumptions: copper conductivity = 5.959E-9(S/m), dielectric thickness= 30um, copper thickness= 15um. The separation between adjacent VCC and VSS plane for option 2 is 10um. From Table 1 we

see that VSS plane underneath has more influence over the loop inductance than adjacent VSS plane. For option 1 to match with loop inductance offered by option 2 a narrower plane would suffice (please compare entries highlighted by dotted circle in Table 1), hence saving real estate. This is assuming we have enough layers to route. In certain packages, like 2 layer package, with substantial core thickness option 2 could be an advantage.

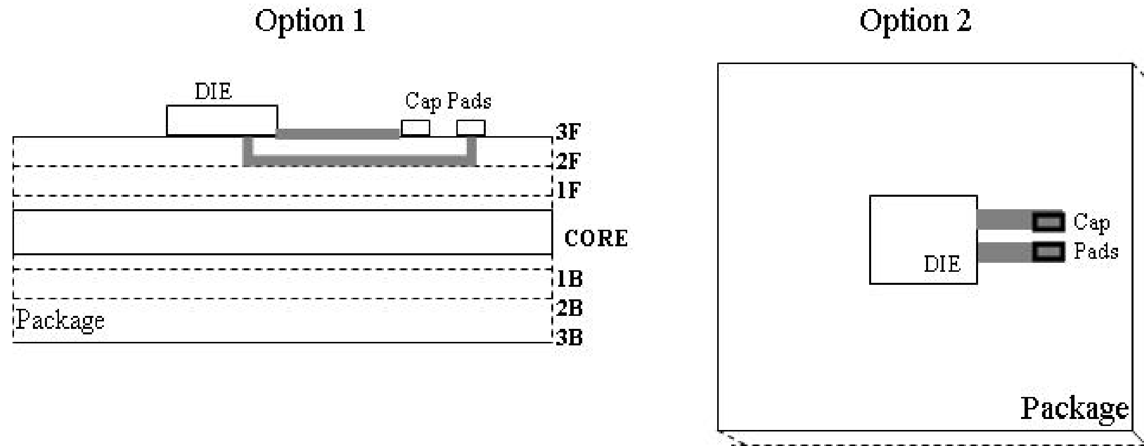

Figure 6: Two choices for connecting cap pads.

Option 1		
VCC	VSS	Loop Inductance
5mm	5mm	145pH
	2.5mm	211pH
	1.25mm	364pH

Option 2		
VCC	VSS	Loop Inductance
5mm	2.5mm	400pH
	5mm	358pH
	10mm	322pH

Table 1: Loop inductance variation with VSS geometry for both the options.

Option 1 and option 2 were tried over DDR interface. Option 1 had 0.8mm wide VSS plane underneath 0.6mm wide VCC plane, Option 2 had 2.4mm wide VSS plane adjacent to the VCC plane. Simulation showed noise of 41mVpp and 90mVpp for option 1 and option 2 respectively. Jitter data collected from lab showed 15ps improvement with option 1 over option 2.

Section 4: A new technique to view the loop inductance

During the PDN design cycle layout constraints (such as KOZ) could vary impacting the loop inductance of the network. KOZ limit is a design rule constraint which defines the minimum distance of cap pads from the die edge. Figure 7 shows a pictorial of KOZ. KOZ varies with technology, package size, die size etc. During the product design cycle the manufacturing constraints could change with new technology being enabled. The constraints could redefine the KOZ region and sometimes KOZ gets larger as shown in Figure 7. The increase in KOZ region pushes cap pads away from the die edge resulting in higher loop inductance and thus impacting PDN resonance. To better handle the impact to the overall loop inductance we look at the loop from a different perspective.

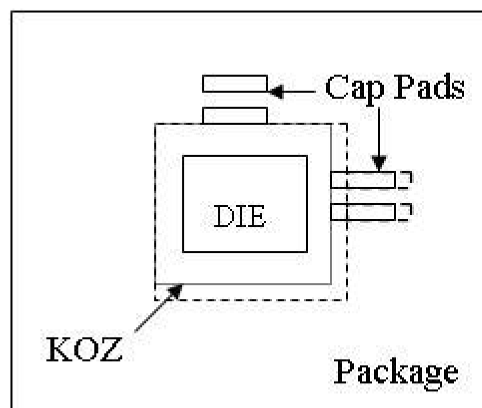

Figure 7: A depiction of KOZ

Consider a simple AC loop as shown in Figure 8. The figure shows a conceptual view of a VCC and VSS plane which could be for either option 1 or option 2 as in Figure 6. The overall loop inductance of this loop is L_total. The entire loop is viewed as sum of three subsections as shown in Figure 9, each sub section contributing its respective inductance adding to overall inductance (L_total). Any layout change resulting in increase in the length of the entire loop say by Δx (Figure 8) can be seen as increase in length of one sub section (section 3) by $\Delta x3$, as shown in Figure 9. To compensate for the increase in the L_total, width of section 1 can be increased by $\Delta w1$ as shown in Figure 9. Thus maintaining the over all inductance, L_total. However this assumes that there is scope for optimizing the overall loop. In situations where the loop is optimized, increase in the width of one of the subsection could be achieved at the cost of some other adjacent rail. A critical rail is given priority over the adjacent non critical rail. Figure 10 shows that the inductance can be maintained with distance when width is varied proportionally, shown by the dotted line. This technique helps identify a section of the loop which could be optimized to handle the loop inductance variation due to change in the layout constraints such as KOZ.

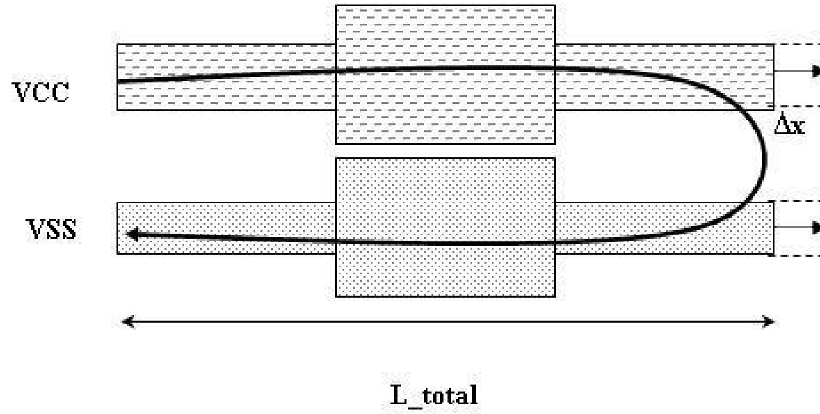

Figure 8: A simple AC loop

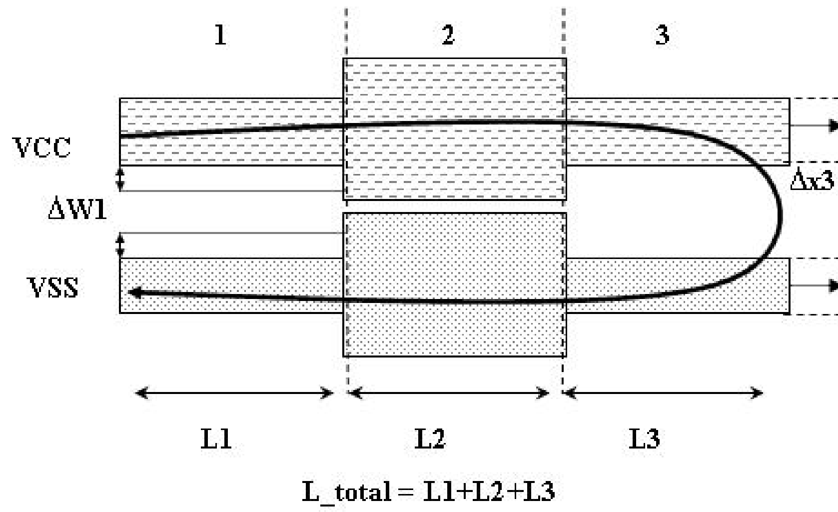

Figure 9: AC loop broken down into smaller sub sections

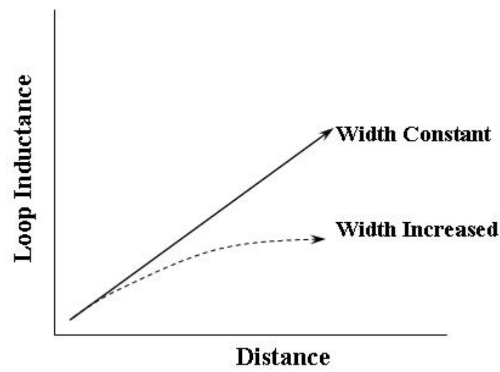

Figure 10: Loop Inductance variation with distance (length of loop).

During a case study, the power plane was designed to have overall loop inductance of 289pH. Due to KOZ change the cap pads got shifted away from the die by 1400um. The VSS necking width was increased by 170um and the new loop inductance was evaluated to be 282pH.

Section 5: Summary

This paper provided techniques to handle layout constraints for optimizing the PDN performance. Employing a mesh on the power plane to our advantage for one typical case of bump out and stack up were discussed. The paper showed that the mesh if designed properly helped a PDN to improve the impedance profile and in another application it was used to isolate a quiet rail form the noisy source. Simulation/lab data were provided to show that the return path with strong mutual coupling is preferred and it helps achieve a given target loop inductance with minimum real estate. Lastly a new technique to view overall loop inductance as sum of smaller subsections was discussed. This helped to identify the section of the overall loop which could be optimized for PD performance in the event of the layout changes. The techniques discussed in this paper depend on some assumptions but their application may not be limited by them.