

Broadband Methodology for Power Distribution System Analysis of Chip, Package and Board for High Speed IO Design

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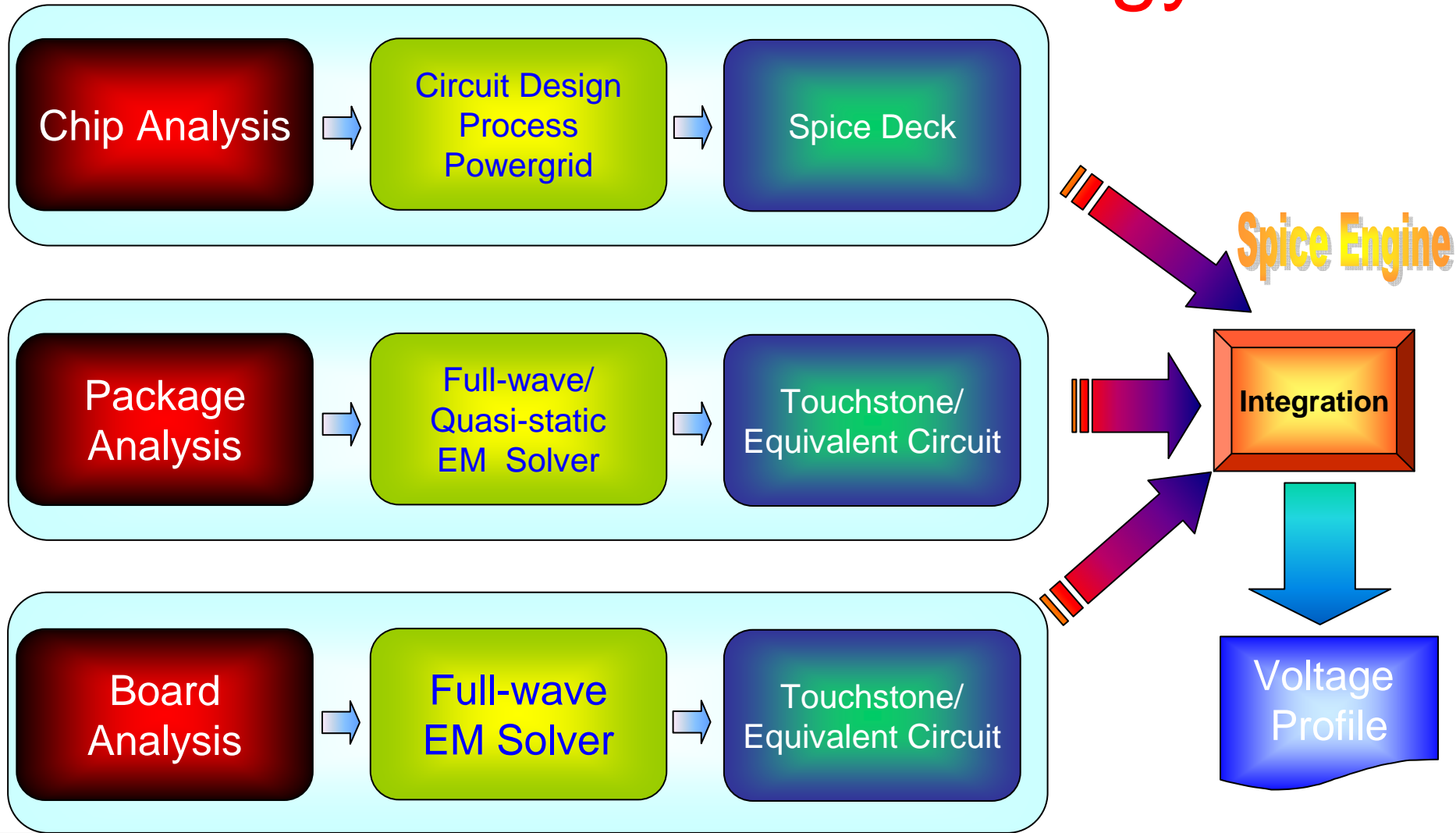


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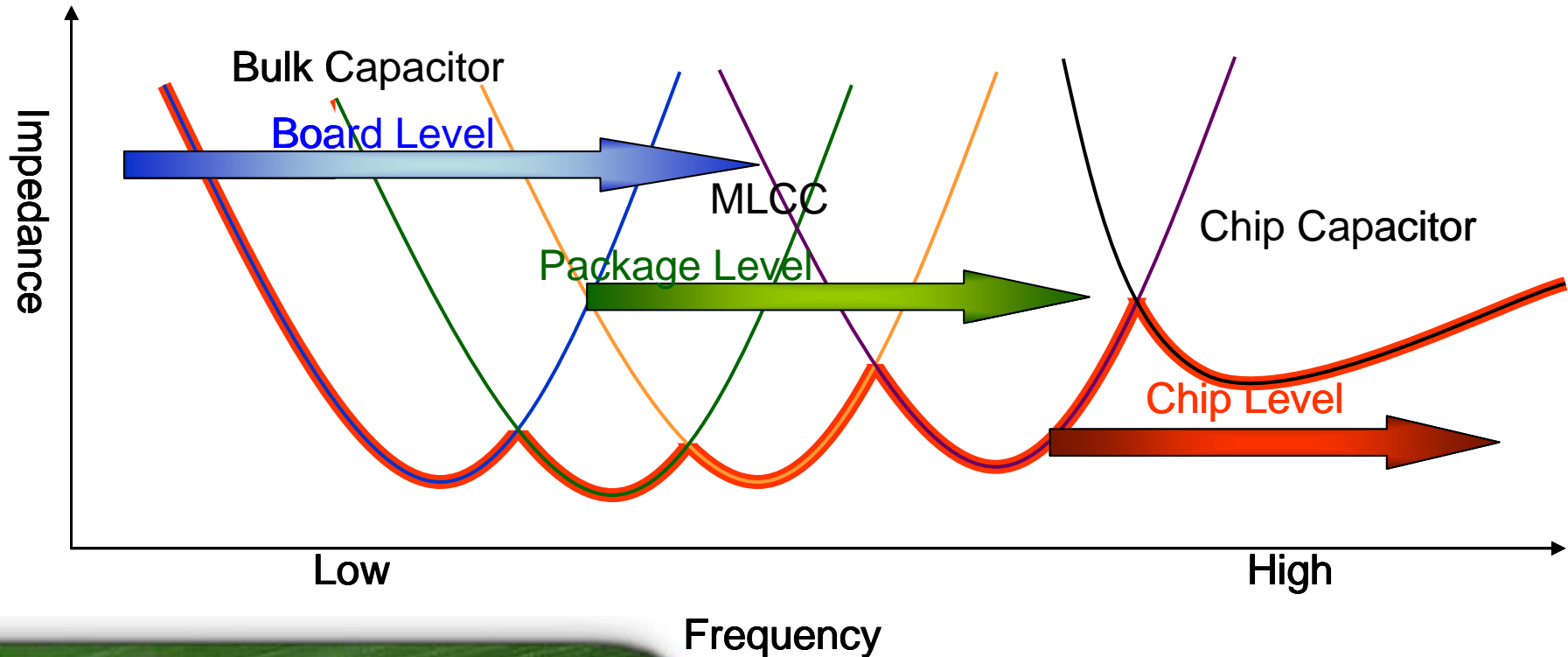
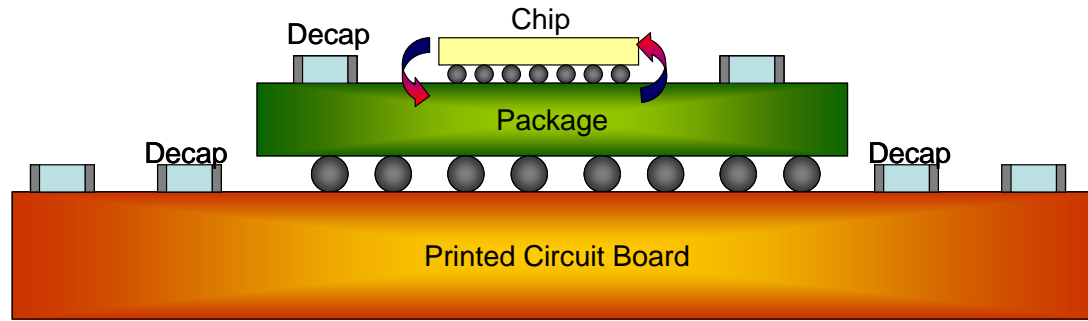
Outline

- Introduction
 - Traditional Methodology
 - Analysis Issues and Platform Request
- Co-simulation Methodology
- Power Distribution System
 - Electrical Characteristics Interaction
 - Location Dependent Impedance Profile
 - Power Distribution System Interference
 - What-if Analysis in Decoupling Capacitors Population
- Conclusion

Traditional Methodology

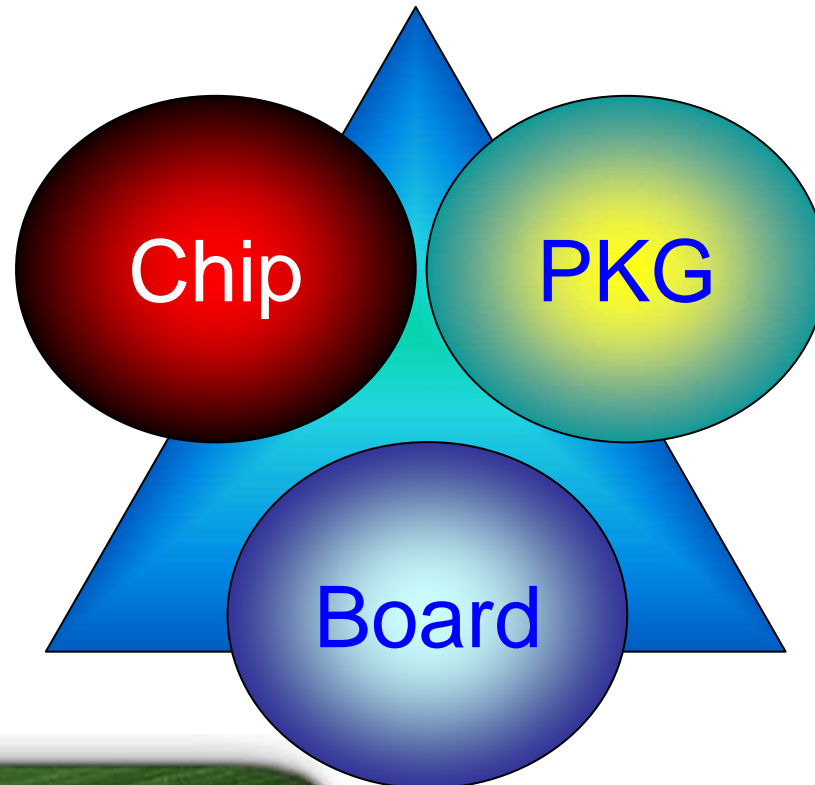


Physical Interaction

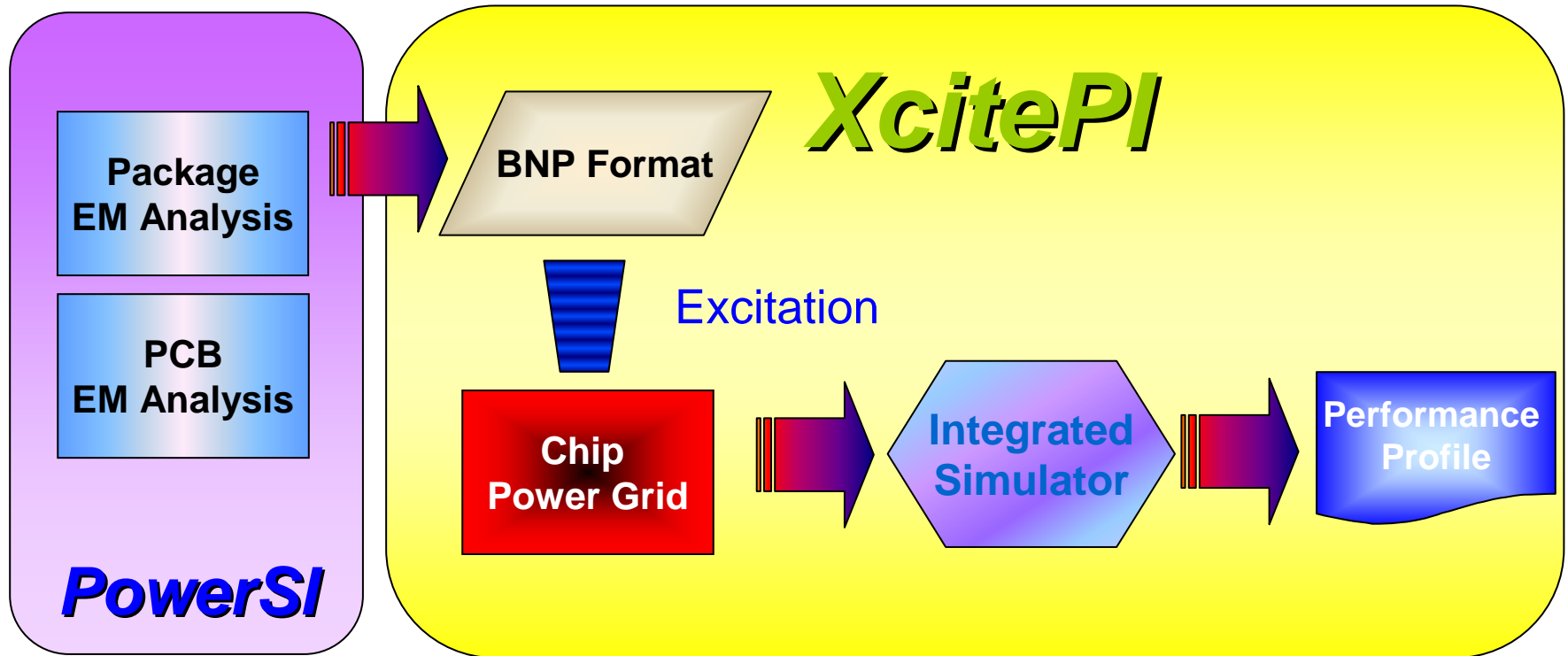


Analysis Issues and Platform Request

- Analysis Issues
 - How to efficiently Calculate On-chip Powergrid
 - Frequency-dependent Response of On-chip Powergrid
 - How to Link with the Different Simulator Results with SNP and Spice Netlist
 - How to Deal with these Combined Effect in this Complicated and Large Netlist
 - How to Link in the Global SSN Perspectives
 - How to Define Operation Pattern and Design CriteriaETC

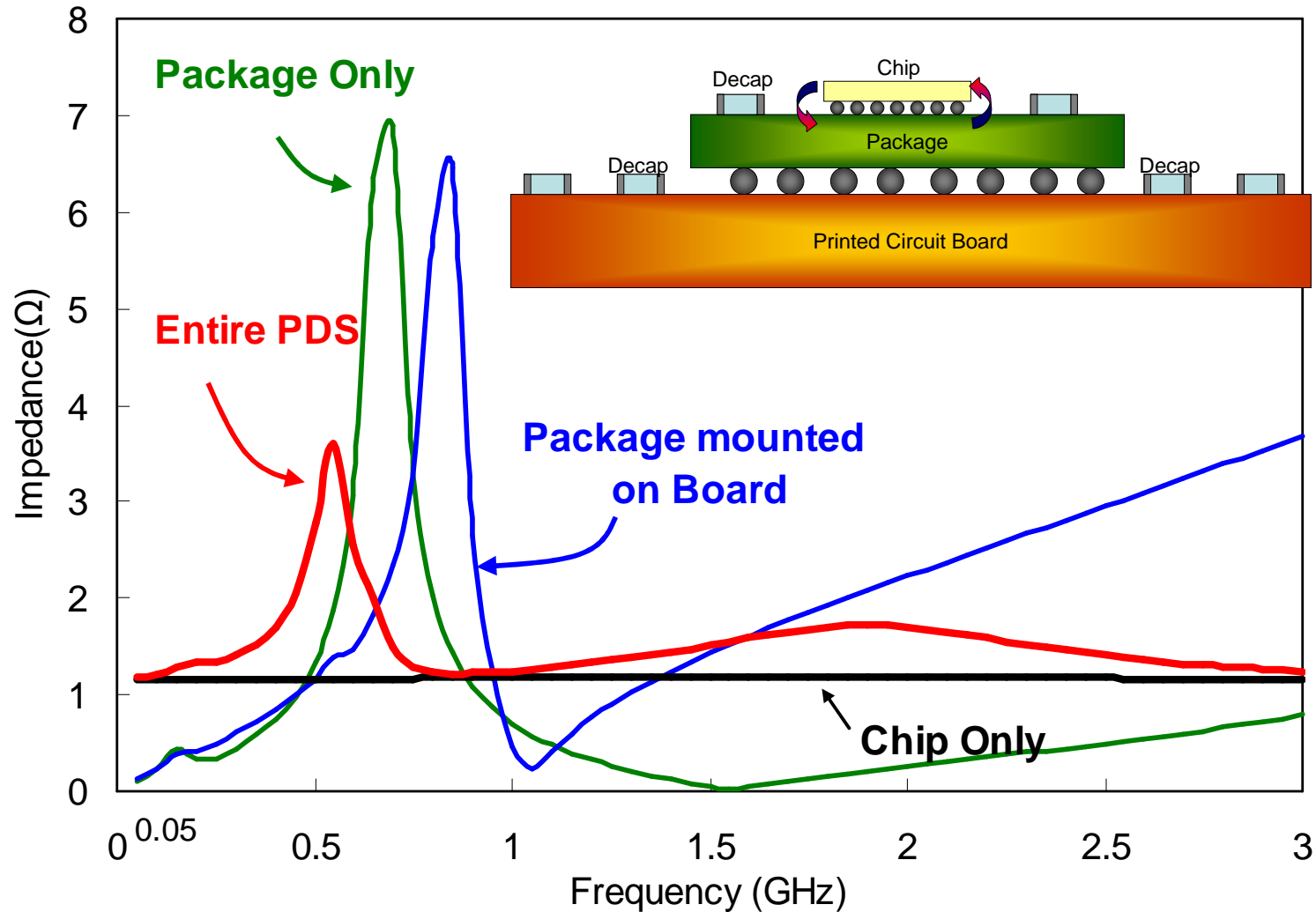


New Co-simulation Analysis Flow



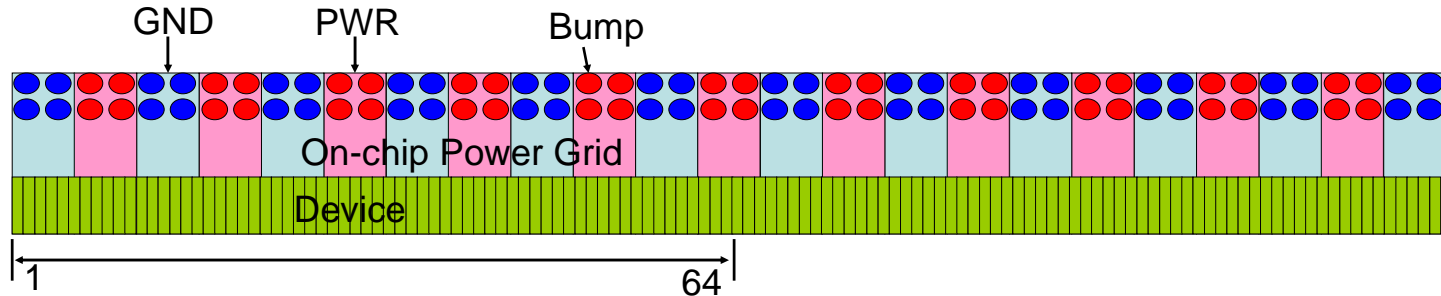
- Automatic Linkage Method by Using Unique BNP Linkage between Chip Power Grid, Package and Board
- Powerful Integrated Simulator to Deal With the Complicated Network
- Frequency-dependent Performance Profile
 - Easy for debugging
 - Effective for Characterization

Electrical Characteristics Interaction

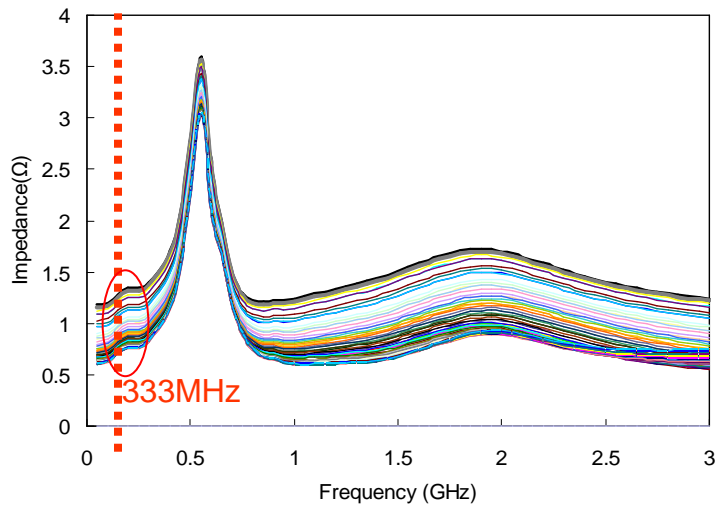


Location Dependent Impedance Profile

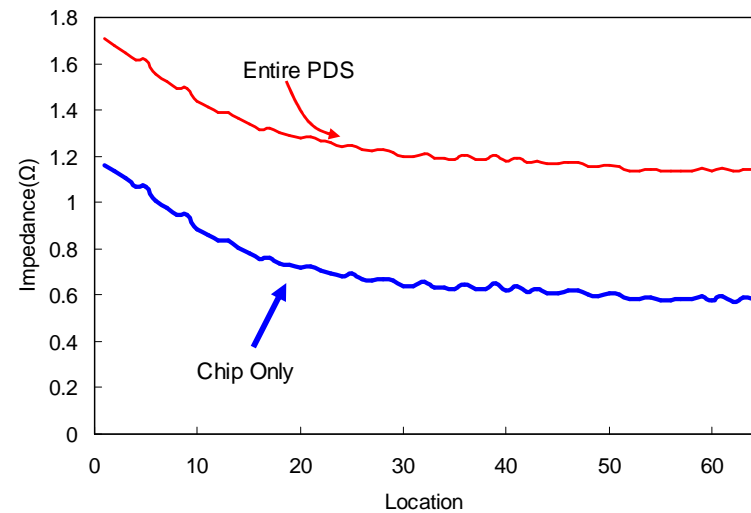
Chip Physical Design



Frequency Response



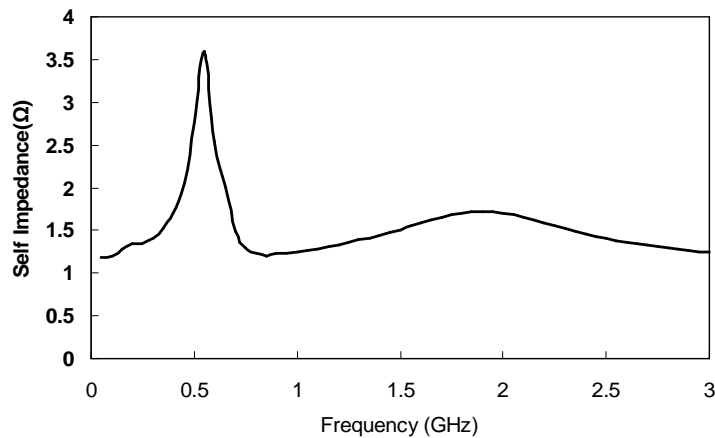
Spatial Distribution @ 333MHz



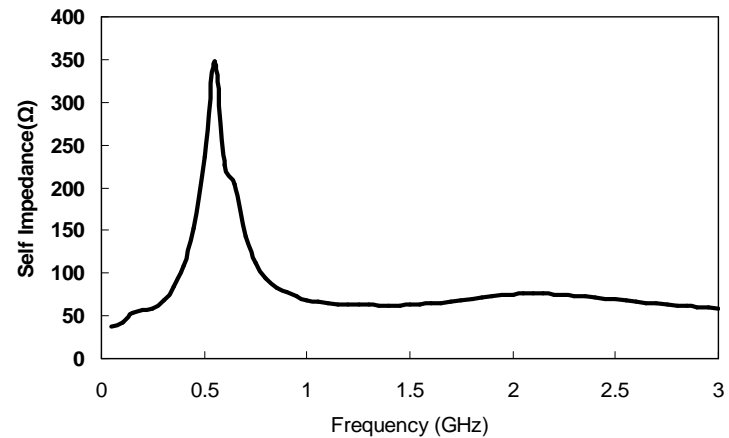
PDS Total Impedance by Interference

Z_{Total} / Z_{11} at 333MHz $\sim 30X$

Self Impedance



Ztotal

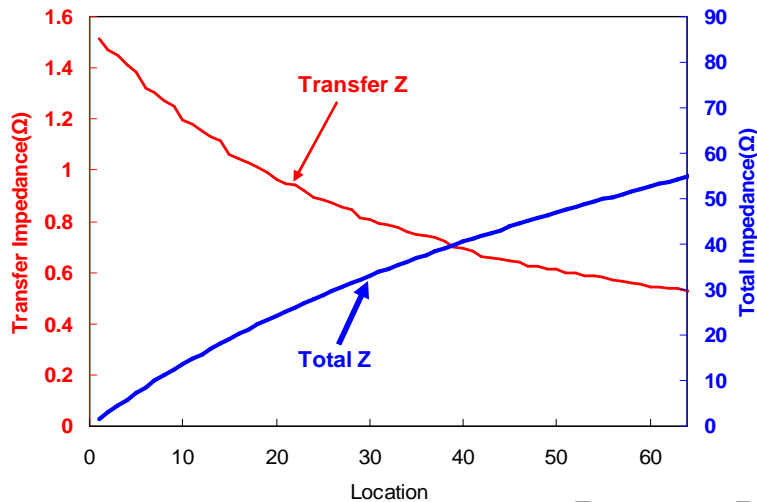


$$Z_{total} @ IO\#1 = \sum_{x=1}^{64} Z_{(1,x)}$$

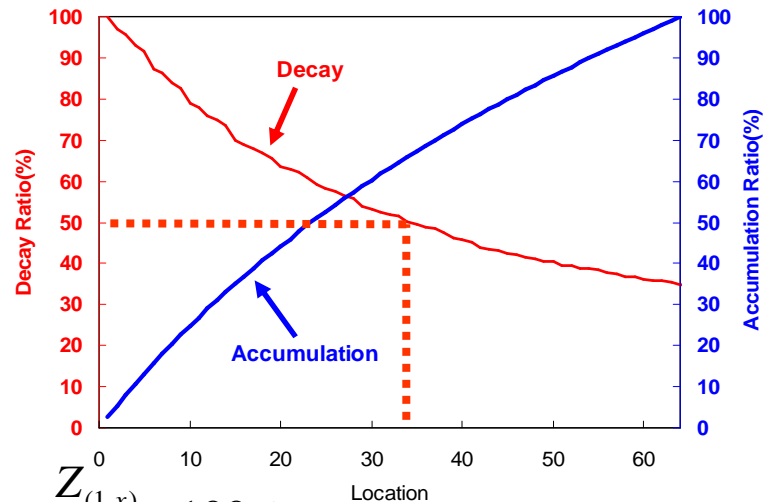
PDS Interference Characteristics

PDS interference in SSN should be seriously emphasized.

Observation at Location #1 @333MHz



Interference Decay and Accumulation @ Location #1 @333MHz

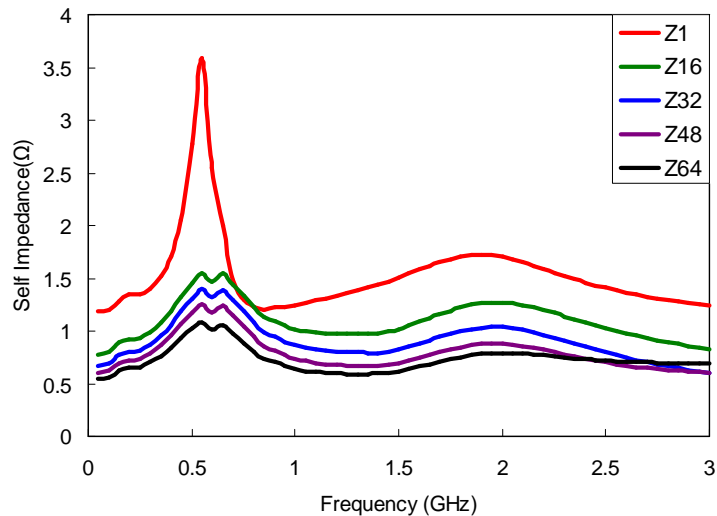


$$Decay_Ratio = \frac{Z_{(1,x)}}{Z_{11}} \times 100\%$$

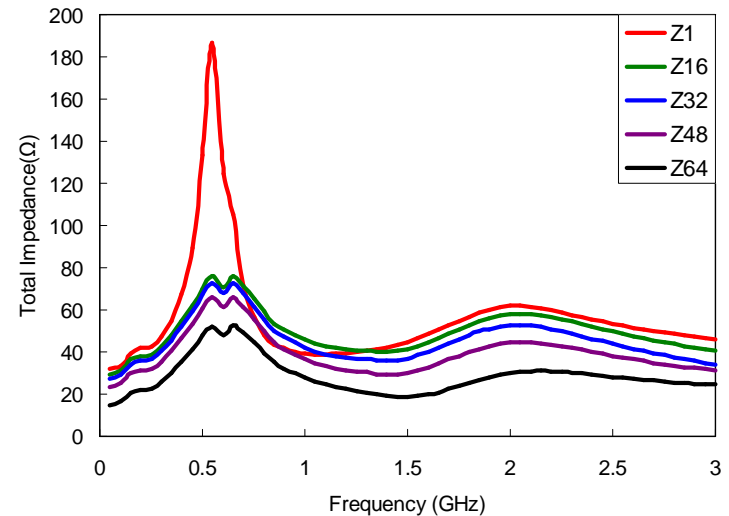
$$Accumulation_Ratio @ N = \frac{\sum_{x=1}^n Z_{(1,x)}}{\sum_{x=1}^{64} Z_{(1,x)}}$$

Location Dependency

Self Impedance

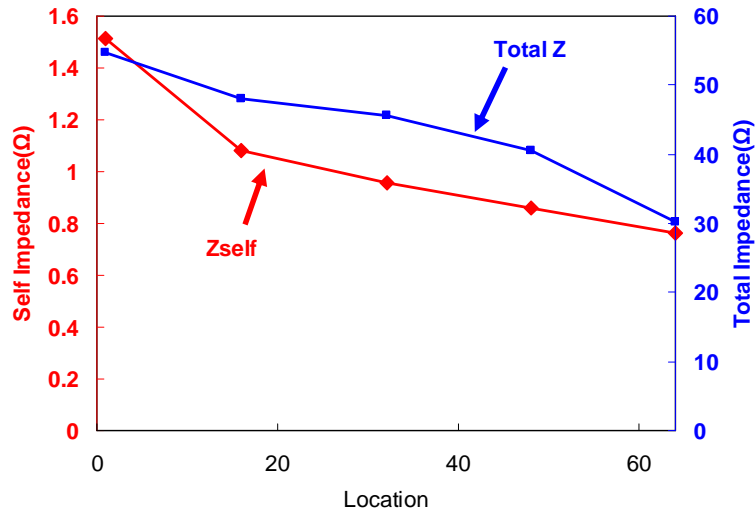


Total Impedance

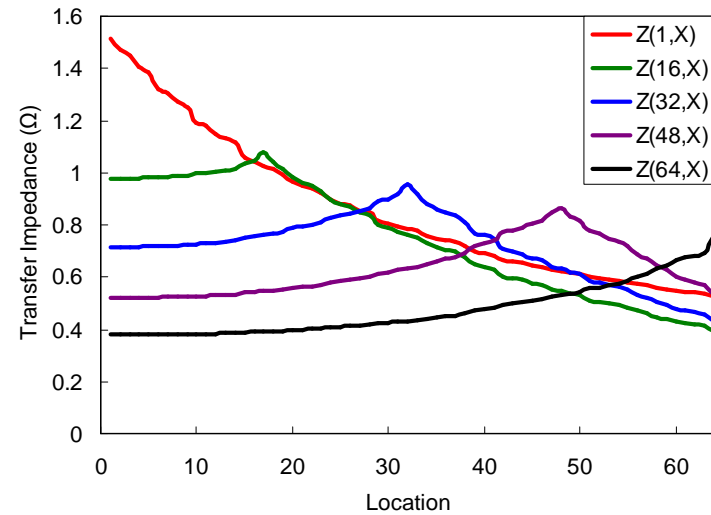


Location Dependency

Self Z V.S. Total Z



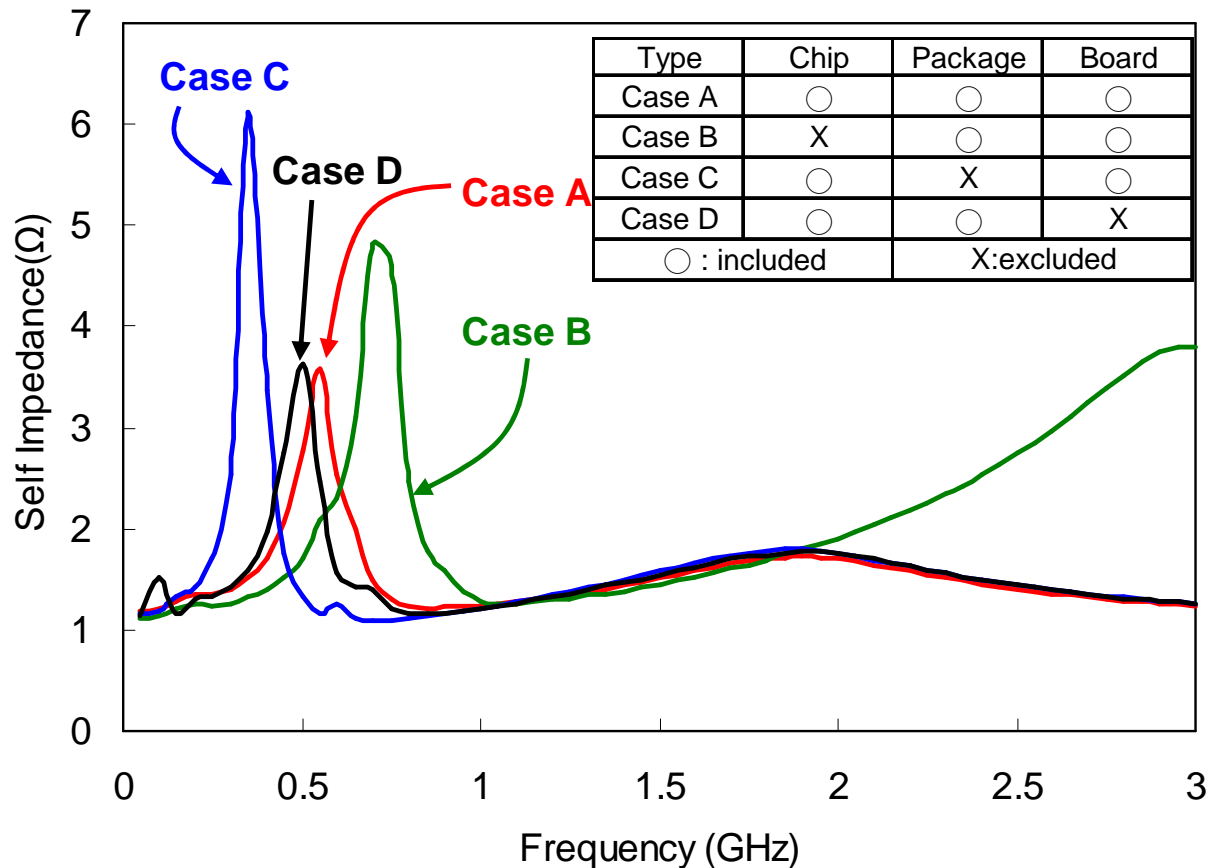
Transfer Impedance



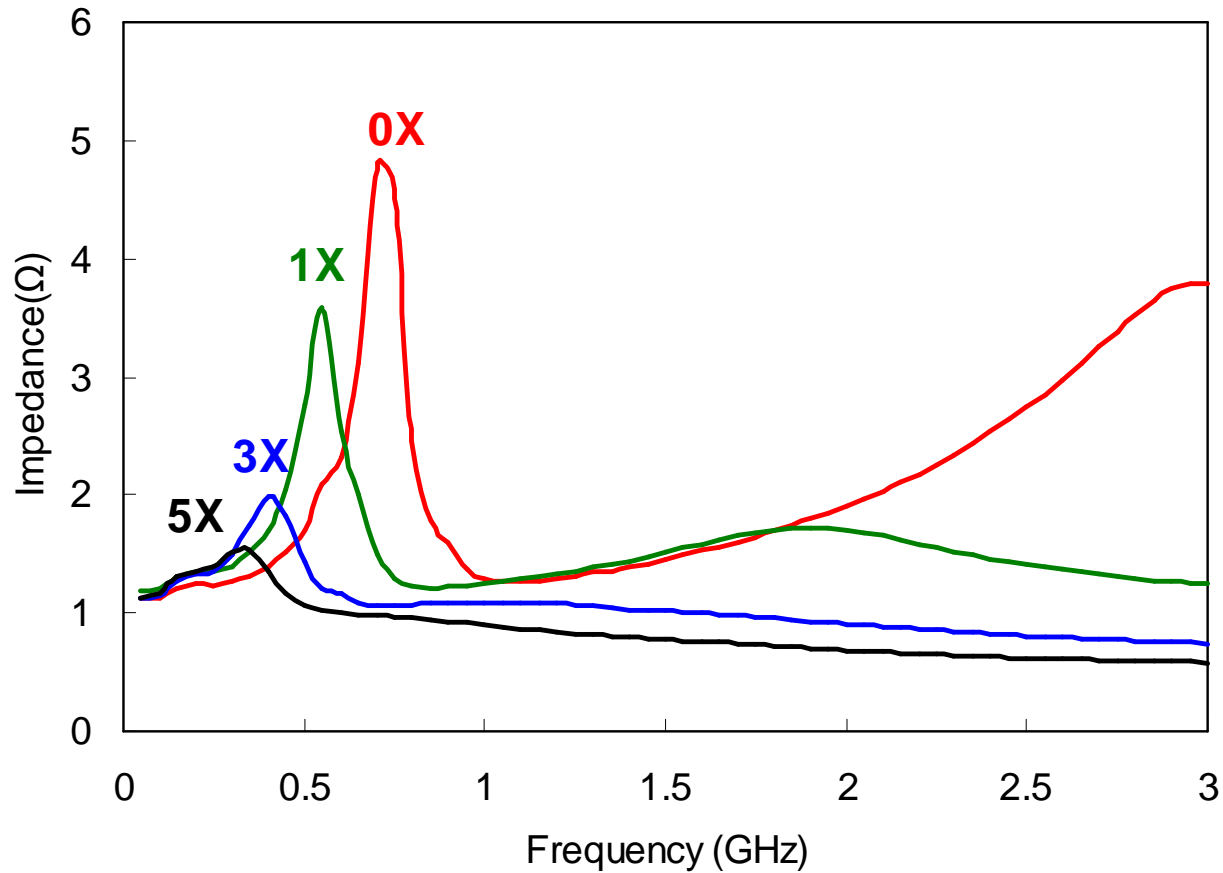
What-if Analysis in Decoupling Capacitors Population

- Influence of Decoupling Capacitors in Different Levels
- On-chip Capacitor Impact on the Entire PDS
 - Chip Capacitance Influence
 - Removal of Chip Capacitor
 - Excessive Chip Capacitor
- Off-chip Power Distribution System Optimization

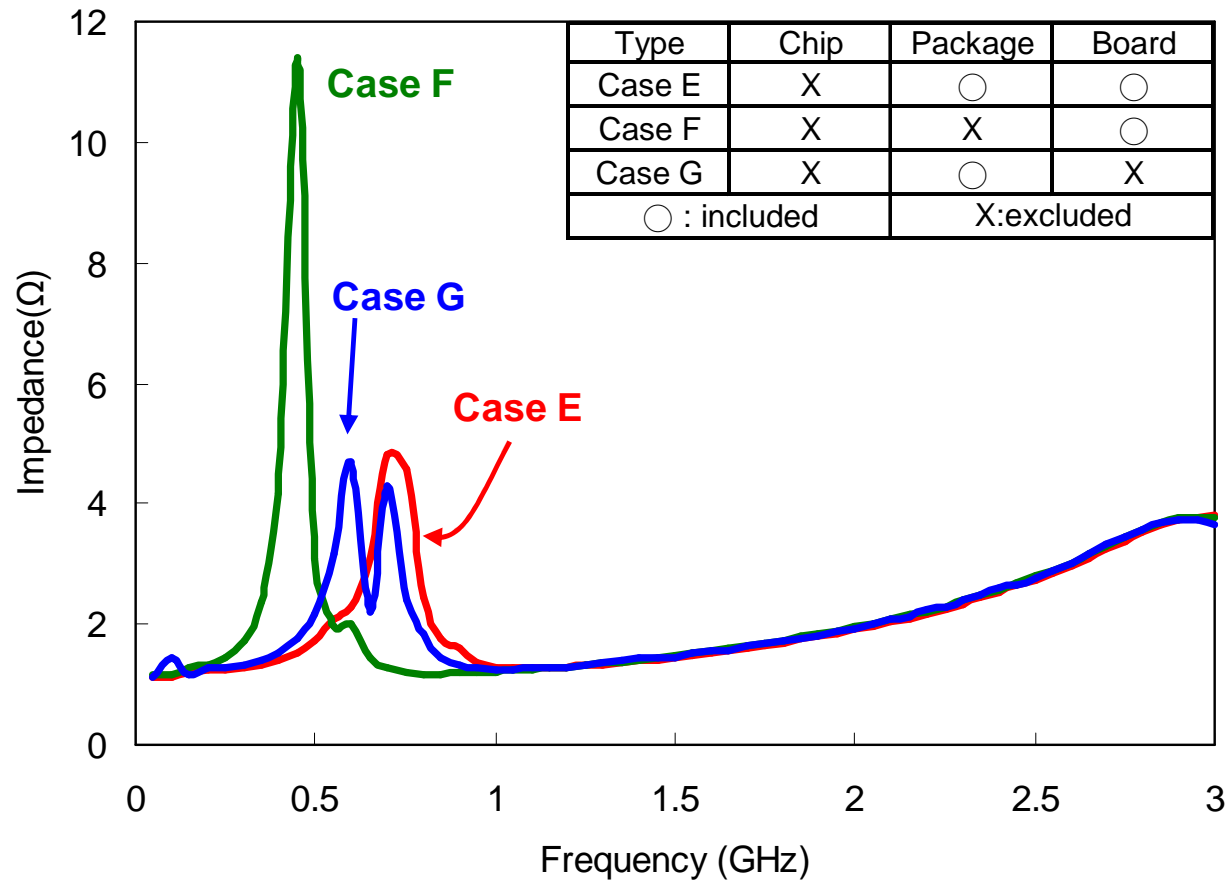
Influence of Decoupling Capacitors in Different Levels



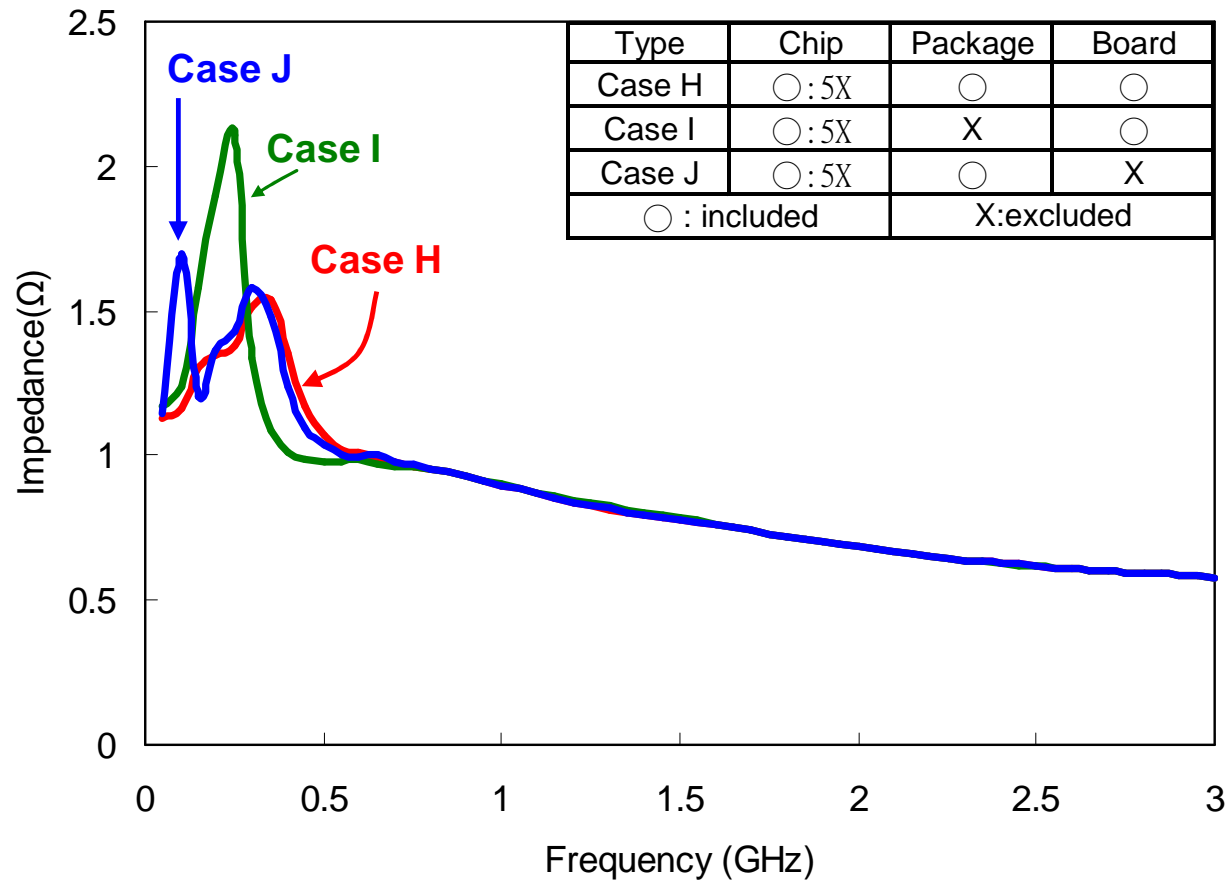
On-chip Capacitor Impact on the Entire PDS



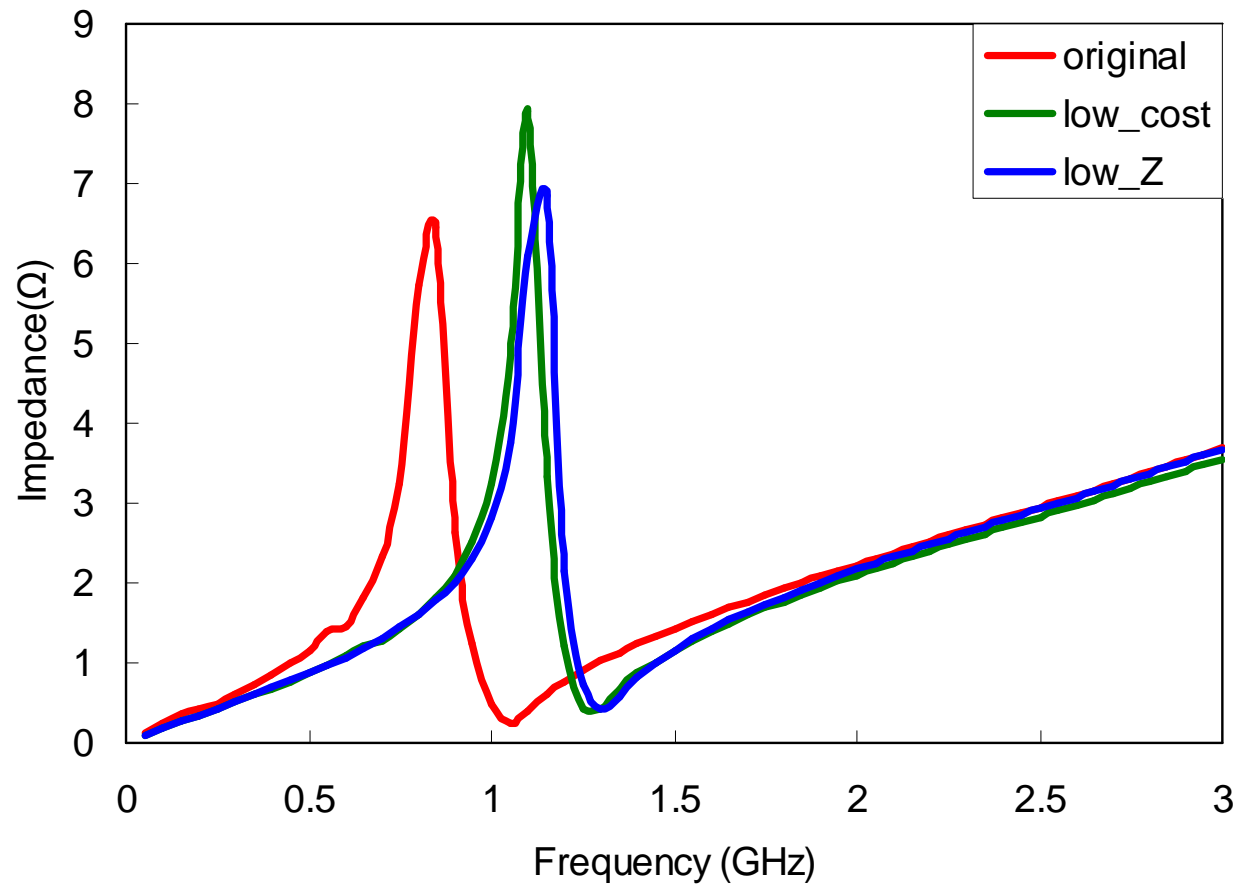
On-chip Capacitor Impact on the Entire PDS



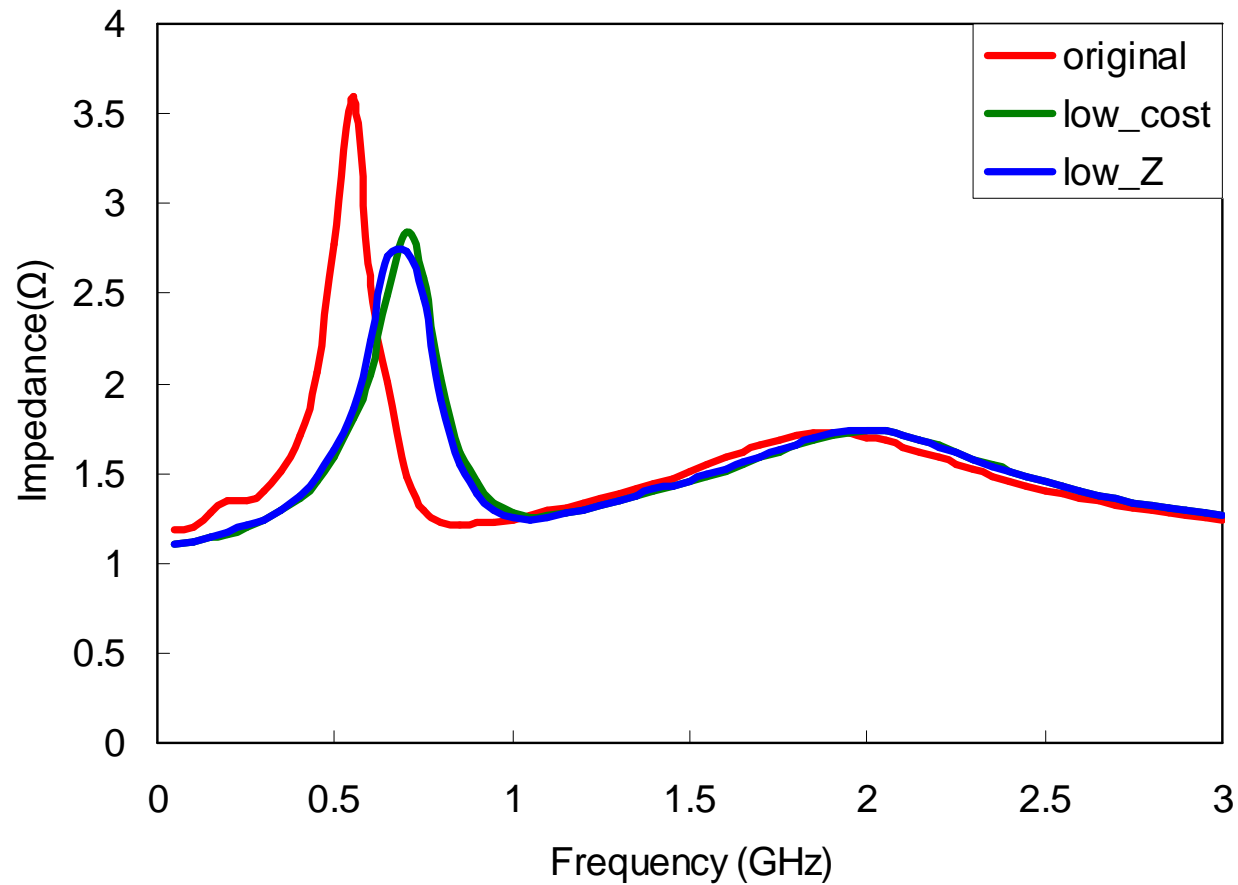
On-chip Capacitor Impact on the Entire PDS



Off-chip PDS Optimization



Entire PDS Comparison



Summary

- The entire PDS methodology from the chip, package to board was proposed to validate the system design by using the frequency domain analysis.
- The location dependency and the interference through the shared network were analyzed to efficiently figure out the design defect and simultaneously switching noise in PDS.
- The different level capacitors are contributed to different frequency bands.
- This kind of the methodology is efficient to compromise the different physical design solutions between the performance driven and cost saving perspectives.