

A Resonance-Free Power Delivery System Design Methodology applying 3D Optimized Extended Adaptive Voltage Positioning

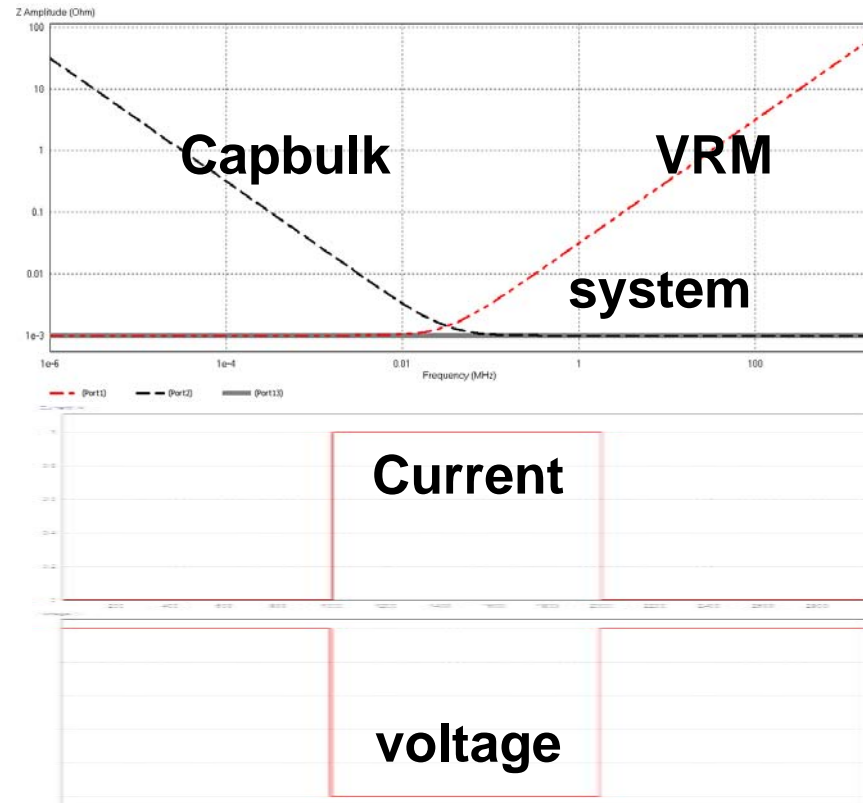
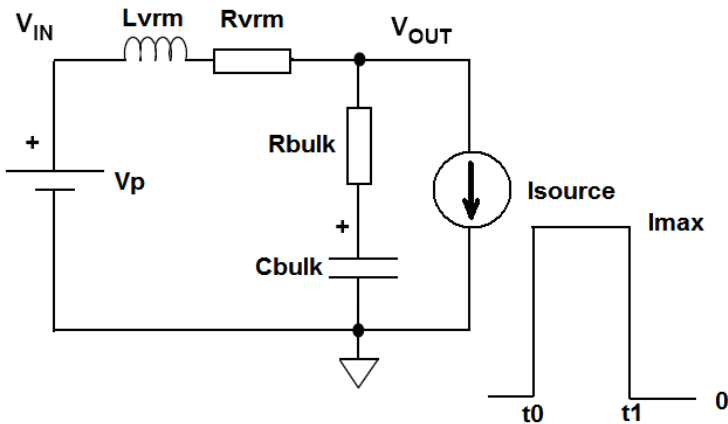
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Agenda

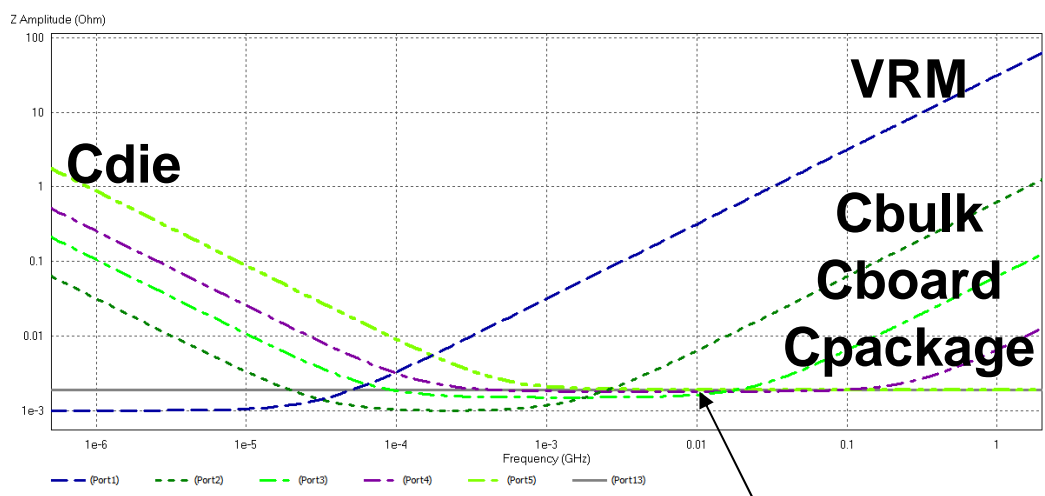
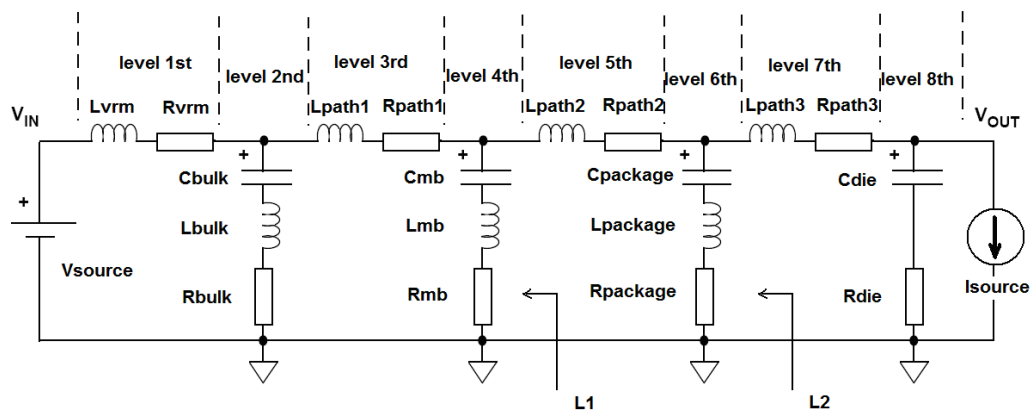
- Adaptive voltage positioning (AVP)
- Extended adaptive voltage positioning (EAVP)
- Optimized extended adaptive voltage positioning
 - Method
 - Real case application
- Time domain verification

Adaptive Voltage Positioning (AVP)



- AVP method was originally proposed to design a VRM with a bulk capacitor
- A flat PDS impedance can be achieved, if the component values are satisfied the conditions: $R_{vrm} = R_{bulk}$, $R_{bulk} \cdot C_{bulk} = L_{vrm} / R_{vrm}$

Extended Adaptive Voltage Positioning (EAVP)



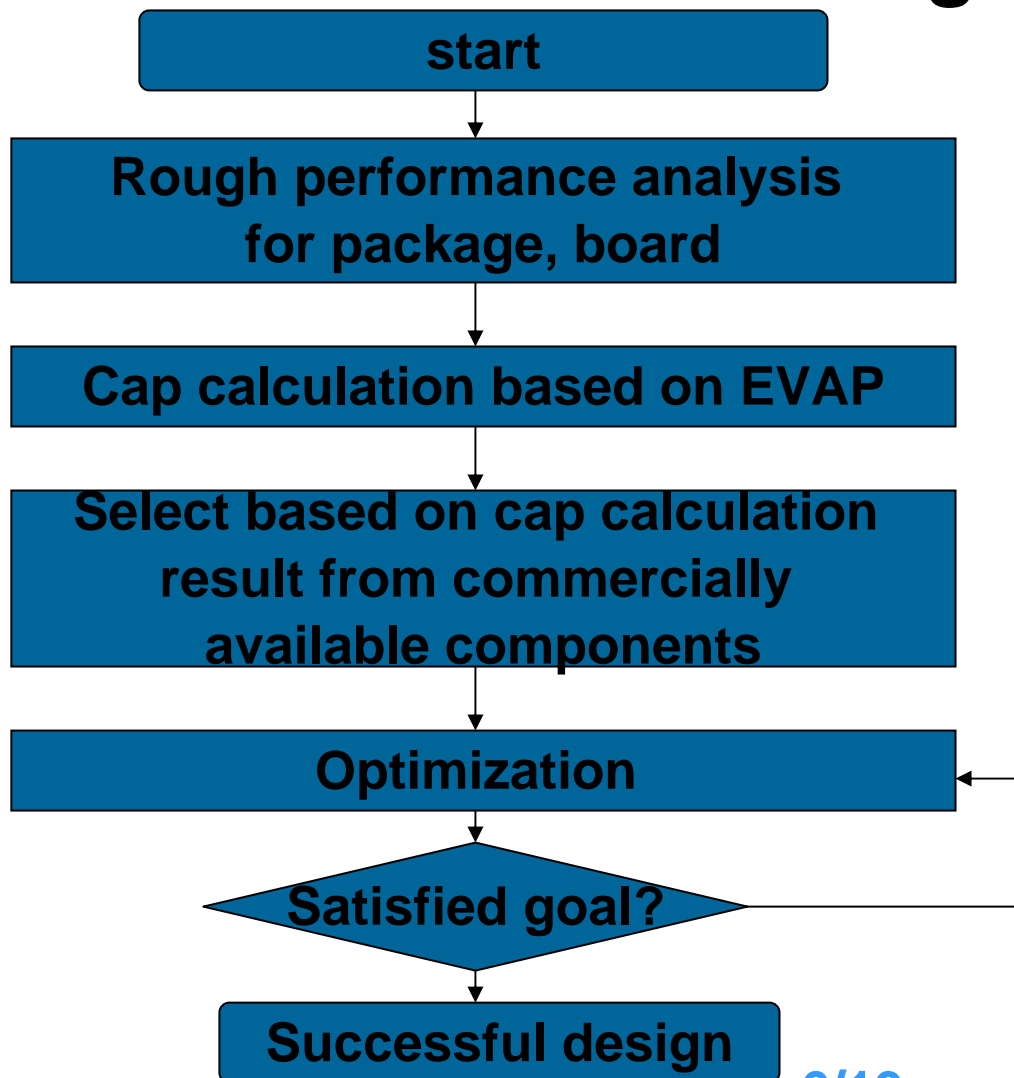
system

- To yield a flat PDS impedance
 - the ESR of decoupling stage N must be equal to the ESR of decoupling stage N-1.
 - the RC time constant of decoupling stage N must be equal to the L/R time constant of stage N-1.

Optimized Extended Adaptive Voltage Positioning—Why

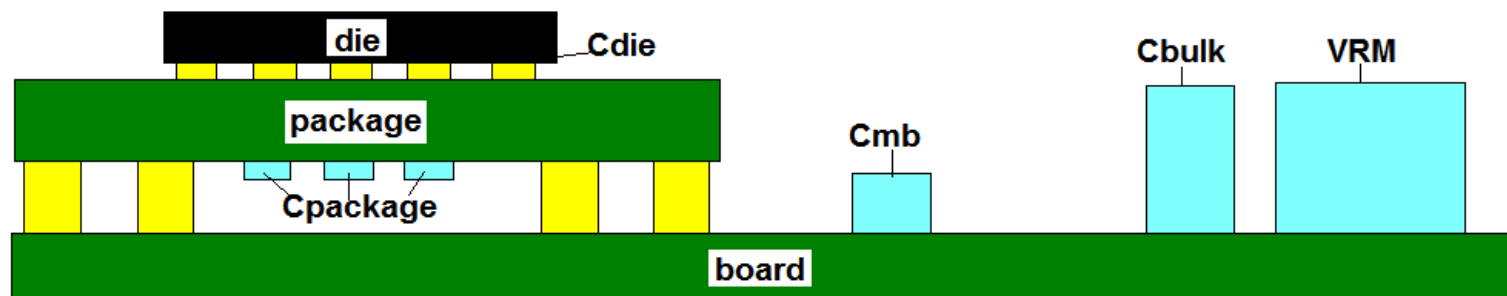
- 1D EVAP circuit topology does not correspond well to the complex 3D nature of a modern PDS.
 - vertically-stacked power planes
 - laterally-distributed decaps
 - Decaps are located on top and bottom of boards and packages.
- the RLC element values required at each level of the PDS are often difficult to implement with commercially available components

Optimized Extended Adaptive Voltage Positioning—How



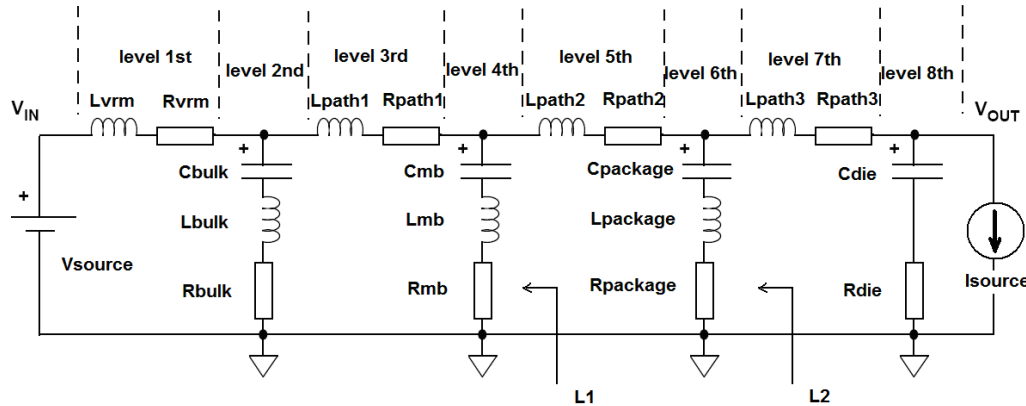
- EAVP was used to select capacitors for the initial PDS design.
- Then 3D EM analysis was applied to characterize the 3D PDS structure with capacitors placement diversity across multiple levels of the PDS (board-package-chip) and the ability to select capacitors from a library of commercially available components

Real system design



- An 6 layer FCBGA package
- An 8 layer board
- A 1 m Ω and 5.4 nH VRM
- Design goal :5 m Ω PDS impedance
- Interested frequency range: DC to 2 GHz.

Calculation with EVAP



- $R_{vrm} = R_{bulk}$
- $R_{bulk} * C_{bulk} = L_{vrm} / R_{vrm}$
- $R_{mb} = R_{bulk} + R_{path1} = R_{vrm} + R_{path1}$
- $R_{mb} * C_{mb} = (L1 + L_{path1}) / (R_{vrm} + R_{path1})$
- $(L_{vrm} // L_{bulk} + L_{path1}) / (R_{vrm} + R_{path1})$
- $R_{package} = R_{mb} + R_{path2}$
- $R_{package} * C_{package} = (L1 + L_{path2}) / (R_{mb} + R_{path2})$
- $R_{die} = R_{package} + R_{path3}$
- $R_{die} * C_{die} = (L2 + L_{path3}) / (R_{package} + R_{path3})$

First level system calculation

		Inductance	Resistance	Capacitor
Condition	VRM	5n	1m	
	Path1	3.27n (estimated)	0.5m (estimated)	
	Path2	2n(estimated)	0.3m(estimated)	
	Path3	0.65n(estimated)	0.1m(estimated)	
Result	Bulk capacitor	0.1n	1m	5000u
	Capacitor on motherboard	0.01n	1.5m	1500u
	Capacitor on package	0.001n	1.8m	620u
	Capacitor on die		1.9m	180u

- The result for capacitor is not applicable directly

Real cap lib selection

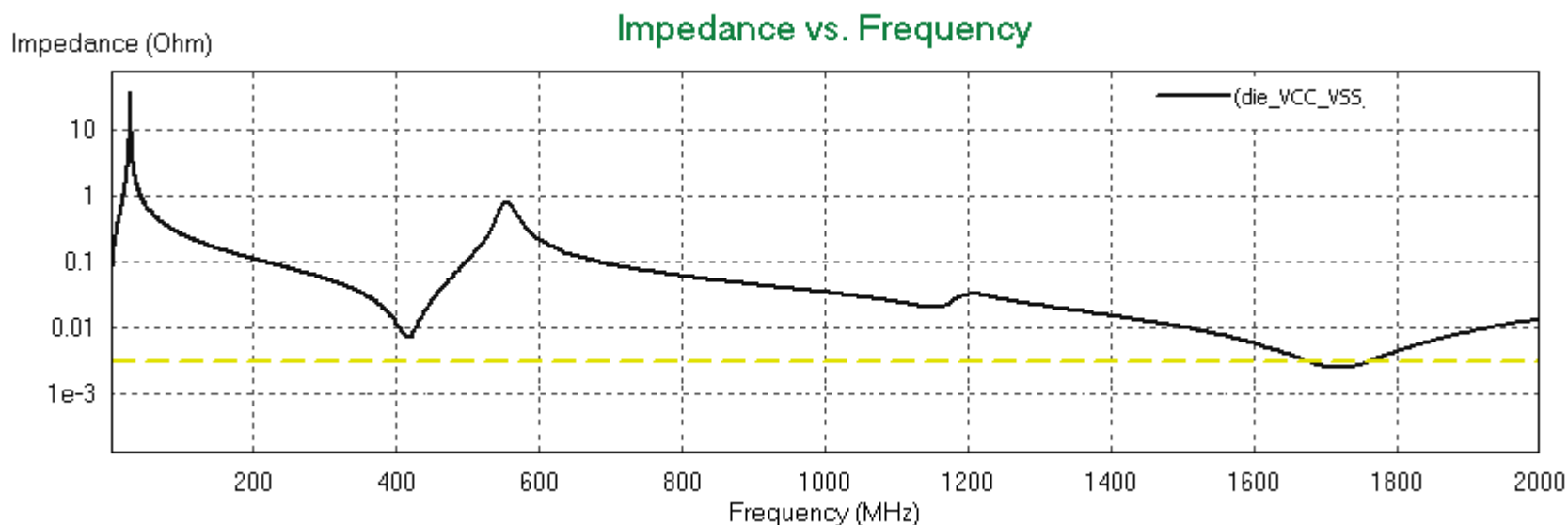
Capacitor Library Manager

Project Library External Library

ID	Part No.	Prefer...	Size	Model Type
1	Cdie1	5	0302	RLC
2	Cdie2	5	0302	RLC
3	Cpackag1	5	0402	SPICE Model
4	Cpacka...	5	0402	SPICE Model
5	Cpackage	5	0402	SPICE Model
6	Cpackge4	5	0402	SPICE Model
7	Cmf1	5	0806	SPICE Model
8	Cmf2	5	0806	SPICE Model
9	Cmf3	5	0806	SPICE Model
10	Cmf4	5	0806	SPICE Model
11	Cmf5	5	0806	SPICE Model
12	Cbulk	5	3030	RLC

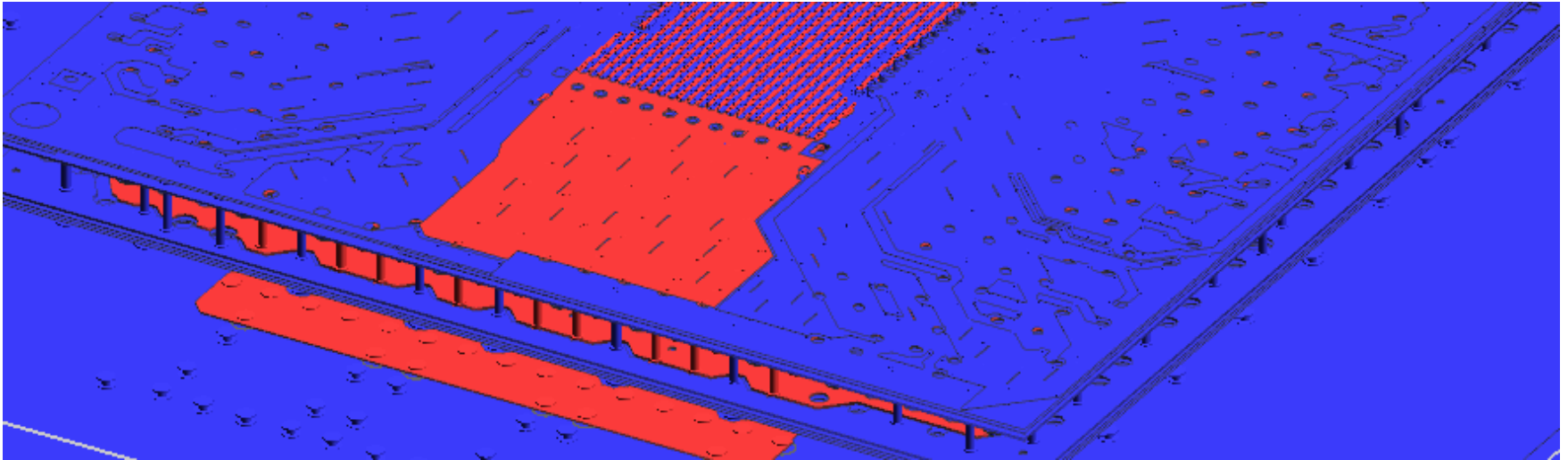
- Several caps were chosen based on EVAP calculation result among commercially available component.

Performance with no cap



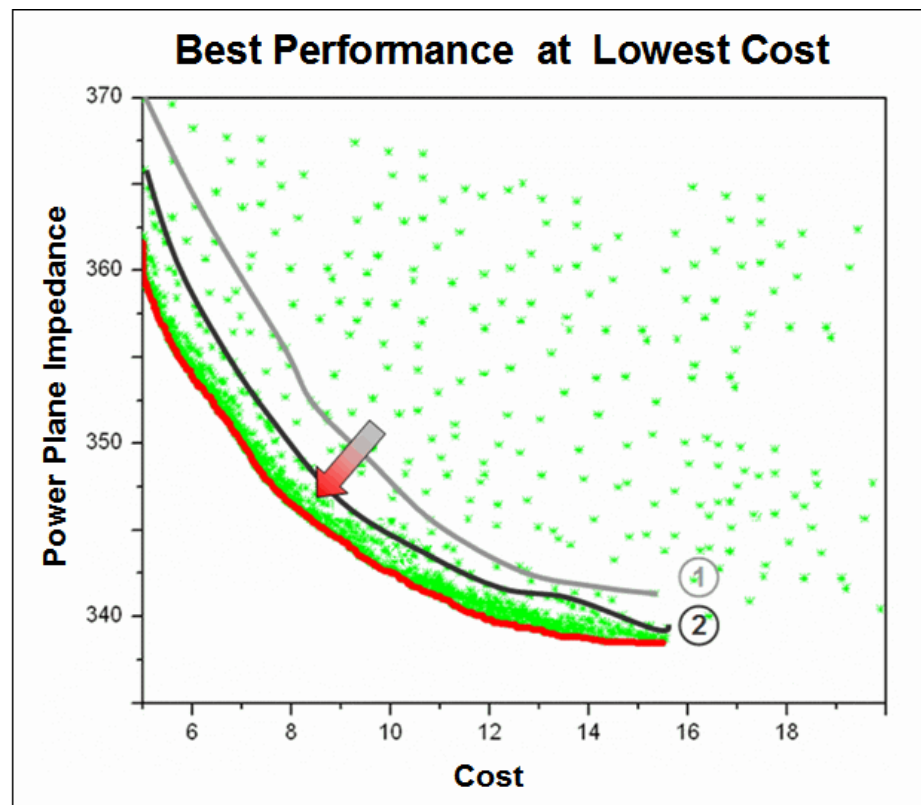
- When no cap was assembled on the system, the system works as above.
- The maximum impedance achieves to 38 ohm

Optimization structure



- Whole system including Cdie, package, caps on package, board and caps on board was consider as a whole.
- 3D EM solver was used to do optimization.

Performance vs. Cost



- The best performance vs. least cost design will be found automatically by OptimizePI.

Optimization process

[Load a new/current Layout](#)
[Load/Edit Capacitor Library](#)
[Unload a Pre-computed Data File](#)

Stackup
[Check Stackup](#)

Ports
[Select Ports](#)

Circuit Models
[Define Circuit Models](#)

Model for Simulation
 VRM
[Decoupling Capacitors](#)
[Impedance Observations](#)
[Other Circuits](#)
[Frequency/Time Range](#)

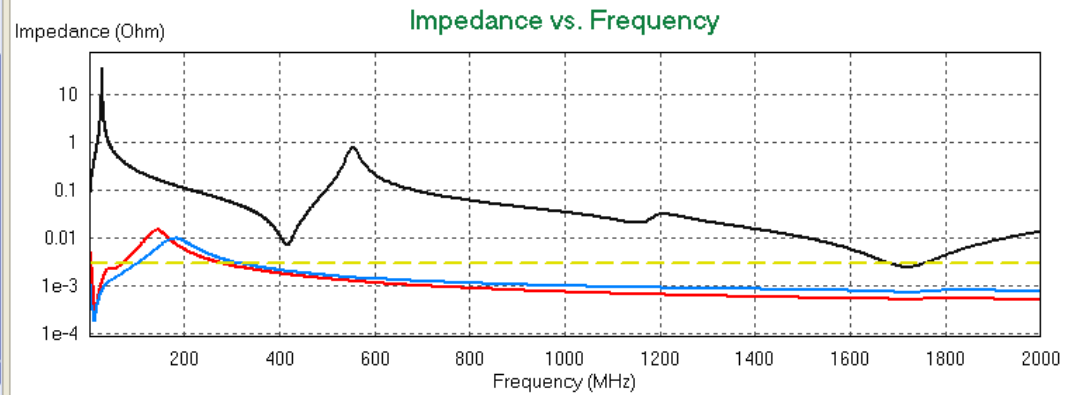
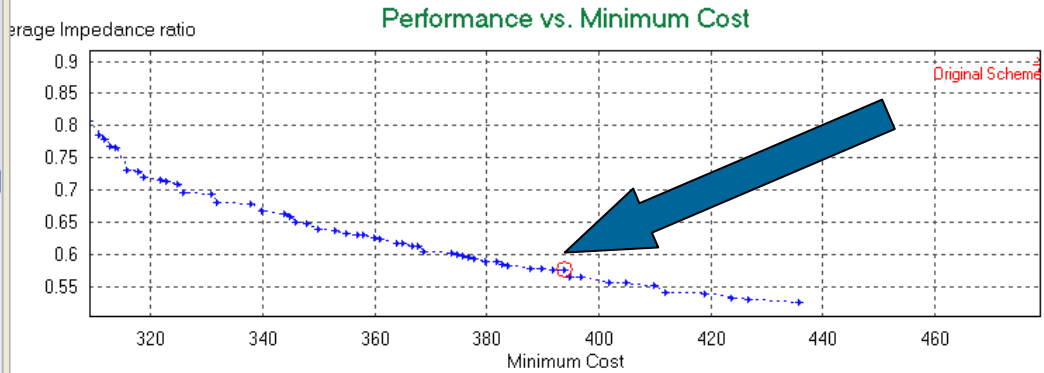
Simulation Type
[Type: Optimization/What-if Analysis](#)
[Optimization Parameters](#)

Results
[View Optimization Results](#)
[Save Optimization Results](#)
[Load Optimization Results](#)

Show No Capacitor
 Show Relative Values to Original Scheme
 Draw Placement on Layout View

Scheme ID	Cost	Impedance ratio in log scale
Scheme 26	360	0.626429
Scheme 27	361	0.623621
Scheme 28	364	0.616769
Scheme 29	365	0.616508
Scheme 30	367	0.613341
Scheme 31	368	0.61246
Scheme 32	369	0.604141
Scheme 33	374	0.603009
Scheme 34	375	0.59914
Scheme 35	376	0.597252
Scheme 36	377	0.596049
Scheme 37	378	0.592961
Scheme 38	380	0.588928
Scheme 39	382	0.588756
Scheme 40	383	0.585252
Scheme 41	384	0.583742
Scheme 42	388	0.579139
Scheme 43	390	0.577297
Scheme 44	392	0.576591
Scheme 45	394	0.576314
Scheme 46	395	0.566135
Scheme 47	397	0.565844
Scheme 48	402	0.556658
Scheme 49	405	0.555485
Scheme 50	410	0.5517
Scheme 51	412	0.541832
Scheme 52	419	0.540115
Scheme 53	424	0.533242
Scheme 54	427	0.531355
Scheme 55	436	0.525731

Output
 Optimizing... (12.1%)
 Optimizing... (12.2%)
 Optimizing... (12.3%)
 Optimizing... (12.4%)



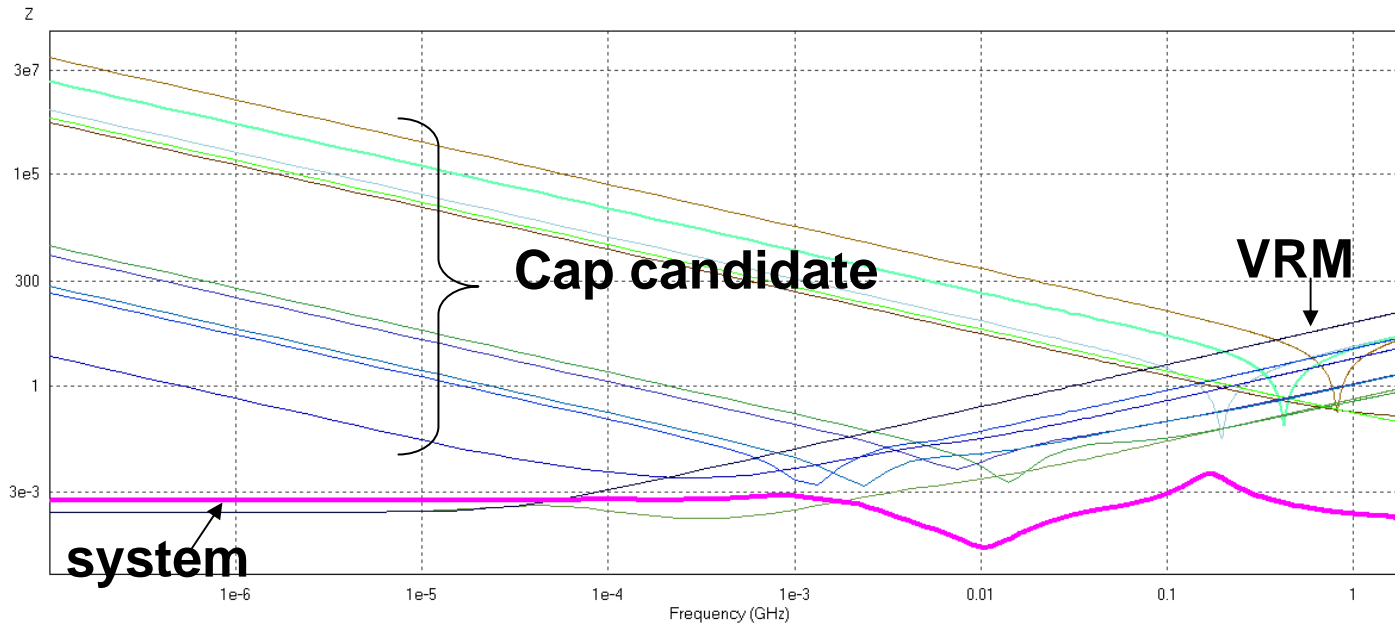
- Optimization is in processing.
- Several scheme will be provided with different performance and cost.

Placement

Scheme ID	Cost	Impedance	C1_	C2_	C3_	C4_	C5_	C6_	C7_	C8_	C9_	C10_	C11_	C12_	C13_	C14_	C15_	C16_	C17_	C18_	C19_	C20_	C21_	C22_	C23_
Scheme 1	0.201	19.965131	X	4	X	X	X	X	2	X	2	X	X	X	X	4	4	X	X	X	X	X	3	X	
Scheme 2	0.202	19.918919	X	X	X	X	4	X	X	4	X	X	X	X	X	X	X	X	X	4	3	X	5	3	
Scheme 3	0.21	19.725069	4	X	X	X	X	X	X	3	X	X	2	4	X	X	X	X	2	X	X	X	4	5	4
Scheme 4	0.227	19.676452	X	X	X	5	X	X	X	4	X	2	X	X	2	X	X	X	X	X	X	X	5	4	
Scheme 5	0.229	19.667312	X	X	X	4	X	X	X	X	2	2	4	X	3	X	X	X	X	2	X	X	3	4	
Scheme 6	0.236	19.539375	X	X	X	5	3	X	X	X	2	X	X	4	X	5	4	X	4	4	X	X	X	X	X
Scheme 7	0.237	19.285003	3	X	X	X	X	X	X	4	X	X	X	2	X	X	2	X	X	X	X	3	4	5	3
Scheme 8	0.246	19.259111	X	X	X	4	X	X	2	X	X	X	X	X	X	X	X	X	X	2	X	X	4	4	
Scheme 9	0.256	19.194559	X	4	X	X	X	X	2	X	4	X	X	X	X	4	X	X	X	X	X	X	3	X	
Scheme 10	0.269	18.857856	X	X	X	X	X	2	4	X	X	X	X	3	X	X	X	X	X	X	X	X	1	X	
Scheme 11	0.335	18.755864	X	X	X	5	2	X	X	4	X	X	3	X	5	2	X	X	X	2	X	X	X	X	X
Scheme 12	0.337	18.73206	X	X	X	X	4	2	4	X	X	X	X	3	3	X	X	X	X	3	3	X	1	X	
Scheme 13	0.338	18.702451	X	2	X	X	X	X	3	4	X	X	X	X	X	4	X	X	X	X	5	2	1	3	
Scheme 14	0.35	18.689192	X	X	X	5	X	X	5	X	X	X	X	X	X	X	X	X	X	X	3	X	1	3	
Scheme 15	0.379	18.624997	4	X	4	X	X	X	X	X	X	4	X	X	X	X	X	1	4	X	X	X	5	X	
Scheme 16	0.38	18.620311	2	X	X	X	X	4	3	X	X	X	X	5	4	X	X	X	1	X	X	X	4	1	3
Scheme 17	0.382	18.543074	4	2	X	X	X	X	3	X	X	X	X	3	X	X	3	X	X	4	X	X	2	5	X
Scheme 18	0.385	18.516154	X	1	X	X	5	X	X	X	2	X	X	X	X	4	X	X	X	2	X	4	X	4	
Scheme 19	0.388	18.477548	X	X	X	X	4	4	5	4	4	X	X	X	X	X	X	X	X	X	3	X	1	3	
Scheme 20	0.393	18.427117	X	X	X	5	X	X	X	4	5	X	X	X	5	2	2	X	X	4	X	X	4	4	X
Scheme 21	0.43	18.411733	3	X	X	X	X	X	X	3	X	2	X	X	X	X	X	X	X	5	X	1	3	X	
Scheme 22	0.439	18.296769	X	X	X	X	2	2	5	4	2	X	X	X	X	X	X	X	X	X	3	X	1	3	
Scheme 23	0.46	18.268527	X	X	X	5	X	X	5	X	X	X	X	X	X	X	4	X	X	2	3	X	1	1	
Scheme 24	0.486	18.241662	X	X	4	X	X	X	4	4	X	X	X	X	X	X	X	X	4	X	2	4	1	5	
Scheme 25	0.504	18.20095	3	X	5	X	X	2	X	3	X	X	X	X	X	X	X	5	3	X	X	1	1	2	
Scheme 26	0.514	18.190489	X	5	X	5	X	5	4	X	2	X	X	X	4	X	X	3	3	2	3	X	3	1	X

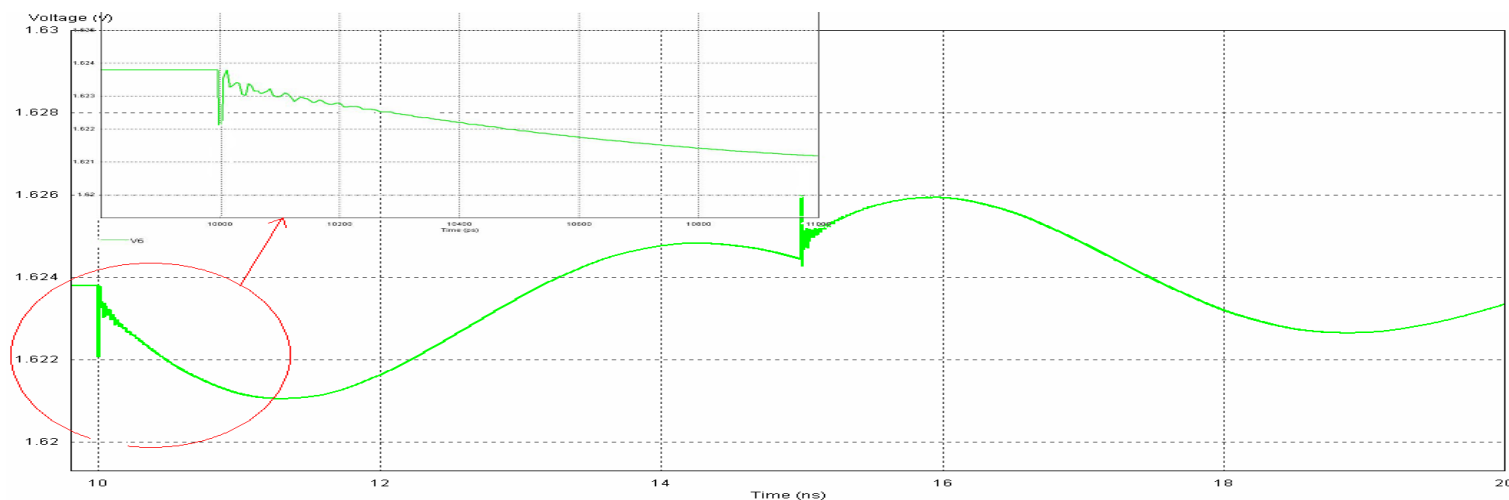
■ The placement of every scheme can be output automatically in table format or in spd format.

Final result in frequency domain



- After optimization, a PDS impedance of less than $5 \text{ m}\Omega$ from DC to 2 GHz is achieved.

Time domain verification



- A step device current source of 1 amp was applied to verify performance in time domain.
- A 50 mV PDS noise voltage results is shown at the active device pins.

Conclusion

- A novel and easily-realized PDS design method was proposed for resonance-free PDS design.
- The 1D EAVP method was used to generate the initial 3D PDS design.
- The initial design was then characterized numerically with 3D EM analysis and subsequently optimized with circuit analysis for maximum performance and minimum cost.
- The time domain noise voltage of this frequency domain Optimized-EVAP method was verified to yield only 50 mV PDS noise.
- This design method is quick and yields 3D PDS designs that are easily implemented with commercially available components.

Reference

- [1] Yao, K.; Ren, Y. and Sun, J., “Adaptive voltage position design for voltage regulators” Applied Power Electronics Conference and Exposition, 2004. IEEE
- [2] Om P. Mandhana, “Effect of Resonant Free Power Delivery Network Design on VRM Performance”, Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE Volume 1, 6-10 March 2005 Page(s):183 - 190 Vol. 1
- [3] Alex Waizman and Chee-Yee Chung, “Resonant Free Power Network Design Using Extended Adaptive Voltage Positioning (EAVP) Methodology”, IEEE Transactions on Advanced Packaging, vol 24, No. 3, August 2001