# Equivalent Radiation Source Extraction Method for System Level EMI and RFI Prediction

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***Abstract*—A novel IC Component level radiation source extraction method is described in this paper. The extracted equivalent current source from the 2.5D full wave simulation is exported out for further 3D full wave system level EMI/RFI prediction. This approach solves high complexity computer system's EMI/RFI prediction challenges. This methodology was demonstrated by using a commercial 2.5D solver to simulate board and package near field emissions during early product design phase. The example used was a 4 inch Intel CK505 GTEM board where measured magnetic field was correlated to simulation. A commercial 3D solver was used for next level simulation and correlation. The methodology shows potential to be a useful tool for predicting near field emission using basic package and board information.**

***Keywords-EMI; near-field; platform ; RFI;***

## I. INTRODUCTION AND BACKGROUD

Today, existing electromagnetic interference (EMI) design and verification techniques are mostly measurement-oriented strategies which utilize conventional approaches such as shielding, grounding, power decoupling, placing absorbing materials, etc [1]. A good EMC design process and evaluation in an earlier stage of a product design chain can significantly reduce the design cycle and better mitigate the EMI and radio frequency interference (RFI) problems from the sources.

However, it is well known that current electromagnetic modeling algorithms running on a desktop computer system with 4GB memory face great challenges to predict EMI of a full computer system, either a desktop or a notebook computer. Although great progress has been made on computational electromagnetics and computer capabilities, so far it is still extremely challenging to model a computer to predict its platform noise and EMI/RFI using straightforward approach such as method of moment (MoM), finite difference time domain method (FDTD), or finite element method (FEM). Furthermore, new faster IO interface introduction such as PCI-Express generation II, requires more meshes in computational domain in order to cover fine 'electrically large' geometries resulting in more memory and computation time requirements. Therefore, a new methodology which can reasonably predict EMI with modest memory requirements and running time is very desirable for platform designers [2].

In DesignCon 2006, Jack Parkes et al [3] presented a joint approach to predict system level EMI by combining 2.5D component level modeling and 3D modeling through Ansoft dynamic link in frequency domain FEM (finite element method). However, this approach doesn't have the flexibility of modeling the non-linear driver due to the lack of a circuit solver. Besides, the 2.5D solver used is a frequency domain solver, which makes it difficult to import time domain excitations.

The objective of this paper is, therefore, to present a novel simulation methodology to study the EMI impact of high-performance packages and printed circuit boards, as well as their radiated emissions, in a complex system environment in an early design phase before a prototype has been manufactured.

The near-field electromagnetic field distribution is generated from the system level time domain simulation of the package and the board. With given excitation sources inside the system, or the switching signal launched on the traces, the current distribution on all surface traces for the entire board and the edge field distribution along the edges of the board are simulated first. Then the near field distribution is calculated from those current distributions. The simulation considers both the power delivery system and the signal transmission system, and the interaction between the two systems. Nonlinear driver and receiver buffer models are used in time domain transient simulation.

Once the near field distribution is generated, such near field distribution can be exported as the equivalent surface current sources for a next level 3D EMI simulation. The next level simulation can be the system level EMI analysis of a chassis with PCBs inside, etc.. Once the equivalent current sources are determined, the fields produced by the sources are calculated under certain assumptions or boundary conditions. "Source Link" technology provides the interface between different EMI simulation tools for calculating the field distribution from the sources under a more realistic environment with certain assumptions. The major analysis steps are summarized as below:

1. Obtain the near field distribution from the board/package simulation using a 2.5D time domain solver
2. Export the equivalent surface current distribution based on the near field distribution through "source link"
3. Calculate 3D field distribution in a next level using a 3D full wave solver

A CK505 clock chip (SLG505YC64L clock synthesizer for Intel PCI-Express chipset) is selected as the device under test (DUT) because it is widely used in Intel's notebook platforms and we applied SPEED2K from Sigrity to predict its near field radiation and extract its equivalent current source for further 3D simulation (CST Microwave Studio, CST MWS). Measured near field scan data were used for the source extraction validation.

## II. CK505 DUT AND SIMULATION MODEL SETUP

The DUT, a CK505 clock chip together with a 4" GTEM test board, measuring 100mm x 100mm was first translated from the layout database and then set up for time domain simulation [4]. The power supply of the board is provided on the back side (Figure 1). Figure 2 shows its TSSOP 64 (Thin Shrink Small Outline Plastic) packaging and its IO and power delivery pin configurations. In our study, we only enabled six PCI related functionality IOs located on its left upper corner such as PCI-0/CLKREQ_A# etc. and two XTAL pins, XTAL_IN and XTAL_OUT (highlighted in the rectangular boxes in Figure 2) on top right. By definition, the six PCI clock pins should perform 33.3MHz periodic clock signals and the two XTAL pins should be running at 14.318MHz.

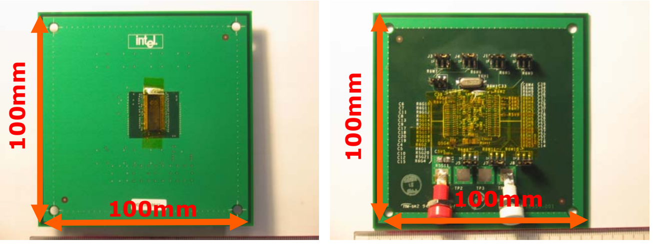


Figure 1. Top nd bottom view of CK505 on a 4" GTEM board

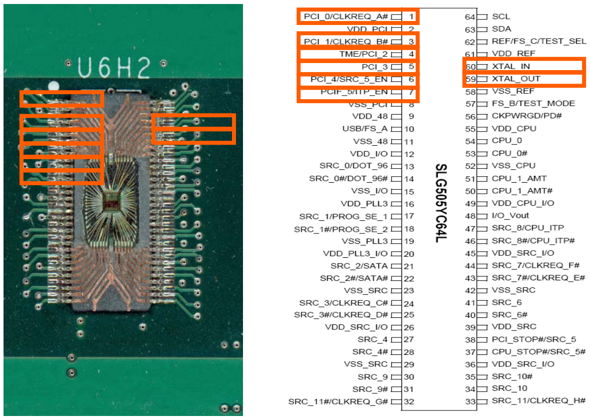


Figure 2. Top view of CK505 for its physical view and its pin map with IO and power/ground

The test board is a 6-layer 4" GTEM board with the main signal routing layers on top and bottom. (Figure 3)

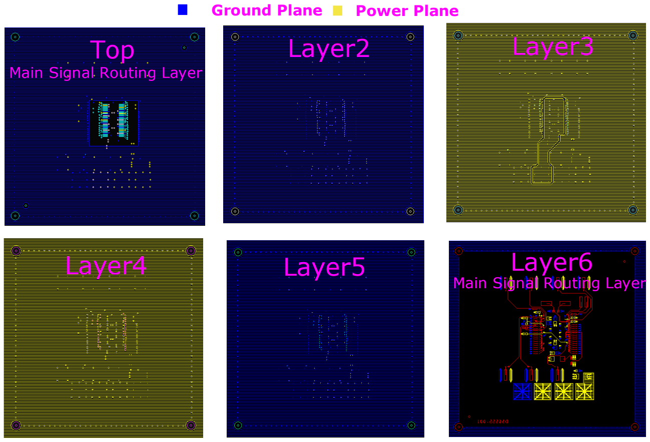
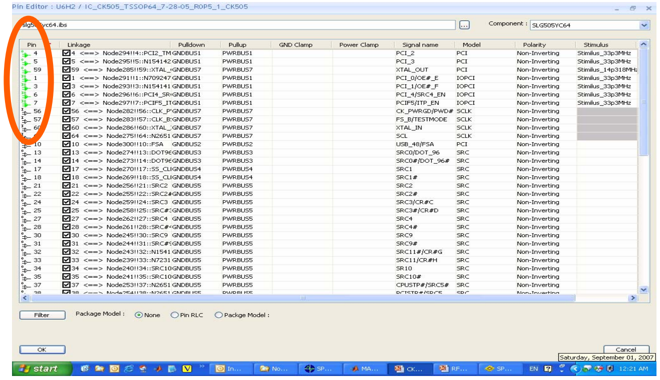


Figure 3. CK505 test board stackups

Six individual PCI and two XTAL IBIS drivers are connected to the ends of the corresponding traces in the center of package for the 6 enabled PCI clocks of 33.33MHz and 2 XTAL clocks of 14.318MHz (Figure 4).


Pin Editor : U6H2 / IC_CK505_TSSOP64_7-28-05_R0P5_1_CK505

slg5[illegible]yc64.ibs

Component : SLG505YC64

| Pin | Linkage | Pulldown | Pullup | GND Clamp | Power Clamp | Signal name | Model | Polarity | Stimulus |
|---|---|---|---|---|---|---|---|---|---|
| 4 | ☑4 <==> Node294!!4::PCI2_TM | GNDBUS1 | PWRBUS1 | | | PCI_2 | PCI | Non-Inverting | Stimulus_33p3MHz |
| 5 | ☑5 <==> Node295!!5::N154142 | GNDBUS1 | PWRBUS1 | | | PCI_3 | PCI | Non-Inverting | Stimulus_33p3MHz |
| 59 | ☑59 <==> Node285!!59::XTAL_ | GNDBUS7 | PWRBUS7 | | | XTAL_OUT | PCI | Non-Inverting | Stimulus_14p318MH |
| 1 | ☑1 <==> Node291!!1::N709247 | GNDBUS1 | PWRBUS1 | | | PCI_0/OE#_E | IOPCI | Non-Inverting | Stimulus_33p3MHz |
| 3 | ☑3 <==> Node293!!3::N154141 | GNDBUS1 | PWRBUS1 | | | PCI_1/OE#_F | IOPCI | Non-Inverting | Stimulus_33p3MHz |
| 6 | ☑6 <==> Node296!!6::PCI4_SR | GNDBUS1 | PWRBUS1 | | | PCI_4/SRC4_EN | IOPCI | Non-Inverting | Stimulus_33p3MHz |
| 7 | ☑7 <==> Node297!!7::PCIF5_IT | GNDBUS1 | PWRBUS1 | | | PCIF5/ITP_EN | IOPCI | Non-Inverting | Stimulus_33p3MHz |
| 56 | ☑56 <==> Node282!!56::CLK_P | GNDBUS7 | PWRBUS7 | | | CK_PWRGD/PWD# | SCLK | Non-Inverting | |
| 57 | ☑57 <==> Node283!!57::CLK_B | GNDBUS7 | PWRBUS7 | | | FS_B/TESTMODE | SCLK | Non-Inverting | |
| 60 | ☑60 <==> Node286!!60::XTAL_ | GNDBUS7 | PWRBUS7 | | | XTAL_IN | SCLK | Non-Inverting | |
| [illegible] | ☑64 <==> Node275!!64::N2651 | GNDBUS7 | PWRBUS7 | | | SCL | SCLK | Non-Inverting | |
| 10 | ☑10 <==> Node300!!10::FSA | GNDBUS2 | PWRBUS2 | | | USB_48/FSA | PCI | Non-Inverting | |
| 13 | ☑13 <==> Node274!!13::DOT96 | GNDBUS3 | PWRBUS3 | | | SRC0/DOT_96 | SRC | Non-Inverting | |
| 14 | ☑14 <==> Node273!!14::DOT96 | GNDBUS3 | PWRBUS3 | | | SRC0#/DOT_96# | SRC | Non-Inverting | |
| 17 | ☑17 <==> Node270!!17::SS_CL | GNDBUS4 | PWRBUS4 | | | SRC1 | SRC | Non-Inverting | |
| 18 | ☑18 <==> Node269!!18::SS_CL | GNDBUS4 | PWRBUS4 | | | SRC1# | SRC | Non-Inverting | |
| 21 | ☑21 <==> Node256!!21::SRC2 | GNDBUS5 | PWRBUS5 | | | SRC2 | SRC | Non-Inverting | |
| 22 | ☑22 <==> Node255!!22::SRC2# | GNDBUS5 | PWRBUS5 | | | SRC2# | SRC | Non-Inverting | |
| 24 | ☑24 <==> Node259!!24::SRC3 | GNDBUS5 | PWRBUS5 | | | SRC3/CR#C | SRC | Non-Inverting | |
| 25 | ☑25 <==> Node258!!25::SRC# | GNDBUS5 | PWRBUS5 | | | SRC3#/CR#D | SRC | Non-Inverting | |
| 27 | ☑27 <==> Node262!!27::SRC4 | GNDBUS5 | PWRBUS5 | | | SRC4 | SRC | Non-Inverting | |
| 28 | ☑28 <==> Node261!!28::SRC# | GNDBUS5 | PWRBUS5 | | | SRC4# | SRC | Non-Inverting | |
| 30 | ☑30 <==> Node245!!30::SRC9 | GNDBUS5 | PWRBUS5 | | | SRC9 | SRC | Non-Inverting | |
| 31 | ☑31 <==> Node244!!31::SRC# | GNDBUS5 | PWRBUS5 | | | SRC9# | SRC | Non-Inverting | |
| 32 | ☑32 <==> Node243!!32::N1541 | GNDBUS5 | PWRBUS5 | | | SRC11#/CR#G | SRC | Non-Inverting | |
| 33 | ☑33 <==> Node239!!33::N7231 | GNDBUS5 | PWRBUS5 | | | SRC11/CR#H | SRC | Non-Inverting | |
| 34 | ☑34 <==> Node240!!34::SRC10 | GNDBUS5 | PWRBUS5 | | | SR10 | SRC | Non-Inverting | |
| 35 | ☑35 <==> Node241!!35::SRC10 | GNDBUS5 | PWRBUS5 | | | SRC10# | SRC | Non-Inverting | |
| 37 | ☑37 <==> Node253!!37::N2651 | GNDBUS5 | PWRBUS5 | | | CPUSTP#/SRC5# | SRC | Non-Inverting | |

Package Model : ● None ○ Pin RLC ○ Packge Model :

Figure 4. IBIS driver configuration in Speed2K generator

Terminations of all enabled signal nets are also provided on board and properly connected in the simulation setup as shown in Figure 5.

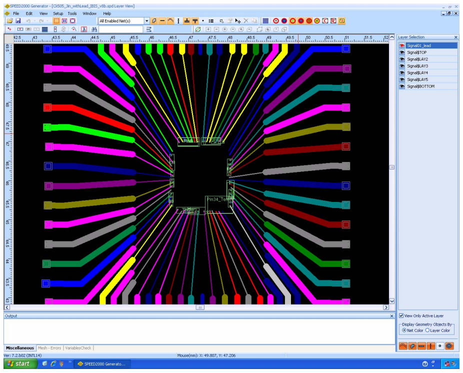


Figure 5. IBIS driver and termination connection in Speed2k generator

## III. DATA ANALYSIS AND VALIDATION

### A. *Time domain signal waveform*

First of all, time domain signal waveforms are being sampled to verify their running behaviors to ensure the accuracy of model set up. Both PCI output clock and XTAL waveforms are recorded and shown in Figure 6 and 7, respectively. In Figure 6, we observed there is some overshoot for these output PCI clocks of 33.33MHz which is not correlated well with measured data due to a few possible reasons such as IBIS model reliability, measurement and simulation error. However, it should not impact the near field radiation we are interested in at 100MHz for this study, because 100MHz is way below the overshoot frequency around GHz. Figure 7 shows the XTAL waveform and good correlation is observed.

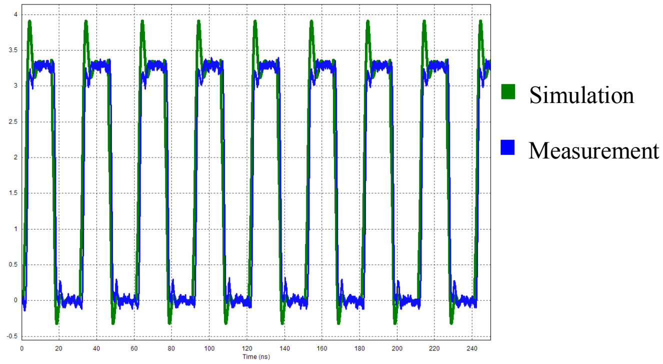


Figure 6. Pin 1 (PCI_0) output waveform

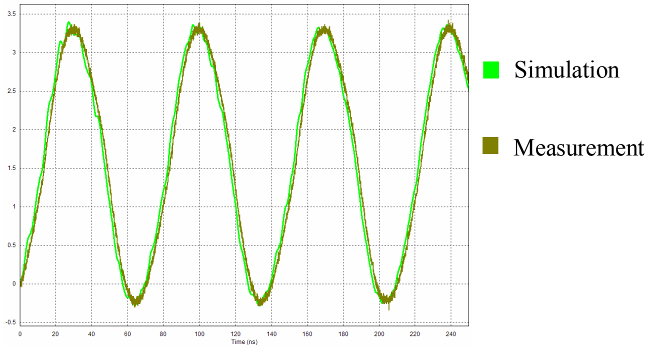


Figure 7. Pin 59 (XTALOUT) output waveform

### B. *Near field scan for magnetic near field correlation*

Based on the 2.5D time domain transient analysis, the frequency domain near-field electromagnetic field distribution at 100MHz is obtained through Fourier transform. A magnetic surface scanning measurement was conducted to correlate the near-field simulation by the 2.5D solver. The near-field scanning measurements were used to correlate the near-field simulation on a same plane 2mm above the DUT at the same frequency and spatial density (Figure 8).

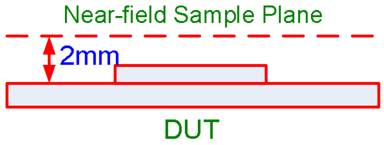


Figure 8. Correlation of the near magnetic field simulation of the DUT

The near field radiation correlation flow and the measurement setup are shown in Figure 9 and 10, respectively. The same PCI clocks and XTALs were enabled in the CK505 measurement setup. The near field scanning was conducted in frequency domain with a center frequency of 100MHz and a resolution bandwidth (RBW) of 1MHz. The actual scanning area was chosen to be the same as the Speed2k simulation, a rectangular area 2mm above the CK505 chip measuring 20mm x 15mm as shown in Figure 11.

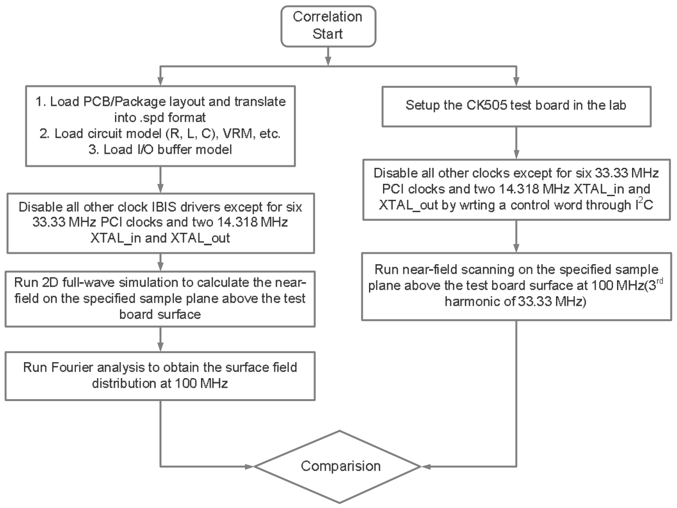


Figure 9. Magnetic near field radiation correlation flow

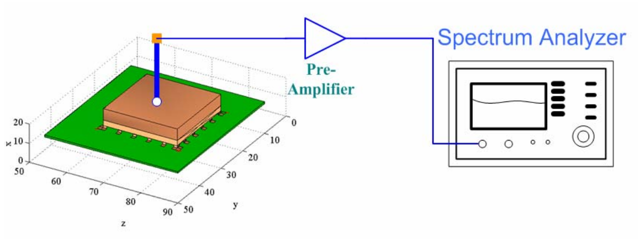


Figure 10. Frequency domain near-field scanning setup

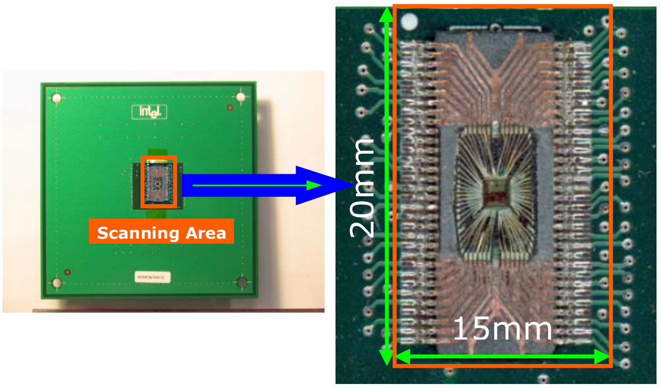
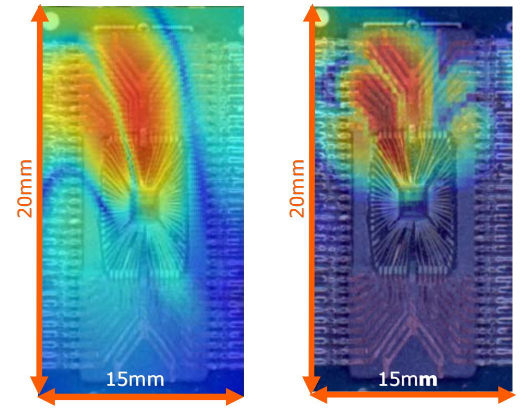


Figure 11. Near field scan area

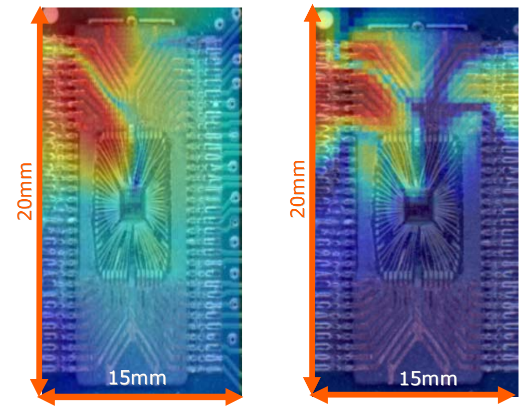
The near field scanning results and Speed2k simulations are compared in Figure 12 and 13 for the x and y components of the magnetic field at 100MHz with a 2mm vertical standoff distance.

The simulated magnetic fields correlate with the measurement very well except for some small discrepancy due to the measurement error introduced by the near-field scanning system. For example, in our simulation, we can ideally assume the board's perfect flatness and our observation plane is perfectly horizonal. However, in the bench top measurement setup, it is very difficult to guarantee the flatness of DUT surface and therefore the distance between the probing dip to surface of DUT may vary which can introduce measurement error. The magnetic field probe will also disturb the field it is measuring due to its physical presence in the field [5]. The non-infinite-small probe loop will average the field it is measuring within its loop area. Therefore, the non-ideal probe will have limited spatial resolution and 'blur' the field it is measuring.



Near-field Scanning Speed2k Simulation

Figure 12. NFS data vs. Speed2K simulation data of Hx at 100MHz with z standoff distance of 2mm



Near-field Scanning Speed2k Simulation

Figure 13. NFS data vs. Speed2K simulation data of Hy at 100MHz with z standoff distance of 2mm

## *C. 3D simulation and correlation*

The equivalent current sources extracted from 2.5D simulation will be imported into a commercial 3D solver, CST MWS, to replace the original DUT (Figure14). At the mean time, if necessary, any interesting 3D complex geometry could be created or imported into the 3D simulation setup with the excitation source selected as the imported field source (Figure 15).

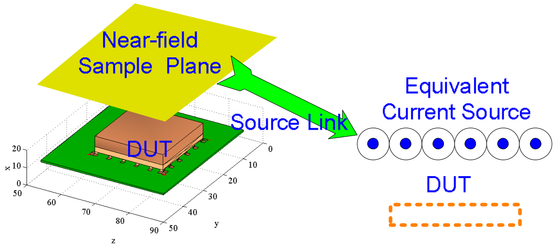
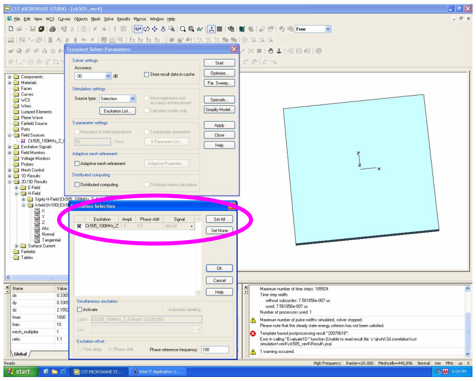


Figure 14. Import of surface current from 2.5D simulation to a 3D solver



Solver settings
Accuracy: -30 dB
☐ Store result data in cache

Stimulation settings
Source type: Selection
☐ Inhomogeneous port accuracy enhancement
☐ Calculate modes only

S-parameter settings
☐ Normalize to fixed impedance 50 Ohms
☐ S-parameter symmetries

Adaptive mesh refinement
☐ Adaptive mesh refinement

Distributed computing
☐ Distributed computing
☐ Distribute matrix calculation

| | Excitation | Ampl. | Phase shift | Signal |
|---|---|---|---|---|
| ☒ | Ck505_100MHz_Z | 1.0 | 0.0 | default |

Simultaneous excitation
☐ Activate
☑ Automatic labeling
Label: Ck505_100MHz_Z_0.8mm[1.0,0.0],[100]

Excitation offset
○ Time delay ● Phase shift
Phase reference frequency: 100

| Name | Value |
|---|---|
| dx | 0.3309 |
| dy | 0.3309 |
| dz | 2.1552 |
| fmax | 1000 |
| fmin | 10 |
| mesh_multiplier | 1 |
| ratio | 1.1 |

```
Maximum number of time steps: 189924
Time step width:
    without subcycles: 7.561856e-007 us
    used: 7.561856e-007 us
Number of processors used: 1
Maximum number of pulse widths simulated, solver stopped.
Please note that the steady state energy criterion has not been satisfied.
Template based postprocessing result "20070618":
Error in calling "Evaluate1D" function (Unable to read result file: c:\jinshi\3d correlation\cst
simulation\ver4\ck505_ver4\Result\.pra)
1 warning occurred.
```

Ready High Frequency Raster=20.000 Meshcells=440,896 Normal mm MHz us K

Figure 15. Excitation selection in CST Microwave Studio time domain solver

To simplify the correlation work load, however, no additional complex 3D geometries were added to the field source in this paper. The magnetic field on a higher sample plane of z=10mm will be compared between the direct 2.5D simulation and indirect 3D simulation along the center line defined in Figure 16. The 3D correlation procedure of the near-field simulation of the DUT is summarized in Figure 17.

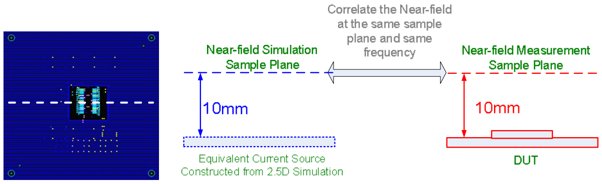


Figure 16. 3D correlation plane definition

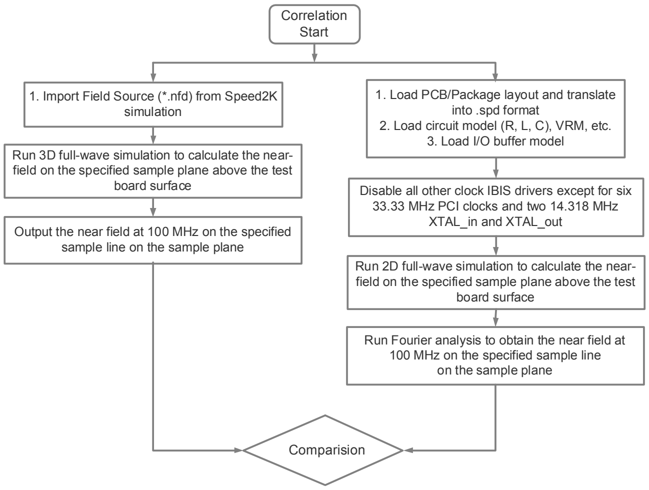


Figure 17. 3D simulation correlation flow

The 3D correlation results along the center sample line (the white dotted line defined in Figure 16) on the sample plane of z=10mm at 100MHz are presented in Figure 18. The direct simuiation results in Speed2K are plotted in red while the indirect simulation in CST MWS using the imported filed source from Speed2K is in blue. It shows a good correlation between the direct simulation result from 2.5D simulation and the indirect 3D simulation.

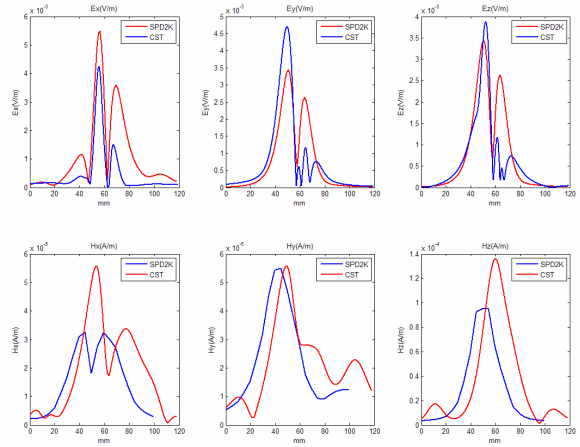


Figure 18. 3D correlation results along the center sample line on the sample plane of z=10mm at 100MHz

## IV. SUMMARY

This study shows how to extract equivalent current source from a 2.5D simulation. A CK505 chip was used as a benchmark for simulation and measurement. Simulated near fields using a 2.5D solver were correlated with measured near field scanning data and fairly good agreement was observed. The direct simulation result from 2.5D simulation also correlated well to the indirect 3D simulation using the imported filed source from Speed2K.

This approach is most useful to obtain equivalent current sources for package and PCBs and incorporating them into full wave 3D simulation domain to reduce its computational complexity for a system level prediction of EMI and RFI.

Based on the successful application in Intel's most recent CPU package and reference board design, this approach is also proven to be very useful in providing quick feedback to the package and board design team by comparing its far/near field radiation strength with FCC standards and RFI limits using the fast 2.5D solver.

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