

An Optimized Cost/Performance PDS Design Using OptimizePI

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Agenda

- ➔ Introduction
- ➔ What Is The Benefit of OptimizePI
- ➔ The Design Flow and Design Experience
- ➔ Verification
- ➔ Conclusion



Introduction

- ➔ With increasing frequency and decreasing noise margin, the power rail integrity is becoming more and more important. The reason is that the voltage variation depends on the $Z(f)$ and $I(f)$.
- ➔ The self-impedance represents the resonance profile at the observed node. The general method to mitigate the high impedance of power/ground rail is to use the de-capacitor.
- ➔ The designer must manually replace/remove de-capacitors to check if both self-impedance and transfer-impedance are improved on traditional simulators. Also, it is a time-consuming job to observe all interesting nodes when each time the cap was changed .
- ➔ If the cost of the design is concerned, the overall capacitor cost needs to be calculated when each time the cap was changed.



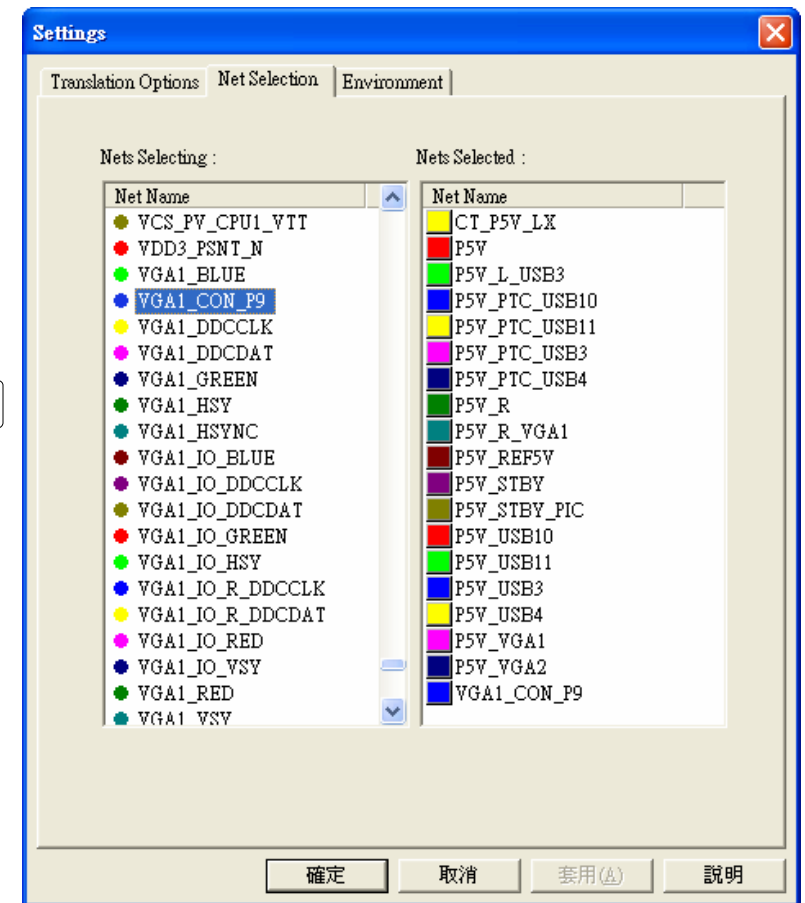
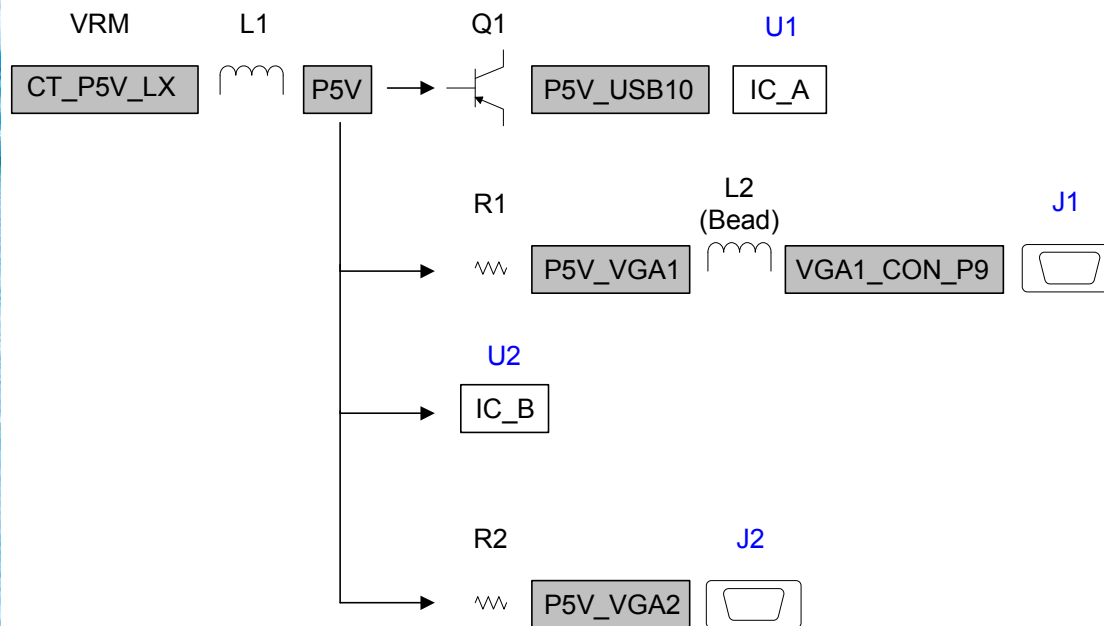
What Is The Benefit of OptimizePI

- ➔ The powerful translator for Allegro-to-OptimizePI.
- ➔ The de-capacitors can be automatically replaced and selected without impact on the layout modification.
- ➔ The performance vs. cost chart is informative for the designer to avoid the over-design.
- ➔ The PDS design can be improved by selecting the specific solutions from numerous design schemes.
- ➔ The available room for the routing can be increased, and the spacing can be utilized for the robust system design.

The Design Flow and Design Experience

→ File Translation

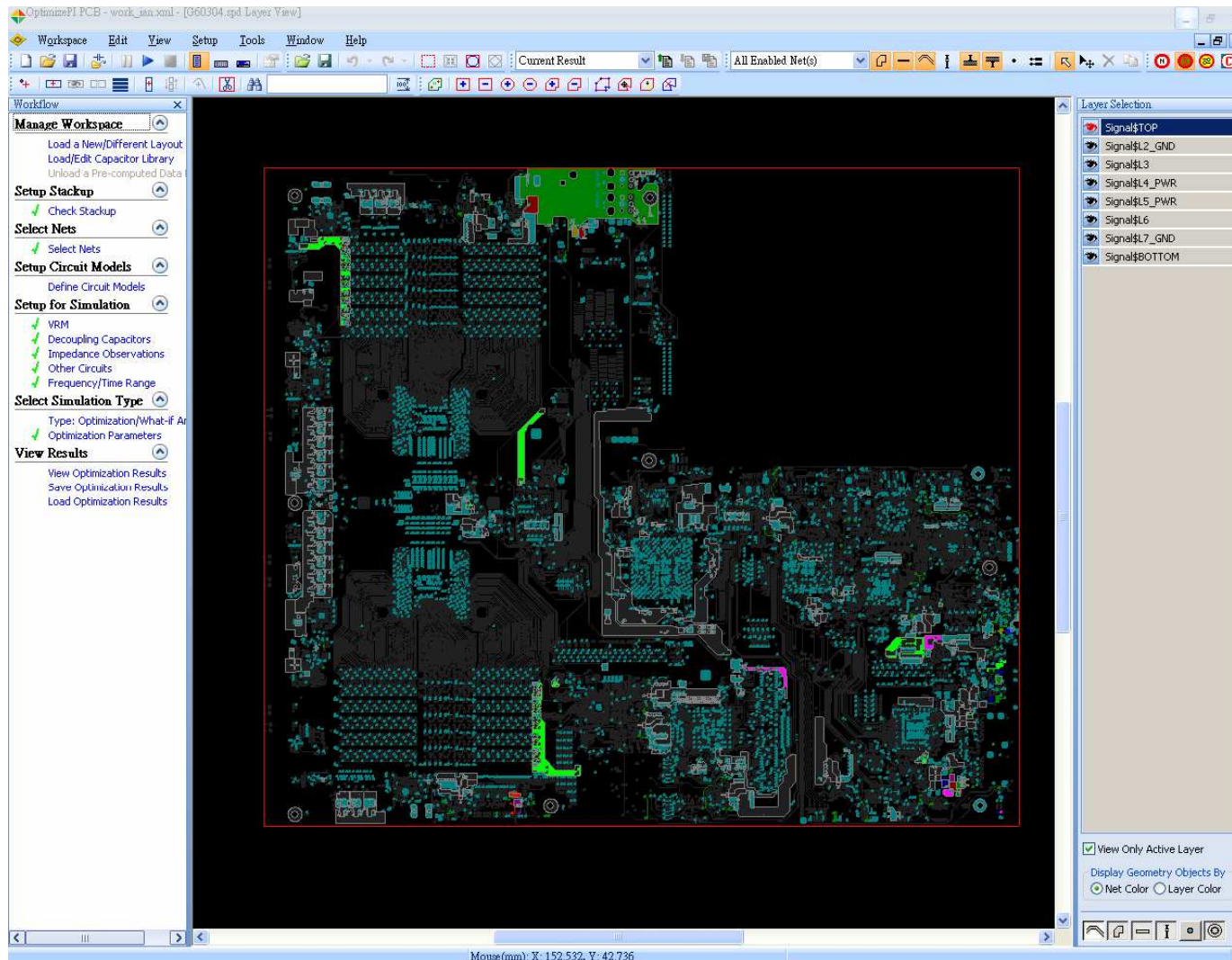
- ➔ Determine which power-tree to be analyzed before the simulation.
- ➔ For the file translation, the insignificant nets can be deselected, and the simulation time can be reduced.



The Design Flow and Design Experience

→ User Interface

➡ The simulation can be completed by the workflow listed below.

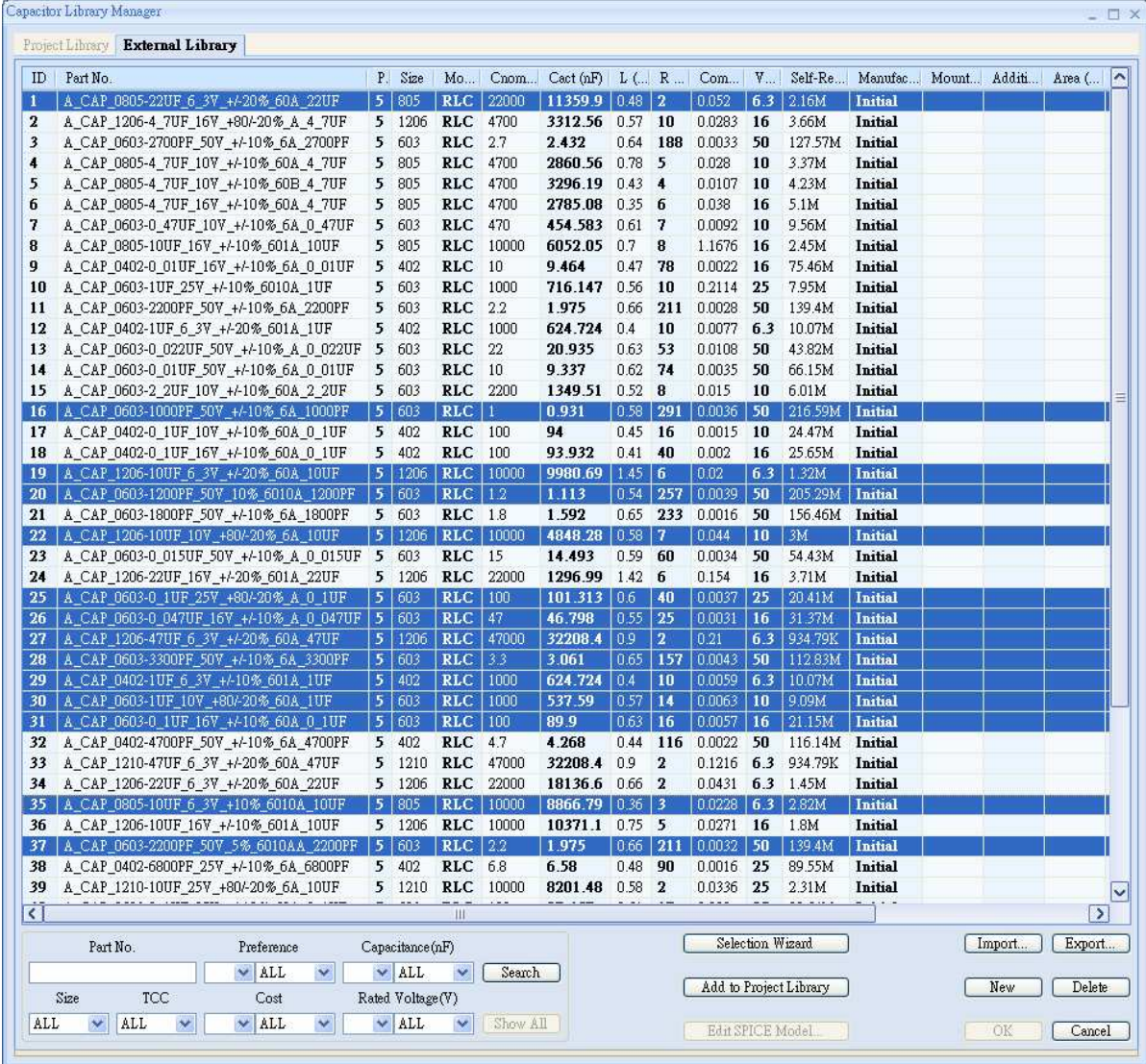


The Design Flow and Design Experience

→ Capacitor Library

→ The capacitor library can be maintained with XML format and it can be reused for any other power rails.

→ There are two capacitor libraries in the Capacitor Library Manager. For the External Library, the count of capacitors is free.



The screenshot shows the 'Capacitor Library Manager' window with the 'External Library' tab selected. It displays a table of capacitor components with various parameters. Below the table are search and filter controls, and buttons for library management.

ID	Part No.	P.	Size	Mo...	Cnom...	Cact (nF)	L (...	R...	Com...	V...	Self-Re...	Manufsc...	Mount...	Addi...	Area (...)
1	A_CAP_0805-22UF_6_3V_+/-20%_60A_22UF	5	805	RLC	22000	11359.9	0.48	2	0.052	6.3	2.16M	Initial			
2	A_CAP_1206-4.7UF_16V_+80/-20%_A_4.7UF	5	1206	RLC	4700	3312.56	0.57	10	0.0283	16	3.66M	Initial			
3	A_CAP_0603-2700PF_50V_+/-10%_6A_2700PF	5	603	RLC	2.7	2.432	0.64	188	0.0033	50	127.57M	Initial			
4	A_CAP_0805-4.7UF_10V_+/-10%_60A_4.7UF	5	805	RLC	4700	2860.56	0.78	5	0.028	10	3.37M	Initial			
5	A_CAP_0805-4.7UF_10V_+/-10%_60B_4.7UF	5	805	RLC	4700	3296.19	0.43	4	0.0107	10	4.23M	Initial			
6	A_CAP_0805-4.7UF_16V_+/-10%_60A_4.7UF	5	805	RLC	4700	2785.08	0.35	6	0.038	16	5.1M	Initial			
7	A_CAP_0603-0.47UF_10V_+/-10%_60A_0.47UF	5	603	RLC	470	454.583	0.61	7	0.0092	10	9.56M	Initial			
8	A_CAP_0805-10UF_16V_+/-10%_60A_10UF	5	805	RLC	10000	6052.05	0.7	8	1.1676	16	2.45M	Initial			
9	A_CAP_0402-0.01UF_16V_+/-10%_6A_0.01UF	5	402	RLC	10	9.464	0.47	78	0.0022	16	75.46M	Initial			
10	A_CAP_0603-1UF_25V_+/-10%_60A_1UF	5	603	RLC	1000	716.147	0.56	10	0.2114	25	7.95M	Initial			
11	A_CAP_0603-2200PF_50V_+/-10%_6A_2200PF	5	603	RLC	2.2	1.975	0.66	211	0.0028	50	139.4M	Initial			
12	A_CAP_0402-1UF_6.3V_+/-20%_60A_1UF	5	402	RLC	1000	624.724	0.4	10	0.0077	6.3	10.07M	Initial			
13	A_CAP_0603-0.022UF_50V_+/-10%_A_0.022UF	5	603	RLC	22	20.935	0.63	53	0.0108	50	43.82M	Initial			
14	A_CAP_0603-0.01UF_50V_+/-10%_6A_0.01UF	5	603	RLC	10	9.337	0.62	74	0.0035	50	66.15M	Initial			
15	A_CAP_0603-2.2UF_10V_+/-10%_60A_2.2UF	5	603	RLC	2200	1349.51	0.52	8	0.015	10	6.01M	Initial			
16	A_CAP_0603-1000PF_50V_+/-10%_6A_1000PF	5	603	RLC	1	0.931	0.58	291	0.0036	50	216.59M	Initial			
17	A_CAP_0402-0.1UF_10V_+/-10%_60A_0.1UF	5	402	RLC	100	94	0.45	16	0.0015	10	24.47M	Initial			
18	A_CAP_0402-0.1UF_16V_+/-10%_60A_0.1UF	5	402	RLC	100	93.932	0.41	40	0.002	16	25.65M	Initial			
19	A_CAP_1206-10UF_6.3V_+/-20%_60A_10UF	5	1206	RLC	10000	9980.69	1.45	6	0.02	6.3	1.32M	Initial			
20	A_CAP_0603-1200PF_50V_10%_60A_1200PF	5	603	RLC	1.2	1.113	0.54	257	0.0039	50	205.29M	Initial			
21	A_CAP_0603-1800PF_50V_+/-10%_6A_1800PF	5	603	RLC	1.8	1.592	0.65	233	0.0016	50	156.46M	Initial			
22	A_CAP_1206-10UF_10V_+80/-20%_6A_10UF	5	1206	RLC	10000	4848.28	0.58	7	0.044	10	3M	Initial			
23	A_CAP_0603-0.015UF_50V_+/-10%_A_0.015UF	5	603	RLC	15	14.493	0.59	60	0.0034	50	54.43M	Initial			
24	A_CAP_1206-22UF_16V_+/-20%_60A_22UF	5	1206	RLC	22000	1296.99	1.42	6	0.154	16	3.71M	Initial			
25	A_CAP_0603-0.1UF_25V_+80/-20%_A_0.1UF	5	603	RLC	100	101.313	0.6	40	0.0037	25	20.41M	Initial			
26	A_CAP_0603-0.047UF_16V_+/-10%_A_0.047UF	5	603	RLC	47	46.798	0.55	25	0.0031	16	31.37M	Initial			
27	A_CAP_1206-47UF_6.3V_+/-20%_60A_47UF	5	1206	RLC	47000	32208.4	0.9	2	0.21	6.3	934.79K	Initial			
28	A_CAP_0603-3300PF_50V_+/-10%_6A_3300PF	5	603	RLC	3.3	3.061	0.65	157	0.0043	50	112.83M	Initial			
29	A_CAP_0402-1UF_6.3V_+/-10%_60A_1UF	5	402	RLC	1000	624.724	0.4	10	0.0059	6.3	10.07M	Initial			
30	A_CAP_0603-1UF_10V_+80/-20%_60A_1UF	5	603	RLC	1000	537.59	0.57	14	0.0063	10	9.09M	Initial			
31	A_CAP_0603-0.1UF_16V_+/-10%_60A_0.1UF	5	603	RLC	100	89.9	0.63	16	0.0057	16	21.15M	Initial			
32	A_CAP_0402-4700PF_50V_+/-10%_6A_4700PF	5	402	RLC	4.7	4.268	0.44	116	0.0022	50	116.14M	Initial			
33	A_CAP_1210-47UF_6.3V_+/-20%_60A_47UF	5	1210	RLC	47000	32208.4	0.9	2	0.1216	6.3	934.79K	Initial			
34	A_CAP_1206-22UF_6.3V_+/-20%_60A_22UF	5	1206	RLC	22000	18136.6	0.66	2	0.0431	6.3	1.45M	Initial			
35	A_CAP_0805-10UF_6.3V_+/-10%_60A_10UF	5	805	RLC	10000	8866.79	0.36	3	0.0228	6.3	2.82M	Initial			
36	A_CAP_1206-10UF_16V_+/-10%_60A_10UF	5	1206	RLC	10000	10371.1	0.75	5	0.0271	16	1.8M	Initial			
37	A_CAP_0603-2200PF_50V_5%_60A_2200PF	5	603	RLC	2.2	1.975	0.66	211	0.0032	50	139.4M	Initial			
38	A_CAP_0402-6800PF_25V_+/-10%_6A_6800PF	5	402	RLC	6.8	6.58	0.48	90	0.0016	25	89.55M	Initial			
39	A_CAP_1210-10UF_25V_+80/-20%_6A_10UF	5	1210	RLC	10000	8201.48	0.58	2	0.0336	25	2.31M	Initial			

The Design Flow and Design Experience

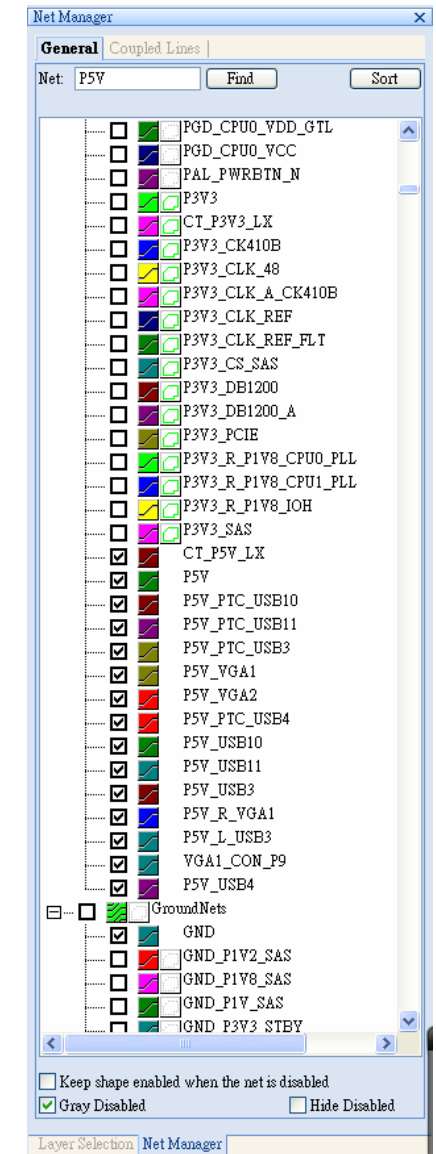
→ Stackup Definition and Net Selection

- ➔ If the PCB cross-section and material information were defined in the layout tool, the design data can be transferred to SPD file for OptimizePI.
- ➔ All following power planes/islands in the specific power tree must be selected in the Net Manager.

Layer Icon	Layer Name	Thickness(mil)	Conductivity(S...	C...	TraceWidth(mil)	Shape Name	Permitti...	Loss Tangent	From File	F
	Medium\$1	4.0000e-001					3.8000	0.0200	<input type="checkbox"/>	
	Signal\$TOP	2.1000e+000	5.8800e+007		3.9370e+000	Shape\$TOP			<input type="checkbox"/>	
	Medium\$3	4.0000e+000					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$L2_GND	1.2000e+000	5.8800e+007		3.9370e+000	Shape\$L2_GND			<input type="checkbox"/>	
	Medium\$5	4.0000e+000					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$L3	1.2000e+000	5.8800e+007		3.9370e+000	Shape\$L3			<input type="checkbox"/>	
	Medium\$7	1.4000e+001					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$L4_PWR	2.4000e+000	5.8800e+007		3.9370e+000	Shape\$L4_PWR			<input type="checkbox"/>	
	Medium\$9	4.0000e+000					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$L5_PWR	2.4000e+000	5.8800e+007		3.9370e+000	Shape\$L5_PWR			<input type="checkbox"/>	
	Medium\$11	1.4000e+001					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$L6	1.2000e+000	5.8800e+007		3.9370e+000	Shape\$L6			<input type="checkbox"/>	
	Medium\$13	4.0000e+000					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$L7_GND	1.2000e+000	5.8800e+007		3.9370e+000	Shape\$L7_GND			<input type="checkbox"/>	
	Medium\$15	4.0000e+000					4.4000	0.0200	<input type="checkbox"/>	
	Signal\$BOTTOM	2.1000e+000	5.8800e+007		3.9370e+000	Shape\$BOT...			<input type="checkbox"/>	
	Medium\$17	4.0000e-001					3.8000	0.0200	<input type="checkbox"/>	

Total Thickness: 6.2600e+001 mil Unit: mil View Material

Import OK Cancel



The Design Flow and Design Experience

→ Circuit Model Definitions

- ➔ Models of VRM, bead, and fuse can be defined in the “Define Circuit Models” for the power plane/island connection. The model can be edited with RLC SPICE format.
- ➔ Please note that capacitor models listed here are just for reference. The simulator would grab capacitor models from the Project Capacitor Library.

Circuit Model	Positive Pin Name	Negative Pin Name
A_CAP_0603-1000PF_50V_+/-10%_6A_1000PF	1	2
A_CAP_1206-10UF_16V_+/-10%_601A_10UF	1	2
A_CAP_1206-10UF_16V_+80/-20%_6A_10UF	1	2
A_CN80_WR805B_VF1_CN80-6012B01A_		
A_DE4PAK_SOIC8-ITA6V5C1RL_6011A_		
A_BEAD_BEAD-4532-130_6014B0023A_130	1	2
A_BEAD_BEAD-1608-60_6014B00331A_60	1	2
A_BEAD_BEAD-0805-2K_6014B00099A_2K	1	2
A_VT234_QFN-VT234WFQX_6019B042A_	6	1
RQ_MODEL	0	1
A_FUSE_B_SMD-0_75A_6013A0096501_	1	2
A_FUSE_B_SMD-1_10A_6013A0096601_	1	2
A_INDUCT_SM-220NH_6014B0087401_220nH	1	2
A_RES_SMT_0402-100K_1%_1/16_60A_100K	2	1
A_RES_SMT_0603-10K_1%_1/10W_60A_10K	2	1
A_RES_SMT_0603-0_5%_1/10W_6013A_0	1	2
A LM393 SOIC8-LM393ADRE4 6019BA		

```
.PartialCkt A_BEAD_BEAD-4532-130_6014B0023A_130 ExtNode = 1 2
L1 1 a 0.04e-6
R1 1 a 28
C1 1 a 0.6e-12
R2 a 2 0.01
.EndPartialCkt
```

The Design Flow and Design Experience

→ VRM Model Setup

- ➔ VRM model can be assigned by using the created model in the “Define Circuit Models”.

The screenshot displays a PCB design software interface. On the left, a 'Workflow' panel lists various tasks, with 'VRM' under 'Setup for Simulation' highlighted. The main workspace shows a PCB layout with a red rectangular area highlighted, indicating the VRM model assignment. Below the workspace, a 'Setup for Simulation -> VRM' table lists circuit names and models. To the right, a tree view shows the hierarchy of the VRM model, including 'PositivePin (CT_P5V_LX)' and 'NegativePin (GND)' with their respective node IDs.

Circuit Name	Circuit Model
U16	A_VT234_QFN-VT234WFQX_6019B042A_

- PositivePin (CT_P5V_LX)
 - Node16518!!17::CT_P5V_LX
 - Node16519!!16::CT_P5V_LX
- NegativePin (GND)
 - Node16509!!11::GND
 - Node16517!!15::GND

The Design Flow and Design Experience

→ Decoupling Capacitor Assignment

- ➔ Capacitor models can be automatically assigned if the layout model name matches the “Part No.” listed in the “Project Library”.
- ➔ If the capacitor is a non-installed type, the capacitor must be deselected.

The screenshot displays the Altium Designer software interface. The main window is titled "OptimizePCB - work_san.xml - [360304.spl Layer View]". The "Capacitor Library Manager" dialog box is open, showing a table of capacitor models in the "Project Library".

ID	Part No.	Prefer...	Size	Model T...	Cnom...	Cact (...	L (nH)	R (m...	Comp...	Mour
1	A_CAP_0603-1000PF_50V_+/-10%_6A_1000PF	5	603	RLC	1	0.931	0.58	291	0.0036	
2	A_CAP_0402-0_1UF_16V_+/-10%_60A_0_1UF	5	402	RLC	100	93.9...	0.41	40	0.002	
3	A_CAP_1206-100F_16V_+/-10%_601A_10UF	5	1206	RLC	10000	103...	0.75	5	0.0271	
4	A_CAP_0402-6800PF_25V_+/-10%_6A_6800PF	5	402	RLC	6.8	6.58	0.48	90	0.0016	
5	A_CAP_0402-0_1UF_16V_+80/-20%_A_0_1UF	5	402	RLC	100	89.2...	0.42	33	0.0012	
6	A_CAP_0603-0_047UF_16V_+80/-20%_A_0_047UF	5	603	RLC	47	49.9...	0.63	49	0.0098	
7	A_CAP_0603-470PF_50V_+/-10%_6A_470PF	5	603	RLC	0.47	0.445	0.56	477	0.0018	
8	A_CAP_0603-100PF_50V_+/-5%_6A_100PF	5	603	RLC	0.1	0.1	0.82	206	0.0036	
9	A_CAP_0402-0_01UF_16V_+/-10%_60A_0_01UF	5	402	RLC	10	9.464	0.47	78	0.0022	
10	A_CAP_0402-0_1UF_10V_+/-10%_60A_0_1UF	5	402	RLC	100	94	0.45	16	0.0015	
11	A_CAP_0402-0_022UF_16V_+/-10%_A_0_022UF	5	402	RLC	22	21.24	0.45	46	0.003	
12	A_CAP_0402-0_015UF_16V_+/-10%_A_0_015UF	5	402	RLC	15	14.7...	0.5	59	0.0018	
13	A_CAP_1206-4_7UF_16V_+80/-20%_A_4_7UF	5	1206	RLC	4700	331...	0.57	10	0.0283	
14	A_CAP_1206-100F_10V_+80/-20%_6A_10UF	5	1206	RLC	10000	484...	0.58	7	0.044	
15	A_CAP_1206-22UF_16V_+/-20%_601A_22UF	5	1206	RLC	22000	129...	1.42	6	0.154	
16	A_CAP_0603-0_47UF_16V_+80/-20%_A_0_47UF	5	603	RLC	47	45.4	0.61	7	0.0098	

The "Setup for Simulation -> Decoupling Capacitors" dialog box is also visible, showing a list of circuit models and their corresponding decoupling IDs. The list includes:

Circuit Name	Circuit Model	Decap ID
C75	A_CAP_1206-100F_16V_+/-10%_601A_10UF	3
C77	A_CAP_1206-100F_16V_+/-10%_601A_10UF	3
C78	A_CAP_1206-100F_16V_+/-10%_601A_10UF	3
C85	A_CAP_1206-100F_16V_+/-10%_601A_10UF	3
C97	A_CAP_1206-100F_16V_+/-10%_601A_10UF	3
C152	A_CAP_0402-0_1UF_16V_+80/-20%_A_0_1UF	5
C158	A_CAP_0603-1000PF_50V_+/-10%_6A_1000PF	1
C159	A_CAP_0603-1000PF_50V_+/-10%_6A_1000PF	1
C160	A_CAP_0603-470PF_50V_+/-10%_6A_470PF	7
C168	A_CAP_0603-470PF_50V_+/-10%_6A_470PF	7
C374	A_CAP_0402-0_1UF_16V_+/-10%_60A_0_1UF	2
C382	A_CAP_0402-0_1UF_16V_+80/-20%_A_0_1UF	5

The Design Flow and Design Experience

→ Impedance Observation Setup

- ➔ The reference impedance and current excitation can be defined for each impedance observation point, and these definitions would affect the optimized result.

Reference Impedance

Circuit Name	Circuit Model	Reference Impedance	Frequency (Hz)	Impedance (Ohm)
J1	A_2X3_CN6-2X3_6012A0105701_			
J14	A_VGACONN_VGA-6012A0063001_			
J18	A_1X6_2MP_26_CN8-1X6_2MP_6026AB_			
J25	A_1X6_2MP_26_CN8-1X6_2MP_6026AA_			
J28	A_SATA_COMBO_2MP_CN13-6012B019A_			
J29	A_2X20_A_2X20_A-6012B0255701_			
J32	A_USBCONN4_CN8-USB_6012B0088501_			
J33	A_USBCONN2_USBCONN2-6012A00633A_			

Current Excitation

Circuit Name	Circuit Model	Excitation Type	Amp(A)	Pulsewidth(ns)	Bandwidth(MHz)	PWL File
J1	A_2X3_CN6-2X3_6012A0105701_	Gaussian pulse	1	1.26667	1500	
J14	A_VGACONN_VGA-6012A0063001_	Gaussian pulse	1	9.5	200	
J18	A_1X6_2MP_26_CN8-1X6_2MP_6026AB_	Gaussian pulse	1	15.2	125	
J25	A_1X6_2MP_26_CN8-1X6_2MP_6026AA_	Gaussian pulse	1	1.52	1250	
J28	A_SATA_COMBO_2MP_CN13-6012B019A_	Gaussian pulse	1	19	100	
J29	A_2X20_A_2X20_A-6012B0255701_	Gaussian pulse	1	1.9	1000	
J32	A_USBCONN4_CN8-USB_6012B0088501_	Gaussian pulse	1	7.91667	240	
J33	A_USBCONN2_USBCONN2-6012A00633A_	Gaussian pulse	1	7.91667	240	

The Design Flow and Design Experience

→ Other Circuits Setup

- ➔ For the transistor, the circuit must be manually created by “Circuit/Linkage manager”, and a DC resistor model can be assigned for the transistor circuit.

The screenshot displays the Altium Designer interface. The main workspace shows a PCB layout with various components. The 'Circuit/Linkage Manager' window is open, showing a list of components and their models. The 'Setup for Simulation -> Other Circuits' window is also open, showing a list of components and their models.

Circuit/Linkage Manager - Model Definition

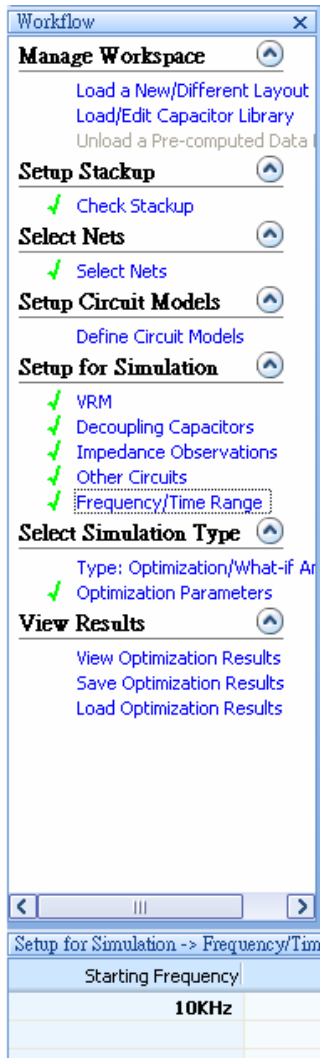
Ckt Name	Ckt Model
RP316	A_SIP8_RS4...
RP317	A_SIP4_SM-0...
RQ25	RQ1
RQ26	RQ1
RQ93	RQ1
RQ227	RQ1
RQ228	RQ1
SW1	A_85WPK_S...
SW4	A_11D_SW6...

Setup for Simulation -> Other Circuits

Circuit Name	Circuit Model
L148	A_BEAD_BEAD-1608-60_6014800331A_60
L222	A_BEAD_BEAD-0805-2K_601480099A_2K
L233	A_BEAD_BEAD-1608-60_6014800331A_60
R622	A_FUSE_B_SMD-0_75A_6013A0096501_
R624	A_FUSE_B_SMD-0_75A_6013A0096501_
R1283	A_FUSE_B_SMD-0_75A_6013A0096501_
R1294	A_FUSE_B_SMD-0_75A_6013A0096501_
R5877	A_FUSE_B_SMD-0_75A_6013A0096501_
R6046	A_FUSE_B_SMD-1_10A_6013A0096601_
R6056	A_RES_SMT_0603-0_5%_1/10W_6013A_0
RQ25	RQ_MODEL
RQ26	RQ_MODEL
RQ93	RQ_MODEL
RQ227	RQ_MODEL
RQ228	RQ_MODEL

The Design Flow and Design Experience

→ Frequency Range Setup



Workflow

- Manage Workspace
 - Load a New/Different Layout
 - Load/Edit Capacitor Library
 - Unload a Pre-computed Data
- Setup Stackup
 - ✓ Check Stackup
- Select Nets
 - ✓ Select Nets
- Setup Circuit Models
 - Define Circuit Models
- Setup for Simulation
 - ✓ VRM
 - ✓ Decoupling Capacitors
 - ✓ Impedance Observations
 - ✓ Other Circuits
 - ✓ Frequency/Time Range
- Select Simulation Type
 - Type: Optimization/What-if Analysis
 - ✓ Optimization Parameters
- View Results
 - View Optimization Results
 - Save Optimization Results
 - Load Optimization Results

Setup for Simulation -> Frequency/Time Range

Starting Frequency	Ending Frequency	Starting Time(ns)	Ending Time(ns)
10KHz	1.5GHz	0	25

- ➔ The frequency range needs to be specified by referring to the bandwidth of current excitation.
- ➔ The “Starting Time” and “Ending Time” also need to be specified if the time-domain verification is needed.
- ➔ Entire simulation setup can be completed by the following workflow.

The Design Flow and Design Experience

→ Power Nets Selection for the Optimization

- ➔ To select the power net with the impedance observation point is the first step of the capacitor optimization.

Select Simulation Type -> Optimization Parameters

Optimization Manager | Decoupling Capacitors | Cost Constraint | Optimization Frequency | Impedance Observations | VRM

Group Name	Net Name
<input checked="" type="checkbox"/> OptimumDefault	Power Nets
	<input checked="" type="checkbox"/> VCC_L_USB11
	<input checked="" type="checkbox"/> VCC_L_USB10
	<input type="checkbox"/> KBVDD
	<input type="checkbox"/> KBMSVDD
	<input type="checkbox"/> MSEVDD
	<input type="checkbox"/> CT_P5V_LX
	<input checked="" type="checkbox"/> P5V
	<input type="checkbox"/> P5V_PTC_USB10
	<input type="checkbox"/> P5V_PTC_USB11
	<input type="checkbox"/> P5V_PTC_USB3
	<input type="checkbox"/> P5V_VGA1
	<input checked="" type="checkbox"/> P5V_VGA2
	<input checked="" type="checkbox"/> P5V_PTC_USB4
	<input type="checkbox"/> P5V_USB10
	<input type="checkbox"/> P5V_USB11
	<input type="checkbox"/> P5V_USB3
	<input type="checkbox"/> P5V_R_VGA1
	<input checked="" type="checkbox"/> P5V_L_USB3
	<input checked="" type="checkbox"/> VGA1_CON_P9
	<input type="checkbox"/> P5V_USB4
	Ground Nets
	<input checked="" type="checkbox"/> GND

The Design Flow and Design Experience

→ Capacitor's Candidate Selection

- ➔ The check mark must be deselected if that capacitor cannot be replacement.
- ➔ The condition of the replaceable capacitor is able to be filtered by using the capacitor's size.

Select Simulation Type -> Optimization Parameters

Optimization Manager **Decoupling Capacitors** | Cost: Constraint | Optimization Frequency | Impedance Observations | VRM

Group Name	Circuit Name	Original ...	Candidate Filter	ID	Manufactu...	PartNo	Size
OptimumDefault	<input type="checkbox"/> C451	3	Same Size	<input checked="" type="checkbox"/> 9	Initial	A_CAP_0402-0_01UF_16V_+/-10%_6A_0_01UF	402
	<input type="checkbox"/> C452	3	Same Size	<input checked="" type="checkbox"/> 10	Initial	A_CAP_0402-0_1UF_10V_+/-10%_60A_0_1UF	402
	<input type="checkbox"/> C453	3	Same Size	<input checked="" type="checkbox"/> 2	Initial	A_CAP_0402-0_1UF_16V_+/-10%_60A_0_1UF	402
	<input type="checkbox"/> C488	3	Same Size	<input checked="" type="checkbox"/> 11	Initial	A_CAP_0402-0_022UF_16V_+/-10%_A_0_022UF	402
	<input checked="" type="checkbox"/> C1823	3	Same Size	<input checked="" type="checkbox"/> 5	Initial	A_CAP_0402-0_1UF_16V_+80/-20%_A_0_1UF	402
	<input checked="" type="checkbox"/> C2518	3	Same Size	<input checked="" type="checkbox"/> 12	Initial	A_CAP_0402-0_015UF_16V_+/-10%_A_0_015UF	402
	<input type="checkbox"/> C2434	4	Same Size	<input type="checkbox"/> 13	Initial	A_CAP_1206-4_7UF_16V_+80/-20%_A_4_7UF	1206
	<input checked="" type="checkbox"/> C152	5	Modified	<input type="checkbox"/> 22	Initial	A_CAP_0603-2700PF_50V_+/-10%_6A_2700PF	603
	<input type="checkbox"/> C382	5	Modified	<input type="checkbox"/> 16	Initial	A_CAP_0603-0_47UF_10V_+/-10%_6A_0_47UF	603
	<input checked="" type="checkbox"/> C808	5	Modified	<input type="checkbox"/> 23	Initial	A_CAP_0603-1UF_25V_+/-10%_6010A_1UF	603
	<input type="checkbox"/> C862	5	Modified	<input type="checkbox"/> 24	Initial	A_CAP_0603-2200PF_50V_+/-10%_6A_2200PF	603
	<input type="checkbox"/> C863	5	Modified	<input type="checkbox"/> 25	Initial	A_CAP_0603-0_022UF_50V_+/-10%_A_0_022UF	603
	<input type="checkbox"/> C892	5	Modified	<input type="checkbox"/> 26	Initial	A_CAP_0603-0_01UF_50V_+/-10%_6A_0_01UF	603
	<input checked="" type="checkbox"/> C997	5	Modified	<input type="checkbox"/> 17	Initial	A_CAP_0603-2_2UF_10V_+/-10%_60A_2_2UF	603
	<input checked="" type="checkbox"/> C998	5	Modified	<input type="checkbox"/> 1	Initial	A_CAP_0603-1000PF_50V_+/-10%_6A_1000PF	603
	<input checked="" type="checkbox"/> C999	5	Modified	<input type="checkbox"/> 27	Initial	A_CAP_0603-1200PF_50V_10%_6010A_1200PF	603
	<input checked="" type="checkbox"/> C1824	5	Modified	<input type="checkbox"/> 28	Initial	A_CAP_0603-1800PF_50V_+/-10%_6A_1800PF	603
	<input checked="" type="checkbox"/> C2520	5	Modified	<input type="checkbox"/> 14	Initial	A_CAP_1206-10UF_10V_+80/-20%_6A_10UF	1206
	<input checked="" type="checkbox"/> C2551	5	Modified	<input type="checkbox"/> 29	Initial	A_CAP_0603-0_015UF_50V_+/-10%_A_0_015UF	603
	<input type="checkbox"/> C844	5	Same or Smaller...	<input type="checkbox"/> 15	Initial	A_CAP_1206-22UF_16V_+/-20%_601A_22UF	1206
	<input type="checkbox"/> C836	6	Same Size	<input type="checkbox"/> 30	Initial	A_CAP_0603-0_1UF_25V_+80/-20%_A_0_1UF	603
	<input type="checkbox"/> C837	6	Same Size	<input type="checkbox"/> 18	Initial	A_CAP_0603-0_047UF_16V_+/-10%_A_0_047UF	603
	<input type="checkbox"/> C838	6	Same Size	<input type="checkbox"/> 19	Initial	A_CAP_0603-1UF_10V_+80/-20%_60A_1UF	603
	<input type="checkbox"/> C888	6	Same Size	<input type="checkbox"/> 20	Initial	A_CAP_0603-0_1UF_16V_+/-10%_60A_0_1UF	603

Select Capacitors on Layout | View Capacitor Library | OK | Cancel

The Design Flow and Design Experience

→ Cost Constraint and Optimization Frequency

- ➔ If the optimization result is not good as expected, to adjust cost constraint may be able to improve the optimization result.
- ➔ The optimization frequency range must be the same or smaller than the defined simulation frequency range.

Select Simulation Type -> Optimization Parameters			
Optimization Manager	Decoupling Capacitors	Cost Constraint	Optimization Frequency Impedance Observations VRM
Group Name	Original Cost	Min Cost	Max Cost
OptimumDefault	0.0658	0.017	0.06909

Select Simulation Type -> Optimization Parameters			
Optimization Manager	Decoupling Capacitors	Cost Constraint	Optimization Frequency Impedance Observations VRM
Group Name	Starting Frequency	Ending Frequency	
OptimumDefault	10KHz	1GHz	

The Design Flow and Design Experience

→ Optimization Settings of Impedance Observation

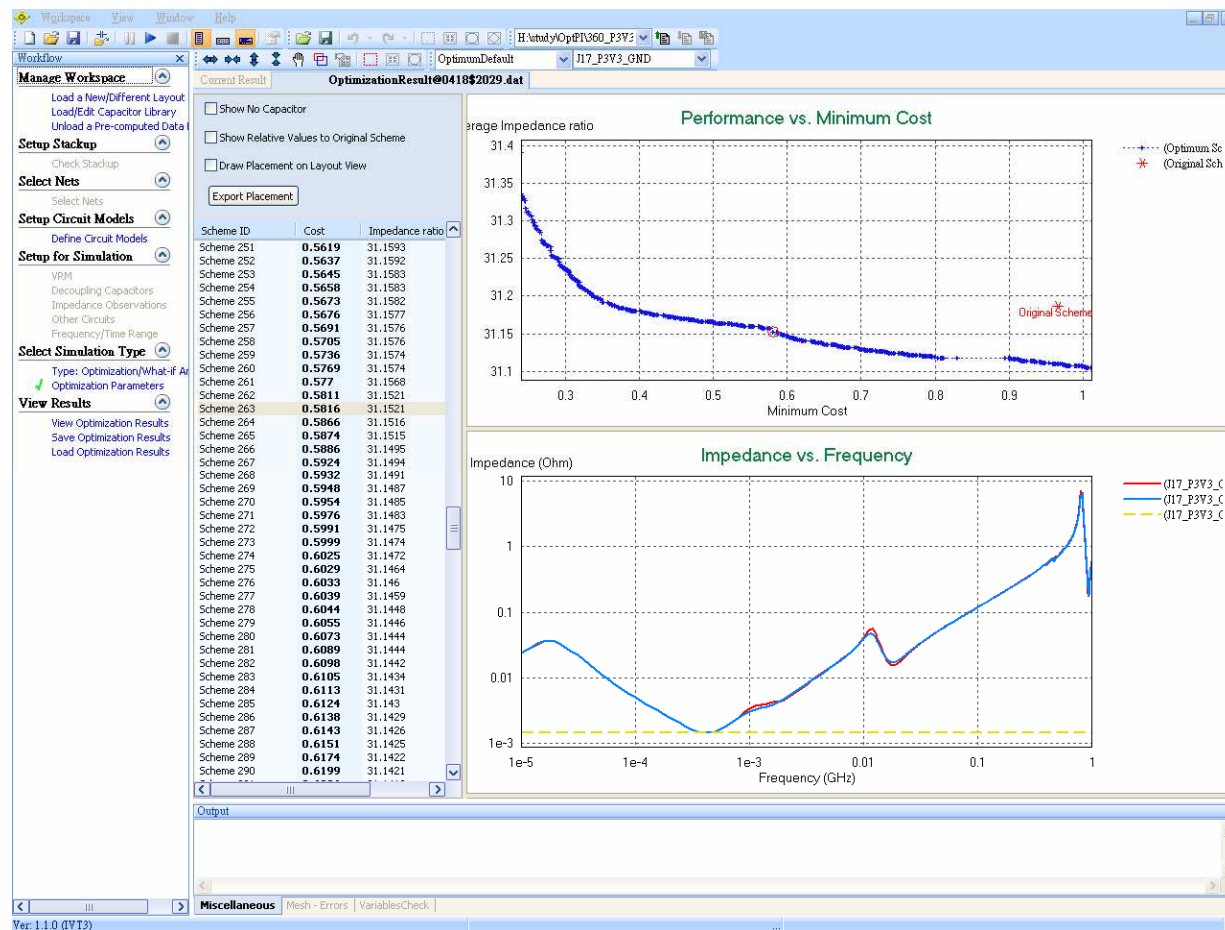
- ➔ The “Weighting” can help the simulator to determine how we concern on each impedance observation point. The weight setup is able to refer to the information of the power consumption.

Select Simulation Type -> Optimization Parameters						
Optimization Manager		Decoupling Capacitors	Cost Constraint	Optimization Frequency	Impedance Observations	VRM
Group Name	Circuit Name	Original Model	New Model		Weighting	
OptimumDefault	J1	A_2X3_CN6-2X3_6012A0105701_	@Open@		1	
	J14	A_VGACONN_VGA-6012A0063001_	@Open@		0.75	
	J28	A_SATA_COMBO_2MP_CN13-6012B019A_	@Open@		1	
	J29	A_2X20_A_2X20_A-6012B0255701_	@Open@		0.5	
	J32	A_USBCONN4_CN8-USB_6012B0088501_	@Open@		0.3	
	J33	A_USBCONN2_USBCONN2-6012A00633A_	@Open@		0.2	

The Design Flow and Design Experience

→ Optimization Result Review

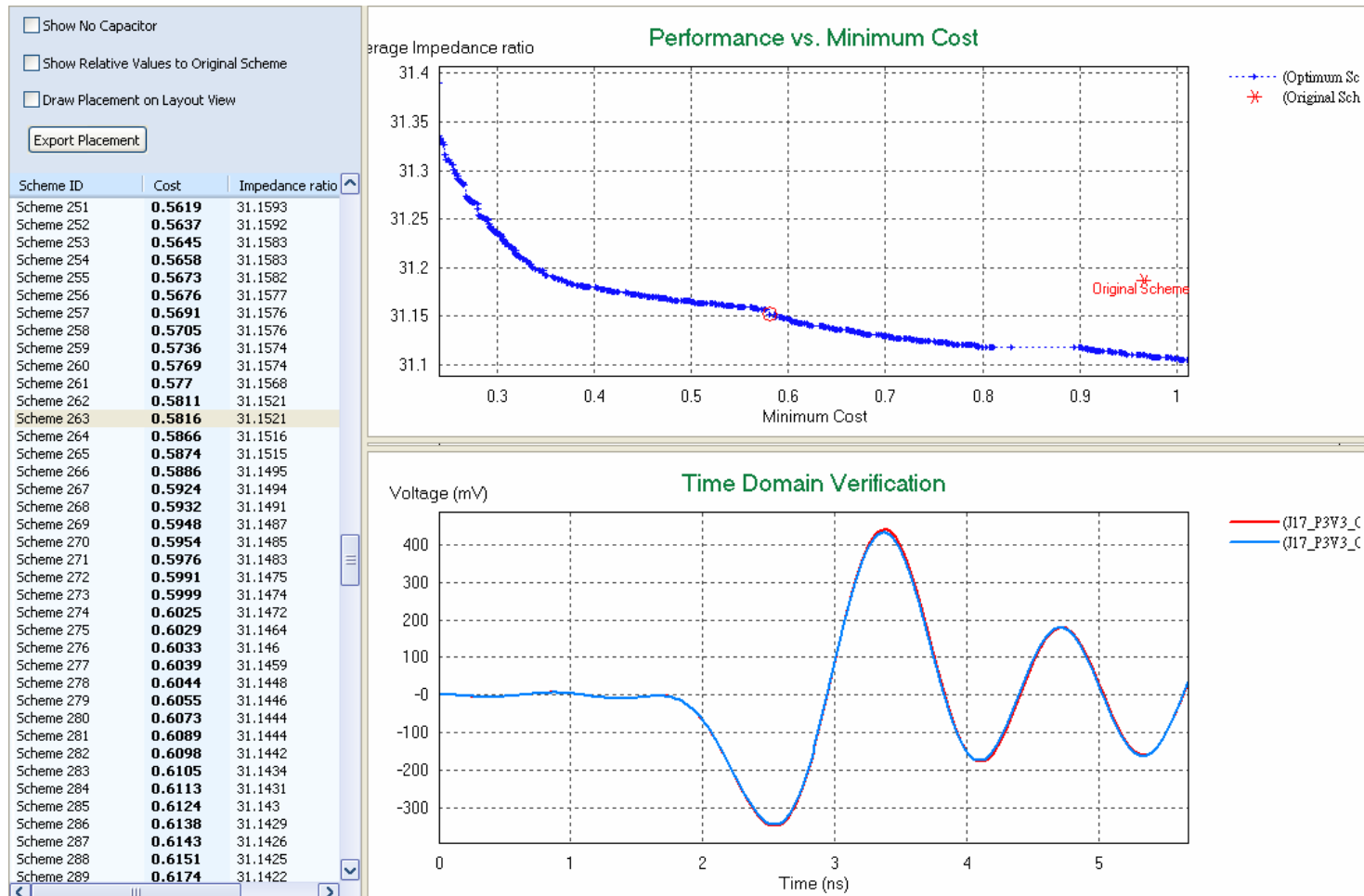
- ➔ A Performance vs. Cost chart is able to provide user numerous solutions/scheme for the capacitor replacement.
- ➔ The impedance plot can be used to compare the self-impedance of original design with the self-impedance of each scheme.



The Design Flow and Design Experience

→ Time Domain Verification

- ➔ For the impedance plot, if it is difficult to know which scheme is the appropriate solution for the design consideration, the time domain verification can help the user make the decision.



The Design Flow and Design Experience

→ Placement Report

- ➔ An Excel format report can be generated, and the capacitor replacement table of each scheme is listed.
- ➔ The table can be translated for user's format, and the updated list can be used for manufacture.

Case	Original	Opt 1	Opt 2
Cost	0.1368	0.0574	0.1024
Cost reduction in %	0.00%	58.04%	25.15%
C152	6010A0036501	6010A0036501	6010A003620G
C382	6010A0036501	Remove	Remove
C808	6010A0036501	6010A0036501	6010A003620G
C836	60100747332T	6010A0044501	6010A0044501
C837	60100747332T	6010A0044501	6010A0044501
C838	60100747332T	Remove	6010A0044501
C888	60100747332T	6010A0044501	6010A0044501
C889	60100747332T	Remove	6010A0044501
C890	60100747332T	6010A0044501	6010A0044501
C892	6010A0036501	6010A0036501	6010A003620G
C893	60100747332T	Remove	6010A0044501
C997	6010A0036501	6010A0036501	6010A0036403
C998	6010A0036501	6010A0036501	6010A0036501
C999	6010A0036501	6010A0036501	6010A0036501
C1823	6010A0044601	Remove	6010A0044601
C1824	6010A0036501	6010A003620G	6010A003620G
C2518	6010A0044601	6010A0044601	6010A0044601
C2520	6010A0036501	6010A0036501	6010A003620G
C2530	6010A0036403	Remove	6010A0036501
C2551	6010A0036501	6010A0036501	6010A003620G

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S
1	Scheme ID	Cost	Impedance ratio	C511	C661	C671	C701	C797	C1003	C1145	C1146	C1147	C1148	C1149	C1154	C1959	C1960	C2047	C204
2	Scheme 1	0.24	31.3905	6	5	5	6	6	X	5	6	6	6	9	6	5	6	24	6
3	Scheme 2	0.2401	31.3357	9	5	X	6	6	X	X	6	X	6	6	X	6	6	24	6
4	Scheme 3	0.2407	31.3337	6	6	X	6	6	X	17	6	X	6	6	X	5	6	24	6
5	Scheme 4	0.2415	31.3336	6	6	X	6	6	X	17	6	X	6	6	X	5	6	24	6
6	Scheme 5	0.2417	31.3331	6	2	X	5	6	X	17	6	X	6	6	X	5	6	24	6
7	Scheme 6	0.2421	31.3317	6	5	X	6	6	X	17	6	6	6	6	X	6	6	24	6
8	Scheme 7	0.2423	31.3292	6	5	X	6	6	X	6	6	X	6	6	X	5	6	24	6
9	Scheme 8	0.2449	31.3291	6	5	X	6	6	X	X	6	X	6	6	19	5	6	24	6
10	Scheme 9	0.2452	31.3268	6	9	X	6	6	X	17	6	X	6	6	X	6	6	24	6
11	Scheme 10	0.2471	31.3165	9	5	X	6	6	X	X	6	X	6	6	X	6	6	24	6
12	Scheme 11	0.2482	31.3112	6	5	X	6	6	X	X	6	X	6	6	X	6	6	24	6
13	Scheme 12	0.2514	31.3108	6	6	X	6	6	X	X	6	6	6	6	X	6	6	24	6
14	Scheme 13	0.2521	31.308	17	6	X	6	6	X	X	6	X	6	6	X	6	6	24	6
15	Scheme 14	0.2549	31.3058	6	2	X	6	6	X	X	6	X	6	6	X	6	6	24	6
16	Scheme 15	0.2561	31.3014	9	5	X	6	6	X	X	6	X	6	6	X	6	6	24	6

Verification

→ Power Noise Measurement (3.3V Rail)

- It is recommended to create an updated BOM for the chosen scheme, and the manufacture is able to install those capacitors by SMT process.
- The verification of 3.3V power rail is based on the manually re-work. Therefore the measurement result includes the adverse parasitic of solder.





Conclusion

- ➔ It is very easy to use OptimizePI for the PDS analysis and the simulation can be completed by the listed workflow.
- ➔ OptimizePI can automatically replace/remove capacitors, and it would save lots of engineering time.
- ➔ Both frequency and time domain responses can be observed for the PDS analysis.
- ➔ OptimizePI is able to avoid costly over-design.
- ➔ OptimizePI helps engineers find a better solution for the robust PDS design.