

Low Cost DTV-SoC System Implementation Using Integrated Signal Integrity Analysis

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Abstract— Analysis of Signal Integrity and Power Integrity are very important to fill the gap between the high performance and the low cost of the DTV system including chip, package and board. In this paper, an integrated signal integrity analysis method which comprises the interaction among power networks, signal operations, and circuit structures of the full system is introduced. The experimental results present excellent correlation between the measurement and results of simulations. The proposed approach is an effective leverage to determine the performance of the system before manufacturing.

I. INTRODUCTION

In recent years, due to a strong price cutting race in digital home appliances market, the low cost of product is considered as a major important issue in those companies. To reduce the cost of products, the chip companies make every effort to develop products using the sub-micron process such as 90nm and 65nm. In case of system companies, they tend to persevere in their effort to reduce PCB layers, PCB size and the number of components for reducing the cost of products. As a result, the performance of the products such as Signal Integrity(SI) and Power Integrity(PI) are getting worse.

Therefore, to fill the gap between the high performance and the low cost of the products, SI and PI analyses such as signal distortion, timing, impedance matching, power disturbance so called SSN, EMI and so on are very important. Thus many approaches have been studied for long time in the many papers [1, 2, 3, 4, 5]. Particularly, to increase the accuracy of the SI analysis, the effects of PI such as Simultaneously Switching Output(SSO) should be considered with full system including chips, packages and boards [6, 7, 8].

In this paper, the low cost DTV system that consists of a 65nm-process SoC(System on a chip) and a 2-layer board had been developed using integrated SI analysis that comprises interaction among power networks, signal operations, and circuit structures of the full system under SSO condition.

Fig. 1 shows the detailed DTV system that had been developed. The DDR interface is the most critical part in this system, so integrated SI analysis focuses on it.

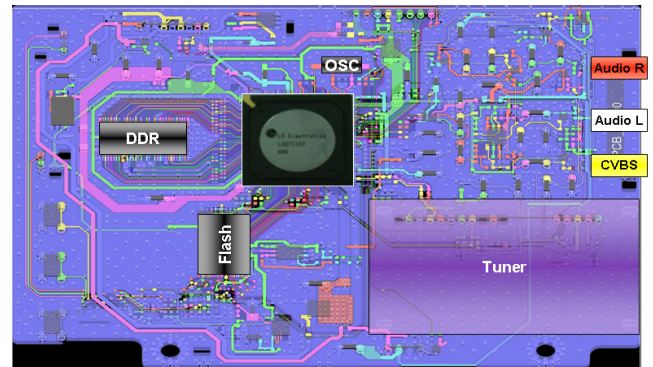


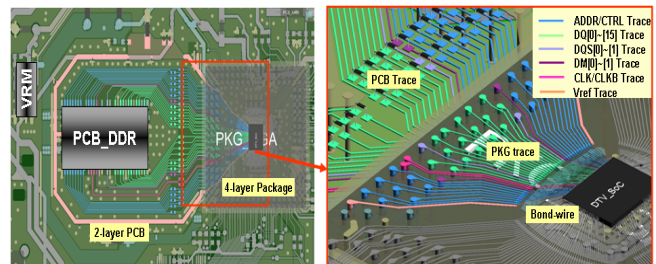
Fig. 1 EUT : CECB System

II. ANALYSIS OF DDR IO INTERFACE

The DDR Interface consists of a 65nm-process SoC, a 4-layer BGA package, and a 2-layer system PCB. Fig. 2 shows their details of the layout and stack-ups of the package and the board.

In this paper, at the early design stage of a DTV SoC, IO pads are selected by the simulation results based on the s-parameter data and RC values which are respectively extracted from the merged layout data of packages and boards, and from the spice-netlists of IO pads. For this analysis of IO pads, impedance matching, overshoot/undershoot, timing, numbers of power pads and SSN is simulated using HSPICE .

For the final integrated SI analysis, full package and PCB layout information are merged and simulated. In case of chips such as the DTV SoC and the DDR memory, IBIS [11] models are used to reduce the simulation efforts. In this paper, Speed2000 is used for this purpose.



Layer Icon	Layer Name	Thickness(mm)	Shape Name	Permittivity
	Medium_PKG_Mold	1.1700e+000		3.6500
	Signal_PKG_Bondwire	1.0000e-003		
	Medium_PKG_Solder	3.0000e-002		3.5500
	Signal_PKG_Top	2.2000e-002	PKG_Top	
	Medium_PKG_DIELECTRIC1	1.0000e-001		4.5000
	Signal_PKG_GND	3.5000e-002	PKG_GND	
	Medium_PKG_DIELECTRIC2	1.5000e-001		4.1000
	Signal_PKG_POWER	3.5000e-002	PKG_Power	
	Medium_PKG_DIELECTRIC3	1.0000e-001		4.5000
	Signal_PKG_Bottom	2.2000e-002	PKG_Bottom	
	Medium_PKG_Solder	3.0000e-002		3.5500
	Medium_PKG_Ball	5.0000e-001		1.0000
	Signal_PCB_Top	3.5000e-002	PCB_Top	
	Medium_PCB_Dielectric1	1.5244e+000		4.0000
	Signal_PCB_Bottom	3.5000e-002	PCB_Bottom	

Fig. 2 Layout data of merged package and board

A. Analysis of DDR IO pad

At the physical DDR interface design stage of a SoC, the most important thing is to select IO pads and to decide the number of power pads considering SSO condition and die size.

To find the optimal number of power pads and the proper signal pad type, all the combinations of power and signal pads which are available in the target 65nm design library are considered.

1) *IO pad selection*: In the used 65nm process, available DDR IO pads are SSTL2_C1 pad, SSTL2_C2 pad, and SSTL2_C1_Differential pad. If there are enough margins on both timing and voltage swing level at 175MHz operating frequency, the pad with lower driving strength has better performance considering integrated SI, especially SSN and EMI. Since SSTL2_C1 pad has enough timing and voltage margins at 175MHz operating frequency under all corner conditions such as SS, TT and FF as shown in Fig. 3, we selected it for DQ/DQS/DQM IO pad.

Fig. 3 shows simulation results of SI characteristics of SSTL2_C1 pad and SSTL2_C1_differential pad. In general DDR applications, a differential pad is used for CLK/CLKB, but SSTL2_C1_differential pad has over 300ps timing delay at rising and falling edges, which reduces timing margin and causes different CLK/CLKB cross-points (first is 1.11V, second is 1.33V in Fig. 3). This can cause skews and common mode noises comparing to SSTL2_C1.

Therefore, we use SSTL2_C1 pad for all DDR IO signals in our DTV-SoC.

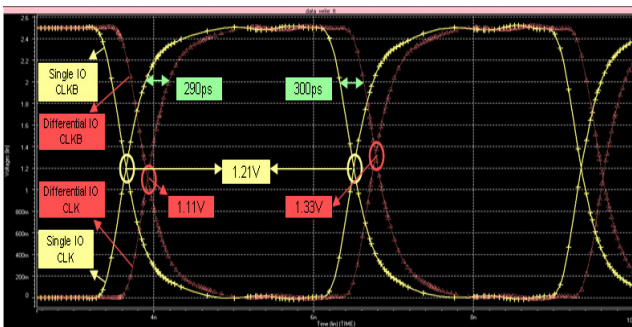


Fig. 3 SSTL_C1 pad vs SSTL_C1_Differential pad

2) *The minimum number of Power pad* : The number of IO pads per power pad affects direct influence to SSN and signal distortion. If the number of power pads is increased, SSN and

signal distortion will be decreased. However, to reduce the die size, it is necessary to decide the minimum number of IO pads per power pads. Fig. 4 and Fig. 5 show the simulation results of SSN and signal distortion considering available SSO conditions. In this experiment, we increase the number of switching signal pads by one, which is supplied by just one power pad. In Fig. 4 and Fig. 5, the case number means the number of SSOs. The result shows that the minimum number of IO pads per power pads is four under the consideration of our SSN specification and die size.

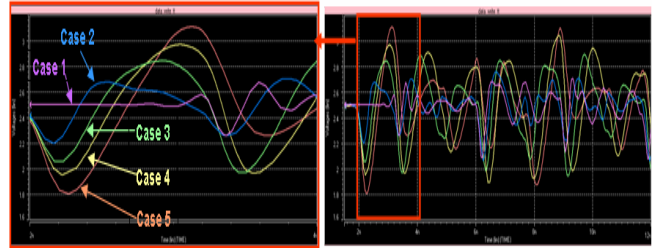


Fig. 4 Power disturbance according to SSO condition

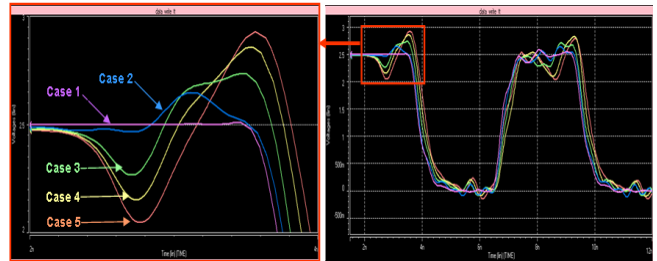


Fig. 5 Signal distortion according to SSO condition

3) *Serial/Termination R value of PCB*: Generally, At the early design stage of a DTV SoC, termination method and component values such as Serial Resistor(R_s) and Terminated Resistor(R_t), are decided for the board design.

In a 2-layer board, if R_t and VTT planes are used, the return current path must be broken due to the spatial problem, so it causes the SI problems such as signal distortion, and EMI[9]. Thus, our product that uses a 2-layer board for cost reduction, just use R_s to ensure the solid return current path.

Fig. 6 shows the simulation result of SI according to R_s values that has varied with 0ohm, 100ohm, 150ohm, and 200ohm. The DDR memory in the board has two different pads such that IO pad for DQ/DQS and Input pad for ADDR/CTL/DMCLK/CLKB, because load conditions are different for one another based on their characteristics. To improve the accuracy of the simulation, those two types of pads are considered for R_s value including SSO condition.

In the result of Fig. 6, 150 or 200ohm has good characteristic of SI, so R_s value is decided as 150ohm. It's the reason that the proper R_s value(150ohm) is higher than the general R_s value(22~33ohm). Similarly the characteristic impedance of designed DDR trace in the 2-layer board is about 140ohm that is also higher than the general 50ohm trace.

And we can see SSN influences the increase of signal distortion.

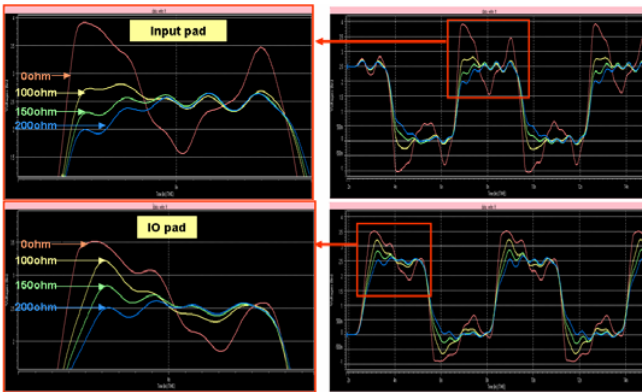


Fig. 6 Rs value tuning considering SSN

B. Analysis of package and board

The first step to minimize SSN is to analyze SSN frequency in time domain followed by a frequency domain analysis for the purpose of reducing impedance at SSN frequency. Also, to increase the accuracy, the impedance of the full power path from the package to the board should be considered.

Fig. 7 shows the simulation result of the worst case SSO condition where DQ[0]~[15]/DQM[0]~[1] signals switch simultaneously and CLK/CLKB/DQS[0]~[2] signals switch simultaneously at the center of high or low state of DQ, so power disturbance and signal distortion are caused at SSN frequency of 175MHz, 234MHz, 350MHz, and 700MHz.

Fig. 8 shows power disturbance and signal distortion according to SSO conditions. Case1 is the case when we only switch DQ 1-bit, and case2 means to switch DQ 8-bit simultaneously. Lastly, simultaneously switching DQ 16-bit is shown in case3.

When the number of SSOs is increased, power disturbance and signal distortion are also increased. Therefore, to improve products' performance and simulation accuracy, we must consider the worst case of SSO conditions such as case 3.

Also, the effective method of reducing SSN is to improve power integrity in the package rather than in the board.

In this section, the effects of power via numbers in a package power ring and of the number of Decoupling Capacitor(Decap) in the package are analyzed.

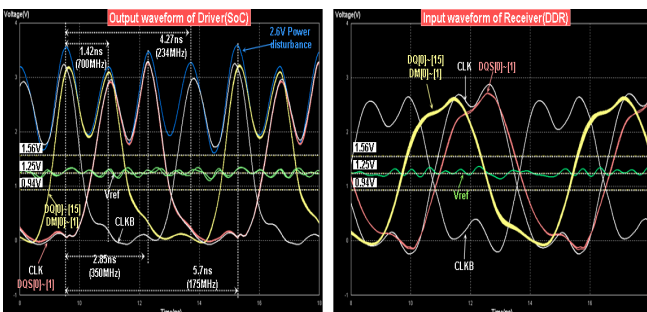


Fig. 7 The simulated result of the worst case SSO

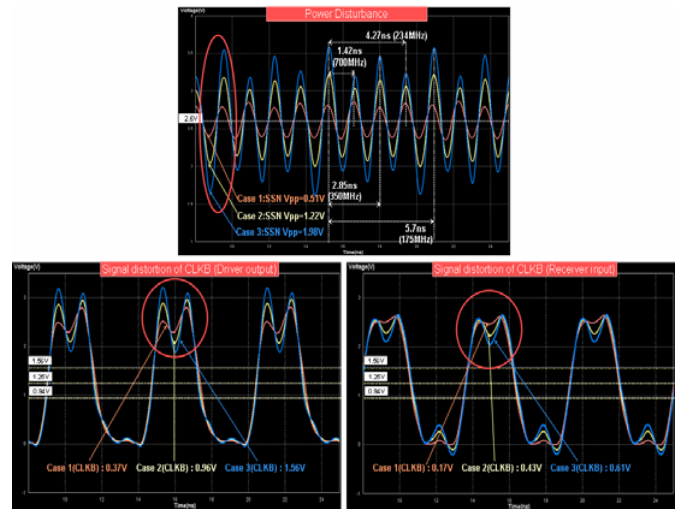


Fig. 8 The SSN influence of SI according to SSO condition

1) *Analysis of power ring via effect.* : Fig. 9 and Fig. 10 show the impedance of power path in frequency domain and power disturbance in time domain according to the number of power ring vias. In frequency domain analysis, the impedance of power path is reduced and resonance frequency is getting shifted to higher frequency by the increase of the number of power ring vias. In time domain analysis, power disturbance of power path is reduced by the increase of the number of power ring vias. Therefore, the DTV SoC system uses 12 power ring vias considering size of power ring.

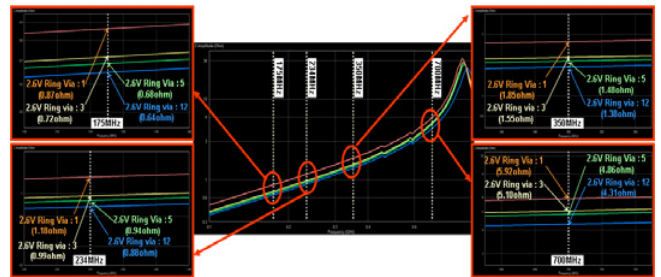


Fig. 9 Power ring via effect in frequency domain

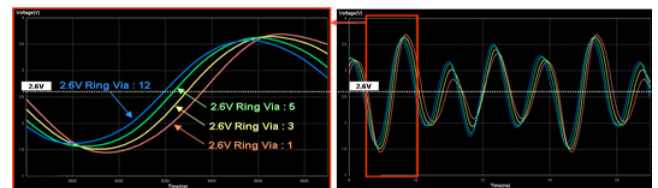


Fig. 10. Power ring via effect in time domain

2) *Analysis of Decap effect in package.* : For additional improvement of SSN, Decaps are added in the package. Fig. 11 and Fig. 12 show the impedance of power path in frequency domain and power disturbance in time domain where the Decaps in the package are used or not. When Decaps are used in the package, the impedance is reduced by about 1/4 times at SSN frequency comparing to the result of not using Decaps in the package. In the same way, when Decaps are used in the package, power disturbance in time domain is also reduced by about 1/4 times.

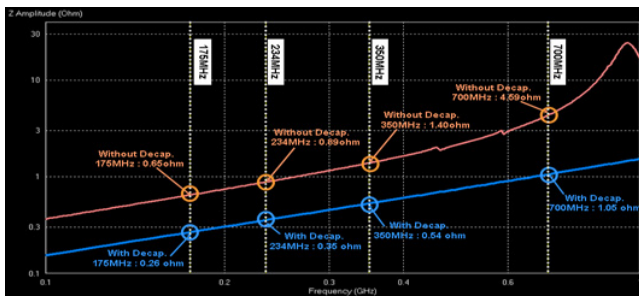


Fig. 11 Package Decap effect in frequency domain

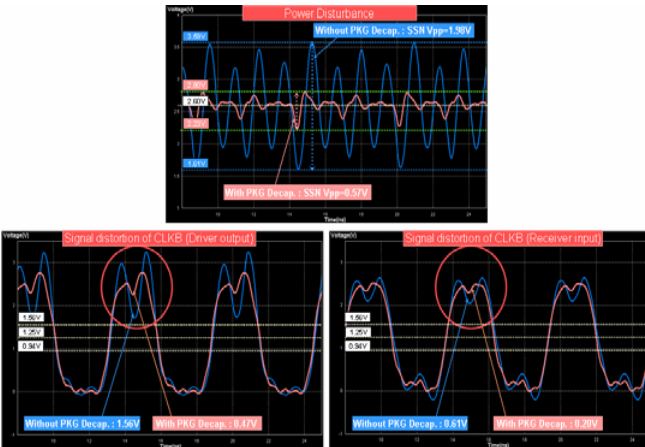


Fig. 12 Package Decap effect in time domain

3) *Correlation of Simulation and measurement* : To increase the accuracy of correlation between simulation and measurement, a probe model and ground position that are used for measurement should be considered, so that we used the circuit model of Tektronix 7260 probe at the same point in measurement. Moreover, the 2.5nf die capacitance of the DTV SoC is considered. Fig. 13 shows the simulation and measurement results of power disturbance that are induced from SSN of the worst SSO condition. It shows a good correlation between simulation and measurement. And, Fig.14 shows the correlation between simulation and measurement results of CLK and DQ signals in the worst SSO condition. It also has a good correlation between simulation and measurement.

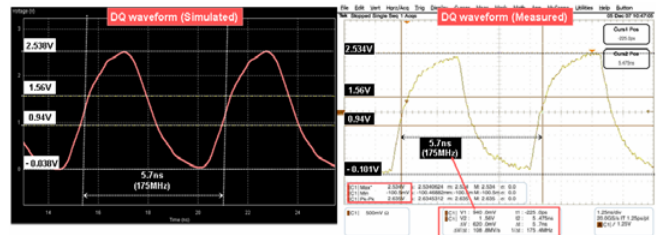
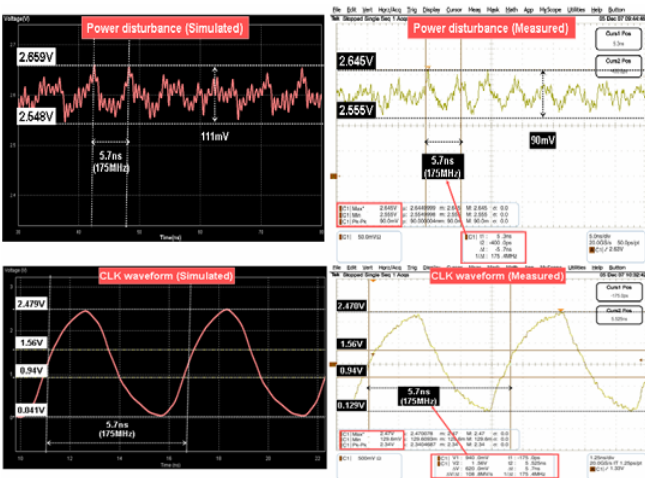


Fig. 13 Correlation of simulation and measurement

III. CONCLUSIONS

SI and PI analysis are very important to fill the gap between the high performance and the low cost of the DTV system. In this paper, an integrated signal integrity analysis method which comprises the interaction among power networks, signal operations, and circuit structures of the full system is introduced.

To increase the accuracy of SI analysis, a full path of signal and power must be analysed by considering SSO condition of the all systems including SoCs, packages, and boards. To reduce SSO effect, the critical factors such as the number of power pads, the full power path impedance at SSN frequency, and decaps in the package should be analyzed using integrated SI analysis method including SSO conditions. To increase the accuracy of correlation, the probe model and ground position should be also considered.

The experimental results show that the correlation between the measurement and simulation results is excellent and the proposed approach can be an effective leverage to determine the performance of the system before manufacturing.

REFERENCES

- [1] M Swaminathan, J. Kim, I. Novak, J. P. Libous, "Power distribution networks for system-on-package : state and challenges", *IEEE Transactions on Advanced Packaging*, vol. 27, May 2004, pp. 286-300.
- [2] E. Sicard, S. Ben Dhia, M Ramdani, T. Hubing, "EMC of Integrated Circuits : A Historical Review", *IEEE Electromagnetic Compatibility, EMC 2007 IEEE international Symposium*, July 2007, pp. 1-4.
- [3] L.D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology", *IEEE Transactions on Advanced Packaging*, vol. 22, No. 3, Aug. 1999, pp. 284-291.
- [4] T. Hubing, "Effective strategies for choosing and locating printed circuit board decoupling capacitors," *IEEE Electromagnetic Compatibility, EMC 2005 IEEE International Symposium*, vol. 2, Aug. 2005, pp. 632-637.
- [5] Howard W. Johnson, Martin Graham, *High-speed Digital Design : A Handbook of Black Magic*, Prentice Hall, 1993
- [6] R. Senthinathan, J. L. Prince, "Simultaneous switching ground noise calculation for packaged CMOS devices", *IEEE Journal of Solid-State Circuits*, vol. 26, no. 11, Nov. 1991, pp. 1724-1728.
- [7] A. Kabbani, A. J Al-Khalili, "Estimation of ground bounce effects on CMOS circuits", *IEEE Transactions on Components and Packaging Technology*, vol. 22, no. 2, Jun. 1999, pp. 316-325.
- [8] B. Young, *Digital Signal Integrity : Modeling and Simulation with Interconnects and Packages*, Prentice Hall, 2001
- [9] Zeeff T. M, Hubing T. H, Van Doren T. P, "Traces in proximity to gaps in return planes", *IEEE Electromagnetic Compatibility, Transactions*, vol. 47, Issues 2, May 2005, pp. 388-392.
- [10] ANSI-EIA-656-A IBIS website.[Online]. Available : <http://www.eigroup.org/IBIS>