



# Addressing 3D Packaging Challenges

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# 3D Package Design and Analysis Challenges

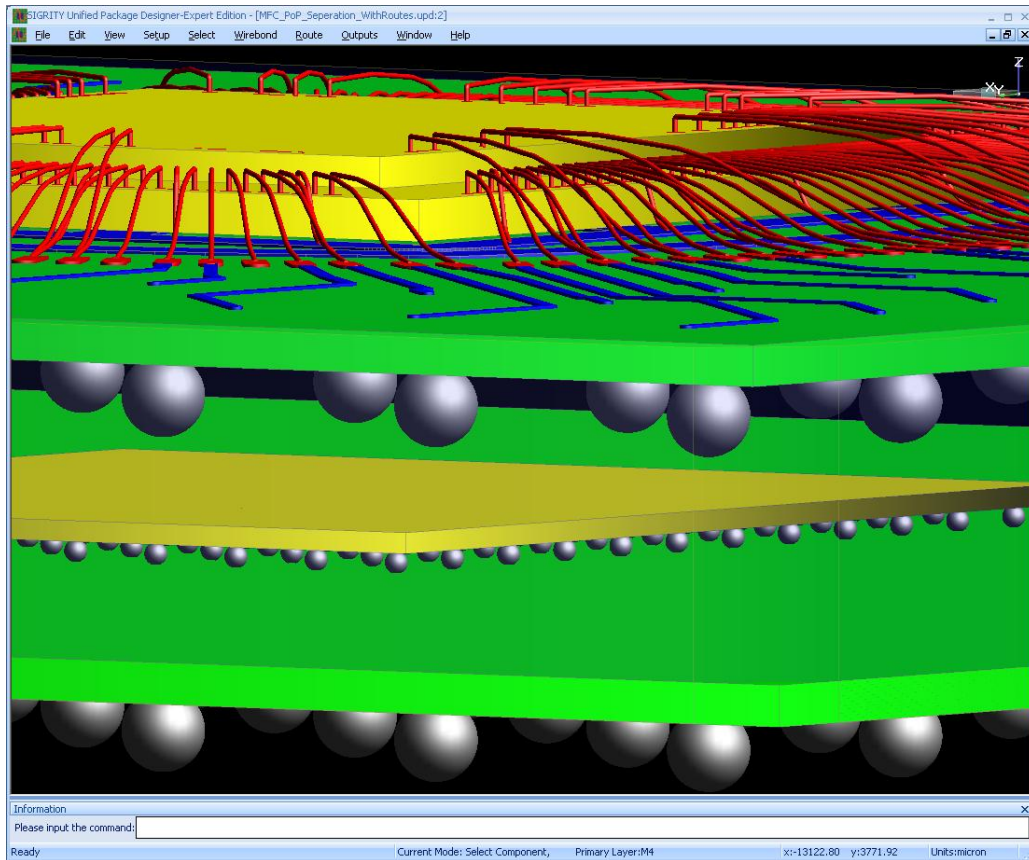
## Overview

The use of 3D semiconductor packages is on the rise. Increasing use of vertical package implementation is driven by the need for additional product configurability and density without adding weight. Every day we use products such as flash drives, mobile handsets and personal entertainment devices that benefit from the technologies. Those who rely on such implantable medical devices as insulin pumps or defibrillators, these 3D packages even play a critical role in improving their quality of life. Popular 3D package implementation approaches include stacked-die, Package-on-Package (PoP), and Thru-Silicon-Via (TSV). Each of these package styles offers valuable benefits which are achieved with targeted design planning, analysis, and implementation strategies.

According to TechSearch International, the use of PoP packages is anticipated to sustain a 40% CAGR through 2012 making it the fastest-growing packaging format. The ability to test at the package level and ease of multi-sourcing make PoP a popular choice with OEMs. Successful PoP implementation requires detailed coordination and design planning. A typical PoP includes a large digital device in the base package and some form of memory in the top package. It's likely the memory is a standard catalog device with fixed pin assignments which limits layout flexibility. For this reason, one important design aspect is coordinating the pad interface between the top and bottom packages. This becomes a significant design challenge because typically each memory source will have different pin assignments.

## PoP Multi-Substrate Planning

Efficient PoP design requires effective planning when options to effect change are greatest. PoP planning should take place prior to, or concurrent with, chip floorplanning because of the direct relationship between the IO pad ring layout and package-to-package interface pads. Ideally, the package-to-package interface becomes the starting point for design planning; the memory devices dictate pad placement, and the IO pad ring placement is modified, as necessary. The die attach method also figures into planning as the configuration of bond fingers for wirebond, and the bump pattern for flip-chip behave as intermediate connection points between the package interface pads and the IO pad ring. Other planning considerations include the routeability of the bottom package, net name differences, and even the host printed circuit board (PCB). The objective is an IO pad ring layout that meets the connectivity needs of the core logic and results in the most cost-efficient package layout possible (i.e., smallest possible number of layers and vias, plus the shortest practical trace lengths).



*PoP with flip-chip and stacked-die*

Coordinated design planning across the chip, multiple packages and, in some cases, the PCB, can be challenging and frustrating — especially with traditional methodologies developed for sequential design flows that use separate tools and databases for packages and chips. Therefore, design teams often collaborate using spreadsheets to communicate pad assignments. The short-coming of this approach is that it's based on snap-shots of static data, resulting in a highly iterative, error-prone process that does little to reduce cycle-time or implementation costs.

Sigrity's OrbitIO Planner, takes a revolutionary approach to concurrent design planning and feasibility by bringing all data sources together into a common, unified planning environment. Functionality for wirebond and route feasibility provides a way to evaluate design aspects traditionally associated with detailed implementation while the design is still in the planning stage. This approach facilitates pad placement. Connectivity scenarios are derived and evaluated in the context of the entire system. OrbitIO Planner's unified chip-package-board data model automatically propagates changes to adjacent domains, providing instantaneous feedback on their system-wide impact.

Efficient PoP development is enabled by tuning the design for performance, cost and manufacturability. Often, tuning the IO pad ring and package-to-package connectivity provide the critical difference in obtaining high quality design results rapidly.

## Modeling and Simulation

Having access to extraction results early in the design flow allows designers know the effects of topology and implementation choices on system-level behavior. Knowing the signal loads, delays, reflections and couplings, IO designers are able to implement more robust on-chip-drivers. Similarly, having early access to package power plane and on-chip power grid electrical models enables designers to trade-off decoupling capacitor placement between package and chip to identify the implementation with the best performance at the lowest possible cost.

Early feasibility studies provide designers with rough estimates of signal net parasitics by using predicted wirebond and trace lengths. Extraction of power delivery system parasitics, however, requires a physical implementation of some form, even if approximate. Discontinuous return paths, power plane resonances and decoupling strategies are dependent on physical implementation. Therefore, considering whether or not to split power delivery planes and their associated interaction with signal integrity is a choice well supported by whole package extraction. This choice must be made early in the package design flow. It is difficult to change late in the flow, even if extraction is applied only for final verification or to provide colleagues or customers with electrical models of the final design.

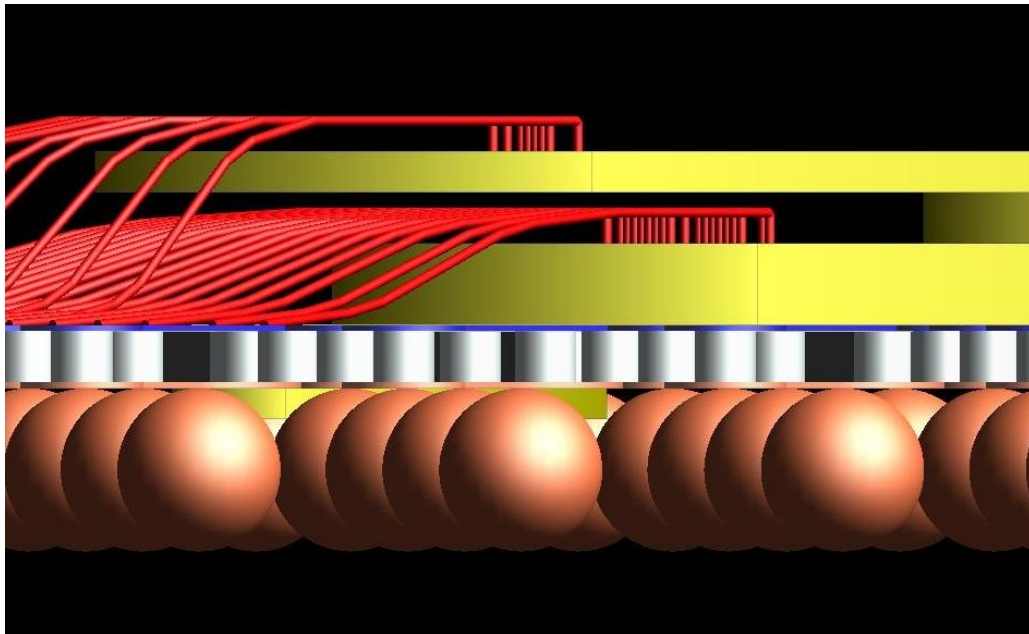
Thru-Silicon-Via (TSV) packaging is a vertical format promising greater integration densities and support for high-bandwidth memory to logic interfaces. Some consider it a means to continue chip scaling when semiconductor processes alone no longer can do so. In TSV, bare die are stacked and directly connected to one another using thru-vias in the silicon, as opposed to wirebonding or bumping. Although processing methods are evolving – some use a vias-first approach, while others use a vias-last approach – a high degree of concurrent design planning is required to coordinate via locations between substrates while considering local on-chip interconnects. There remain gaps in planning and implementation tools for TSV which may slow adoption.

Stacked-die packages exploits the Z-dimension by integrating several die in a stacked configuration within a single package. The high degree of silicon integration in this format greatly reduces the required PCB area, compared to conventionally packaged devices. The close proximity of die makes it ideal for localizing high-speed, high-bandwidth connections, reducing PCB implementation challenges. Compared to PoP, stacked-die packages can provide greater functional density in less weight and mass, but reliability and testing requirements require even more thorough consideration.

Design planning for stacked-die is a critical step in the development process, greatly influencing complexity and cost of the finished package. Wirebonding and die-stack order must be taken into account during planning because bond tier configuration and bond wire length are major cost contributors. The multi-chip aspect of these packages adds the dynamic of die-to-die connectivity, in addition to die-to-package. In many cases, the fixed IO assignments of one die are used to influence the IO pad ring layout of adjacent die. This is a significant challenge, given assembly and design variables, and the multiple datasets involved. The location of power and ground die pads is one example of how wirebonding influences pad ring layout. Dedicated power and ground rings on the package substrate typically are closest to the die edge. Placing the power and ground pads on the outermost row of die pads results in the most direct connections and shortest wire length, with minimal interference to signal wires. The concurrent design planning tools discussed earlier can facilitate this type of multi-die planning and take into account these implementation requirements.

Although it's common to have a mix of flip-chip and wirebond devices within the same package, stacked-die designs usually are dominated by the wirebond interconnect. Typical designs have 2-3 die, but some have a stack with 5-7 die. As the number of die increase, so do the number of wirebond tiers and complex wire-to-wire interactions. One of the first tasks is to determine the actual sequence of the die within the stack, in a way that minimizes wirebond complexity.

On some designs, defining die stack order is as simple as starting with the largest die on the bottom and working upwards, pyramid-style, to the smallest die. In other cases, a larger die may be placed above a smaller one in an overhanging or cantilevered fashion, necessitating a spacer between the die to create adequate space for bonding. Due to the tight quarters, a low-profile wirebond model is used. Other variables to consider during die stack definition are die thickness, cavity depth, and assembly variants. Knowing the assembly and wirebond process is helpful because die stack definition is an exercise in balancing assembly, performance, and design requirements.



*Cantilevered die-stack with low-loop wirebond model*

With the die stack defined, the next challenge is to create wirebond connections from die-to-die and die-to-package while minimizing complexity and wire length, using physical implementation tools. These tools provide a high degree of wirebond automation and extensive editing functions for detailed refinement. Such functionality must be supported by a comprehensive set of design and assembly rules continuously monitored throughout the design process.

Extraction tools must accurately model complex-shaped wirebonds and the proximity coupling among them – significant for parallel and nearly-parallel wirebonds. This coupling can exist within a single package-to-chip wirebond group, or across multiple domain boundaries. For example, package-to-chip-1 wirebonds could couple significantly to package-to-chip-2 wirebonds.

## 3D Designs in a 2D World

Unlike some tools that are used for package design and analysis, Sigrity's Unified Package Designer (UPD) was designed with an understanding of 3D structures (ex. wirebonds). This understanding of the Z-dimension is critical to support design and analysis of 3D packages and is very difficult to achieve with systems that have been modified from conventional 2D layout tools with 3D rendering and DRC tacked on.

The time required for defining the die stack-up and associated wirebonding tiers can be shortened by using new windowing mechanisms. These provide dynamic profile views from any side of the package that are much more intuitive than conventional top-down views. User-definable or manufacturer-specific wire shape models enable a more accurate representation of the assembled device than is possible using traditional JEDEC wirebond models.

Improved design representation combined with 3D DRC opens the door to greater manufacturing insight during the design stage. For example, designers could gain the ability to simulate worst-case placement scenarios – considering placement and rotational tolerances for all die, while still at a point where wirebond changes could easily be made. Other possibilities include defining the wire insertion sequence and being able to simulate it while taking into account capillary tooling clearance. In the future, manufacturing awareness will not be limited by design tool functionality, but by organizations unwilling to change behavior and processes.

Volumetric packaging such as stacked-die and PoP will continue to deliver the functional density, weight, and configurability needed to keep pace with Moore's Law for the foreseeable future. On the horizon, TSV packages promise even greater density and performance; however, lack of EDA tools is a limiting factor to their widespread adoption.

The multi-substrate, multi-domain nature of 3D packaging bring are leading design teams away from sequential design flows with the limitations associated with database variability. Sigrity's design planning, implementation, and analytical tools support critical decision making on issues that impact performance, complexity, and cost at a point in the design process when it's most economical to effect change.