DesignCon 2007

Study of Simultaneous Switching Noise Reduction for Microprocessor Packages by Application of High-K MIM Decoupling Capacitors

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Abstract

This paper describes the effect of using an on-die metal High-K metal-insulator decoupling capacitor (on-die High-K MIM DECAP) in reducing simultaneous switching noise (SSN) for microprocessor packages. The SSN reduction for microprocessor packages due to on-die High-K MIM DECAP added to the IO-power delivery network (IO-PDN) is described using data eye-diagram as a key figure of merits. The power integrity performance of the microprocessor packages, which in turn directly effects the signal integrity is discussed in terms of the resonant free target input impedance and the power-ground noise voltage due to IO switching current of large magnitude through the effective loop inductance of the IO-PDN.

For the purpose of accurate analysis and to provide design guidelines a distributed circuit model of the on-die High-K MIM DECAP, which is developed based on its physical implementation, is described in the paper. Using this distributed model, SSN modeling and simulation results for signal integrity performance of the microprocessor package with DDR interfaces is discussed throughout this paper.

Author(s) Biography

Om P. Mandhana is a Senior R&D Engineer in the Networking and Computing Systems Group (NCSG) of Freescale Semiconductor, Austin, Texas, since 1998. His current responsibilities include developing methodology and strategy for chip, package, board, and interconnect co-design modeling and simulations capability to address power integrity and signal integrity issues related to NCSG products. Before joining Freescale, he has worked as an Advisory Engineer for seven years in the high performance workstations group at IBM, Austin, TX. He was involved in teaching electrical engineering courses as an Adjunct faculty at The University of Texas, Austin, as an Assistant Professor at University of Kentucky, Lexington, as a lecturer at University of Missouri, Columbia, and as a lecturer at Birla Institute of Technology and Science, Pilani (India). His research interest includes modeling, simulations, and design of advanced microprocessor packages and interconnects including dc-dc converters for high-speed digital systems. He has authored several journal and conference papers in the field of power integrity, signal integrity and power electronics. He received the Ph. D. degree in electrical engineering from University of Missouri, Columbia.
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Héctor Sánchez is the Chief Engineer in charge of the Advanced Circuits Design Center (AC/DC) of the Networking and Computing Systems Group of Freescale Semiconductor. Over the last 16 years he has worked as a custom circuit designer with Motorola's Semiconductor Products Sector in Austin, Texas working on the development of PowerPC microprocessors. He received a BS and ME degrees in electrical engineering from Texas A&M University in 1987 and 1990, respectively. His professional activities include: phase-locked loop circuit design, clock generation, clock distribution, high-speed analog-digital circuits, design for low-power, microprocessor thermal management, temperature sensor circuit design, I/O buffer design, microprocessor chip integration, and technology definition (advanced transistor and metallization including FinFET, 3D circuits) for sub-90nm technologies. He has authored more than 18 papers and has 13 patents granted and several pending. He is a member of the Digital sub-committee at the IEEE ISSCC (2001-2006) and a member of the IEEE International SOI Conference Committee (2002-2006), and of the IEEE International Interconnect Technology Conference (2005, 2006). He is a member of IEEE

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Jonathan Burnett is a Senior Signal Integrity Engineer with the Networking and Computing Systems Group (NCSG) of Freescale Semiconductor. His currents activities include system-level signal integrity analysis for reference and testcard designs at Freescale Semiconductor. He is also involved in IO buffer modeling support, largely through the use of IBIS. He has worked in the field of high speed printed circuit board design for 15 years. His educational background is a BSEE from Rice University in Houston, Texas.

1. Introduction

With increasing interface data rate of high-speed digital systems, reducing the IO noise, such as simultaneous switching noise (SSN) due to several IO drivers switching simultaneously and improving overall signal integrity performance of microprocessor packages is a critical design concern.

The primary adverse electrical effect of microprocessor packages on the signal quality is the noise induced due to package parasitics. The signal transmission paths on the signal layers inside the package share the coupled IO-PDN environment, thus the power delivery network (PDN) noise is directly coupled into signals transmitted inside the package. The noise induced due to package parasitics limits the total number of signals that can switch simultaneously. Therefore, two main physical mechanisms generating undesired SSN are the delta-I noise in the PDN and the inductive coupling among signal to power, signal to ground and signal to signal traces connected with switching IOs. In general, the inductive coupling between signal traces and PDN produces poor power integrity and signal integrity issues which results in the poor performance of high speed CMOS devices. The poor signal integrity problems in a package mounted with chip/die can arise either at the chip level or at the package level. At the chip level signal integrity issues may be due to improper IO buffer design, whereas at the package level these issues can arise due to high IO-PDN inductance, mismatched traces, improper routing, inadequate return path etc.

Simultaneous switching of several IO drivers draws a fast changing current through the IO-PDN. The voltage droops and fluctuations at the power to ground terminals are generated as a result of the transient currents through IO-PDN planes. These voltage droops and fluctuations, also described as delta-I noise, across the power and ground terminals of the IOs weaken the signal driving capability of IO drivers which causes signal integrity problems. In particular, the power-ground planes of the package IO-PDN behave as a cavity resonator at high frequencies due to which the impedance profile of the IO-PDN may contain several resonant peaks. SSN, therefore, is a function of the switching currents of faster edge rates through the power/ground planes of the IO-PDN of the microprocessor package. The SSN problem due to package parasitics can be reduced significantly by designing the resonant free IO-PDN of impedance magnitude as close as possible to target impedance over a wide frequency range.

Looking from the package point of view, designing the packages with reduced effective loop inductance of PDNs can control the corresponding PDN impedances. One commonly used solution to reduce the effective loop inductance of the PDN is to increase the number of power and ground pins in the power delivery current path. However, with increasing number of required IO-pins this solution is cost-prohibitive. Therefore, the packaging technology can only provide partial relief in reducing the PDN impedance over a wide frequency range. Traditionally, the resonant free IO-PDN of low impedance magnitude is realized by using a combination of on-die IO capacitance of small value and several package mounted discrete decoupling capacitors (PKG-DECAPS). These decoupling capacitors act as sink/source of extra charge for IO drivers. This helps to reduce the voltage droops and fluctuations at the power-ground terminals of IO-drivers until the primary power source of the system responds. The performance of these discrete DECAPS on the microprocessor packages is limited by the associated ESR and ESL of the capacitors. Alternatively, on-die High-K MIM DECAP in addition to the existing package and board level capacitors, are used by designers for more effective reduction of PDN impedance magnitude over a wide frequency range, and to eliminate chip supply voltage transients [1].

The main emphasis of this paper is to describe modeling and simulation methodology illustrating the impact of on-die High-K MIM DECAP on reducing the SSN of the microprocessor packages due to simultaneous switching of several DDR-IOs. In this paper we propose, and present results of, the implementation of massively pervasive On-Die High-K MIM DECAP for improved performance of the IOs of the CMOS devices. The technology information and physical implementation of the on-die High-K

MIM DECAP are also described. Simulation results and parametric curves for voltage droop at the power-gnd terminals of the IO drivers are obtained as a function of the on-die High-K MIM DECAP, including the different parameters of its distributed model. These simulation results illustrate that the on-die High-K MIM DECAP, as function of different parameters of the distributed model, is effective in improving the power integrity and in reducing the SSN noise due to package parasitics. These simulation results can be used for design guideline specifications and also for the package performance improvement.

2. On-Die High-K MIM DECAP

It has been shown that MIM capacitors help the maximum frequency of microprocessors improve by close to 10% [2]. However, application of large amounts of decoupling capacitance may be needed in a larger relative scale for IO interfaces. The large amount of instantaneous current demand on the PDN due to simultaneous switching of several IOs dictates the critical need to improved power integrity of the system. The power integrity problem is due to large transient voltage droop caused by the fast changing current through the effective loop inductance of the PDN. Note that the signal edge rate for typical 1.8 V DDR-IOs with 18 Ω impedance is in the nano-second range. This yields 0.1 A of peak current per IO switching per nano-second. For 64 IOs switching simultaneously, this represents a total peak current drawn from the power source equal to 6.4 A/ns per interface. If it is assumed that IOs must rely on their internal capacitance to supply this charge at high frequencies, then the decoupling capacitance needed to keep the power supply within 10% of the nominal value would require upwards of capacitance, $C = I*dT/dV = 6.4A*1ns/0.18V = 35.56$ nF.

In order to effectively reduce the high frequency noise on the IO-PDN, the white space on the chip in practice is filled with decoupling capacitors realized by gate-oxide capacitance of the transistors. However, with the advancement in technology, on-die High-K MIM DECAP is considered as an alternative to on-die gate decoupling capacitor. Due to dielectric leakage of the thin gate oxide, the on-die High-K MIM DECAP is more effective as compared to gate-oxide capacitance in realizing the resonant free low input impedance for IO-PDN over a wide frequency range. Additionally there is no chip area penalty associated with the inclusion of MIM capacitance as compared to a substantial penalty for gate oxide capacitors.

The MIM capacitor used to decouple the internal power supply is shown in Figure 1. The 8fF/μm^2 planar MIM capacitors of the 90nm SOI technology are formed by physical vapor deposition of alternating layers of HfO_2 and Ta_2O_5 dielectrics between TaN electrodes [3]. It is physically located below the thick last metal used for clock, power routing, and IO signals. Holes are created on the capacitor plates to provide access to signals that need to get from the last metal to the lower level metals. Furthermore, vias are used from last metal down to the top and bottom plates to contact these. The density of the MIM plate contacts defines the series resistance for RC coupling to the power grid, and is key to optimizing capacitor utilization and performance.

The physical implementation of the MIM capacitor can be realized in different ways to provide flexibility of integration. However, the flexibility afforded by the approach may also have an impact on the resulting electrical performance.

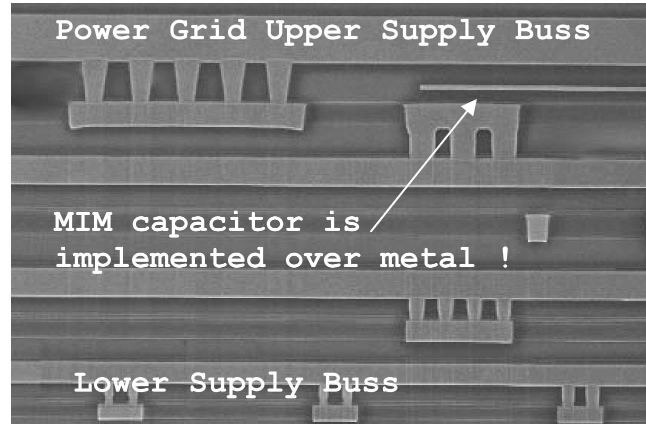


Figure 1. Cross-section of metallization stack for upper 8 metal levels showing integration of MIM into copper/low-K backend.

In its most flexible implementation, IOs are placed on a die without regard to the MIM implementation specifics. Next, a MIM mask is created as a post-processing step to alter the original database. The advantage of this method is that the inclusion of MIM is "non-intrusive" as it only modifies the mask to provide feed-through paths from the lower metal levels to the uppermost metal level**.** Another key advantage is that MIM decoupling capacitor can cover ANY area of the chip, and as such it can exceed the physical boundary of the IOs and extend over non-IO areas of the die. This provides the flexibility to add very significant amounts of on-die DECAP (> 20nF) for IOs that would be prohibitive with standard gate-oxide capacitors.

Circuit representation of On-die High-K MIM DECAP

A circuit representation of the on-die High-K MIM DECAP and associated IOs, based on its physical implementation is shown in Figure 2. Notice that the on-die High-K MIM DECAP module connects to the IOs at an effective pitch dictated by the OVDDIO and GND C4's. The electrical parameters of interest are the MIM capacitance (C_{mim}), the MIM plate resistance and via resistance (R_{mim}), the metal resistance (R_{metal}), the connecting metals resistance from IOs to C4's and the resistance of C4's (R_{c4}). The MIM capacitance value is the aggregate total capacitance obtained by Capacitance_per_unit_Area ($fF_{mim}/\mu m^2$)* Area (μm^2). The MIM plate resistance is in the order of 50 ohms/square. This high MIM plate resistance forces either a large amount of metal utilization to contact the on-die High-K MIM DECAP or a degraded frequency response. The metal resistance, R_{metal} is the contribution of the metal connection from the IO bank to the on-die High-K MIM DECAP. The metal resistance from the IO bank to the power/ground C4's and the associated power/ground resistances of C4's are modeled as part of the R_{c4} component. Note that careful management of these metal parasitics is critical to the performance of the on-die High-K MIM DECAP.

The physical implementation described above is improved by connecting IOs to the on-die High-K MIM DECAP at an improved effective pitch, as shown in Figure 3. The metal connection from the IOs to the on-die High-K MIM DECAP occurs at every IO by the inclusion of extra last metal lines that connect each IO power terminal to the on-die High-K MIM DECAP, which extends beyond the IO boundary. This results in improved effective R_{metal} and R_{mim}.

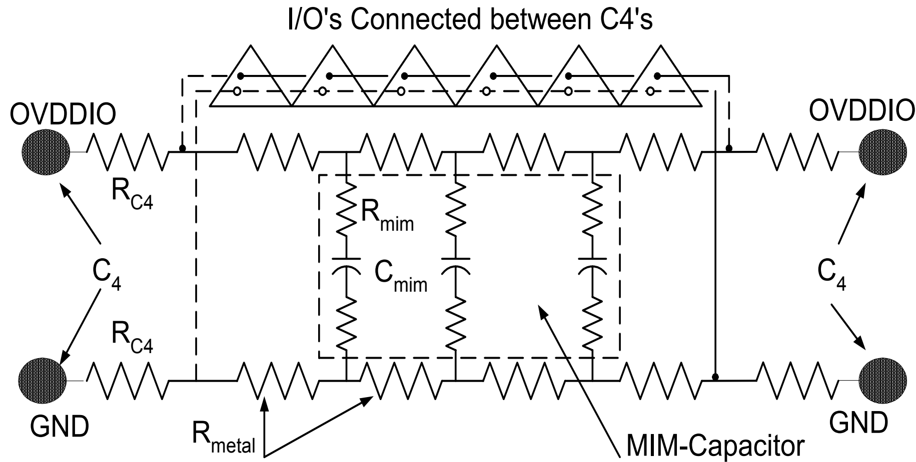


Figure 2. Circuit representation of on-die High-K MIM DECAP based on the physical implementation

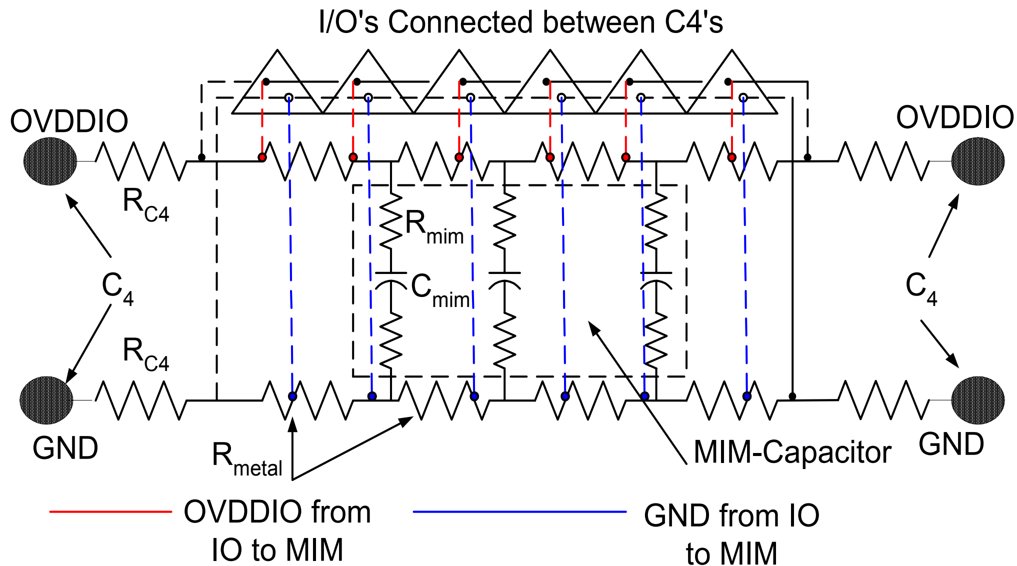


Figure 3. Circuit representation of on-die High-K MIM DECAP based on the improved physical implementation

The most robust implementation for the on-die High-K MIM DECAP with desired frequency response is shown in Figure 4. This optimal physical implementation is attained by reducing the via-MIM spacing between the OVDDIO and GND plates. As shown in Figure 4 (a), this is accomplished by custom integration of the on-die High-K MIM DECAP into the IO itself. Since most of the effective resistances are below 0.1 ohms, the resultant electrical performance of these DECAPS approaches to that of an ideal capacitor, as shown in Figure 4 (b). Therefore, in the physical implementation as shown in Figure 4 (c), almost an ideal DECAP is realized between the power and ground of each of the IO's connected between C4's. It is important to note that by proper custom design, the IO designers are in control of the electrical performance of the IOs. This is in contrast to the other two approaches where the High-K MIM DECAP performance is chip-specific.

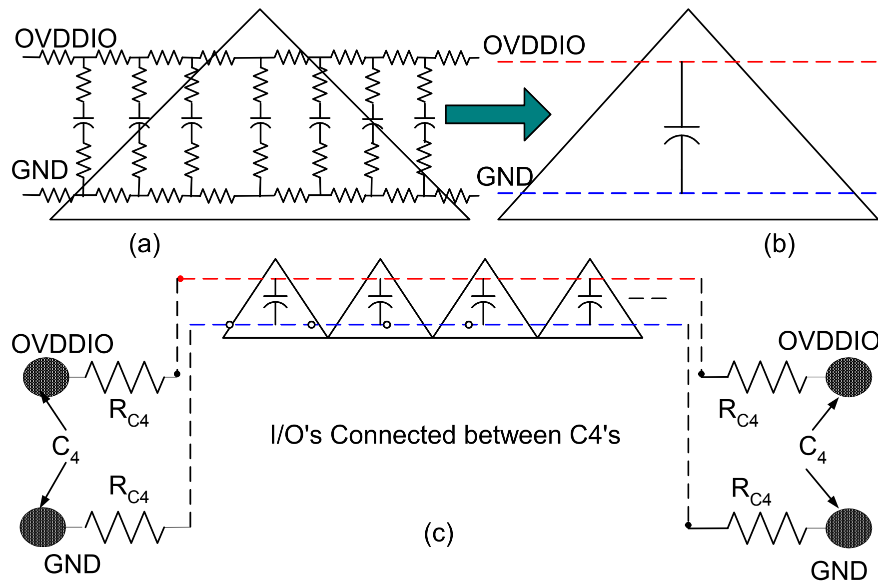


Figure 4. Robust Circuit representation of on-die High-K MIM DECAP

Next, in order to create a distributed circuit model, the on-die High-K MIM DECAP module shown in Figure 2 is subdivided into small subsections with both power and ground connectivity. A given subsection is modeled as a distributed resistive-capacitive network as shown in Figure 5 (a). Note that vias from the metals to the plates have significant resistances which must be modeled carefully. Also, the vias connected to the plates and the center of the overlapping area for a given subsection has undesirable parasitic resistance. As stated earlier, a sheet resistance of 50 Ohms/sq is quite high and may degrade the performance of the on-die High-K MIM DECAP. Therefore it is critical to minimize the parasitic resistance. In order to make these DECAPs available to all the IO circuits, appropriate strapping is created on the upper metal layer of the die. Based on these factors a distributed circuit model of the on-die High-K MIM DECAP per IO is generated as shown in Figure 5 (b).

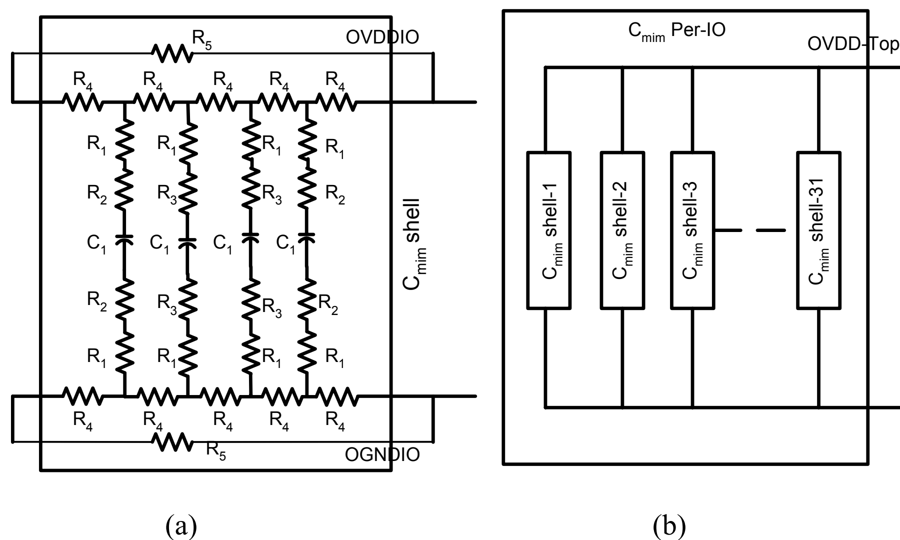


Figure 5. Distributed Circuit representation of High-K MIM DECAP based on Physical implementation

Eye Diagram

The eye diagram provides significant information about the quality of a switching IO-signal, when several IO drivers are switching simultaneously. For example, the eye opening provides information regarding noise margin. A large clear eye signifies high quality signal with very less noise, whereas a smaller or closed eye represents a low quality noisy signal. The signal distortion can be analyzed by observing the thickness of the signal lines at the top and bottom of the eye. The width of the signals due to variations of the zero crossings in time implies the jitter in the output signal. Similarly, the measure of the transition time between the top and bottom of the eye represents the rise and fall times of the output signal.

3. Modeling and Simulation Methodology Overview

This paper presents an efficient modeling and simulation methodology to study the effectiveness of on-die High-K MIM DECAP in improving the SSN performance of a real flip-chip ball-grid array (FCBGA) package. The 3D cross-sectional view of a multilayer (12 layer) FCBGA package used for this study is shown in Figure 6**.** The top layer of the package has pre-defined locations for discrete package DECAPS around the die to reduce the power-ground noise voltage on the PDNs, mostly in the lower mid-frequency range. The time domain and frequency domain modeling and simulation methodology is described in this paper using a commercially available full wave electromagnetic field solver –SPEED2000 and PowerSI [4], with built-in circuit solver. The FCBGA package, including all the power/gnd planes, vias, and signal layer, is modeled and simulated using this 3D full-wave electromagnetic field solver.

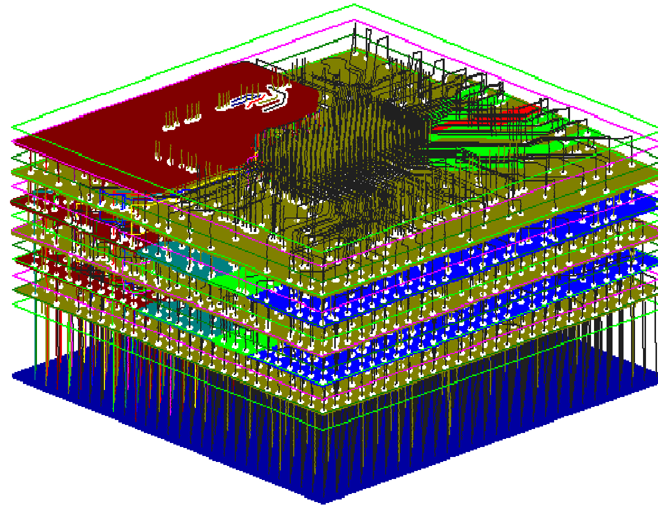


Figure 6. Cross-section of a FCBGA package

Figure 7 shows the block diagram representation of the model used for time domain and frequency domain simulation and analysis to study the effect of on-die High-K MIM DECAP in reducing SSN due to DDR IO drivers. It is important to note that in Figure 7 both PDN and IO signal nets are considered in order to account for all the inductive and capacitive coupling and different components in the electromagnetic field simulation of the package.

The package design database with stackup, material properties and other associated information is converted into the format compatible with the field solver. The stackup dimension and material properties information related to the package can be updated using the menu-driven commands of the generator

module of this field solver [5]. The power (OVDD/VDD) and ground (OVSS/VSS) nodes on the top (bottom) layer are connected to the power and ground terminals of the IBIS model of the DDR IO-drivers (dc power source). Therefore, the PDN connection of the IOs is composed of power and ground chip connection, power and ground vias, power and ground planes and pins in the package substrate dedicated for power and grounds. All the power pins are lumped together, as are the ground pins. A DDR2 full strength IO buffer model with nominal output impedance of 18 Ω is used for driving the device from the DDR2 controller to the memories. The IO buffer was modeled using IBIS 3.2 keywords. The system load connector used modeling and simulation purpose is a DDR2 data load with two DIMM slots and a dual rank DIMM in each slot. The DIMM load for each slot was a JEDEC compliant DDR2 data load. The memory devices were modeled to include on-die terminations of 75 Ω and 150 Ω as applied in industry standard methods. The system load connector circuits, capacitive loads and other circuit element connections can be made using the merge circuit function of the built-in SPICE-based circuit simulator of the field solver.

The design oriented modeling simulation and analysis for improving the SSN performance of the package is discussed for various simulation conditions, such as with lumped/ideal and distributed model of the on-die High-K MIM DECAP connected across IO-PDN of the package. For the purpose of accurate and comparative analysis, different distributed models of the on-die High-K MIM DECAP based on the physical implementations already described in this paper are considered in the simulation.

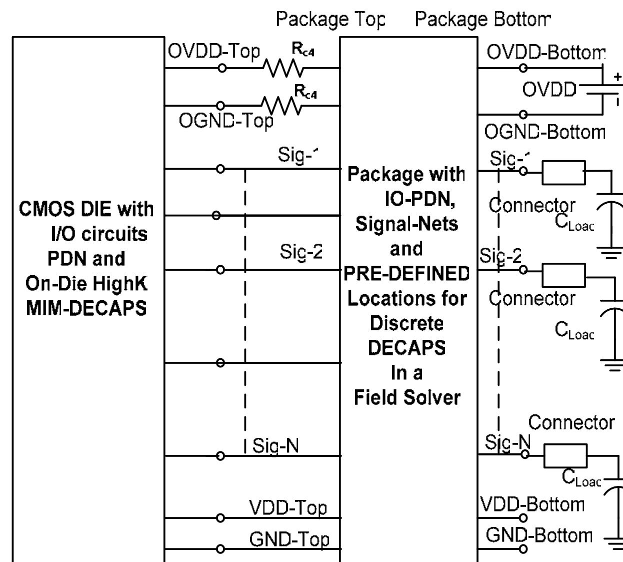


Figure 7. Block diagram model to study effect of On-die HighK MIM-capacitance in reducing SSN

In the first part of the paper, system level modeling and simulation results are described considering the on-die High-K MIM DECAP across the IO-PDN terminals of the package as a lumped capacitance, C_{mim}. The second part of the paper discusses modeling and simulation results, considering a distributed model of the on-die High-K MIM DECAP as shown in Figure 2. Based on the improvement in the actual physical implementation process, the distributed model of on-die High-K MIM DECAP per DDR-IO is considered to discuss the overall power and signal integrity improvement and the resultant SSN performance of the package.

Based on the package level frequency domain modeling and simulations, following design oriented analysis is performed to study the effectiveness of the on-die High-K MIM DECAP,

(i) Determine the self and transfer input impedance of IO-PDN at the die location on the package for different values of on-die High-K MIM DECAP and associated parameters of its distributed circuit model

(ii) Compare these input impedance characteristics for lumped/ideal and distributed circuit models of the on-die High-K MIM DECAP

The package mounted DECAP parameters can be selected by considering the effect of on-die High-K MIM DECAP on the input impedance of the IO-PDN at the die location on the package. The package DECAP parameters are selected by considering the input impedance resonant peaks of IO-PDN at the die location on the package shifted to the low frequency range due to on-die High-K MIM DECAP [1].

Time domain simulations corresponding to different values of on-die High-K MIM DECAP are performed by connecting IBIS models of the DDR-IOs to data signal nets at the top of the package. For each data signal net, a circuit model of the system load connector in series with a capacitor representing a receiver load is connected at the bottom of the package. Based on time domain modeling and simulation, following design oriented analysis is performed to study the effectiveness of the on-die High-K MIM DECAP for SSN performance evaluation of the FCBGA package with 64/144 DDR-IO drivers switching simultaneously,

(i) Determine voltage droop at the die location as a result of the transient currents through IO-PDN planes due to simultaneous switching of several IOs. Different values of the on-die High-K MIM DECAP including its distributed circuit model parameters are considered to study the effectiveness of these DECAPs.

(ii) Determine the critical value of the on-die High-K MIM DECAP for an effective loop inductance value of the IO-PDN, which may increase the power-ground noise voltage for a switching frequency of the IOs.

(iii) Determine data eye-diagram corresponding to a switching voltage signal on the receiver end.

The power to ground voltage droop and height of the central eye opening of eye diagrams are used as figures of merit to provide information about the noise margin and the resultant quality of the transmitted data signal from the IOs to the load. From these simulation results, optimum values of the on-die highK-MIM-DECAP and other parameters of its distributed model are obtained for reduced SSN caused by the several DDR-IOs switching simultaneously. Several other parameters such as signal overshoot, ring back, jitter and signal distortion can be observed and compared for different values of the circuit model of the MIM capacitance models described previously in this paper.

4. Frequency domain and Time Domain Simulations

Part 1

In this section frequency domain and time domain simulation results are described considering the lumped model of the on-die High-K MIM DECAP. The block diagram representation of the model to study effect this DECAP in reducing SSN due to several DDR IOs switching simultaneously shown in Figure 8.

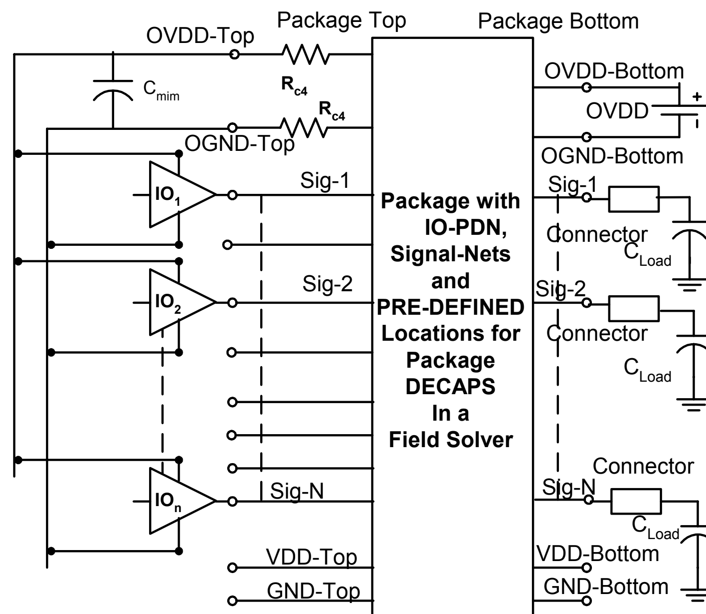


Figure 8. SSN simulation setup considering lumped model of on-die High-K MIM DECAP

Figure 9 shows plots for self and transfer input impedances of the IO-PDN and other PDNs at the die location on the top of the package.

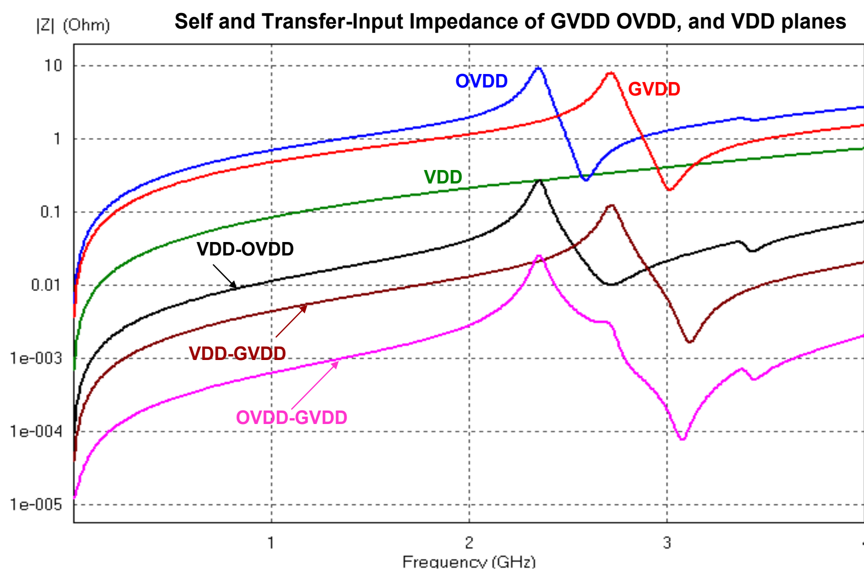


Figure 9. Self and transfer input impedance of PDN

It can be noted from Figure 9 that the input impedance of the PDNs of the package is inductive over a wide frequency range. The effect of on-die High-K MIM DECAP, considered as the lumped capacitance C_{mim}, on the self input impedance of the IO-PDN is illustrated in Figure 10. The value of C_{mim} is considered in the range from no capacitance to 20 nF. The resonant peak of the IO-PDN impedance shifts to the low frequency range with increasing value of on-die High-K MIM DECAP of the IO-PDN. Also, the input impedance magnitude drops steadily in the high frequency range.

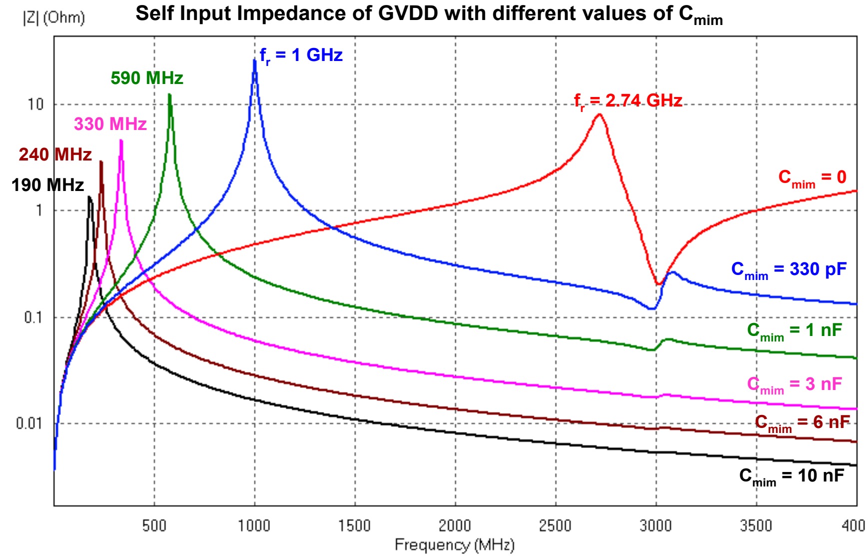


Figure 10. Self input impedance of IO-PDN with different values of MIM capacitance

The impedance peaks are due to the resonant circuit formed by the on-die High-K MIM DECAP and the effective loop inductance of the IO-PDN.

The plots shown in Figure 11 are the transfer input impedances between the IO-PDN and the Core-PDN of the package for different values of on-die High-K MIM DECAP, C_{mim}. Figure 11 illustrates that the transfer impedance at the die-location of the package reduces with increased value of the C_{mim}.

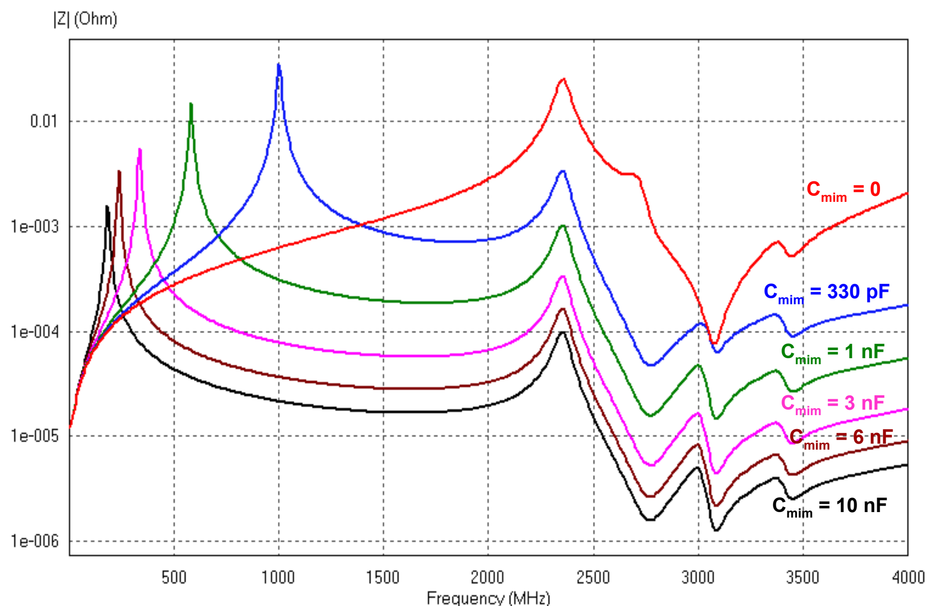


Figure 11. Transfer input impedance IO-PDN to Core-PDN for different values of High-K MIM DECAP

Next, considering different values of C_{mim} across the power bus, Figure 12 shows time domain simulated voltage across power and ground terminals of the 64 DDR-IOs of Figure 8, switching simultaneously at 333 MHz corresponding to 667 MBPS.

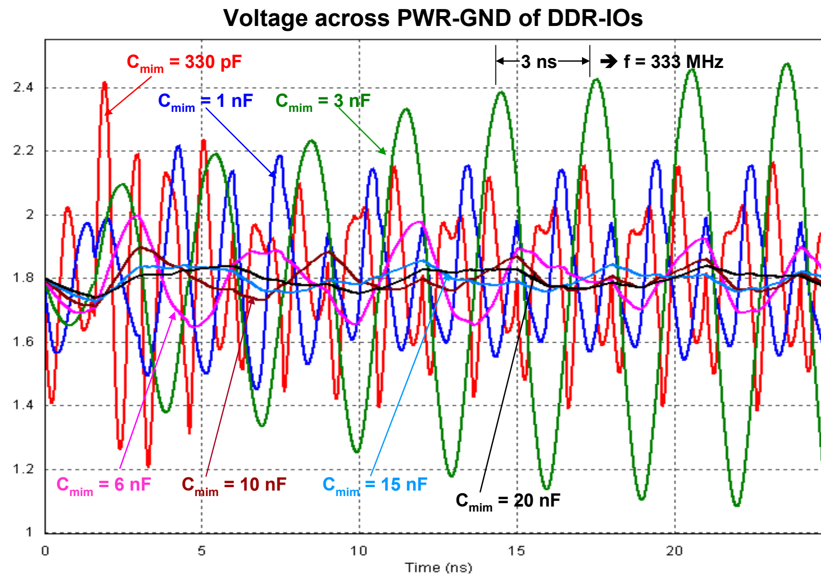


Figure 12. Power-ground noise generated in IO-PDN due to 64 DDR-IOs switching simultaneously

increasing values of C_{mim}. However, C_{mim} = 3 nF in Figure 12 increases the peak to peak noise voltage and it is oscillating at a frequency of 333 MHz. Note that in Figure 10 the resonant peak of the input impedance magnitude of the IO-PDN is shifted from high frequency range to 330 MHz for C_{mim} = 3 nF. Also, the DDR-IOs switching at 333 MHz indicates that the fundamental frequency component of the switching current may be coincident with the impedance resonant peak at 330 MHz. Therefore, the switching current waveforms flowing through the power and ground pins of the package are recorded for different values of C_{mim}. Next, the Fast Fourier Transformations on these currents are performed to obtain the frequency domain spectrum of the switching currents through the power and ground pins.

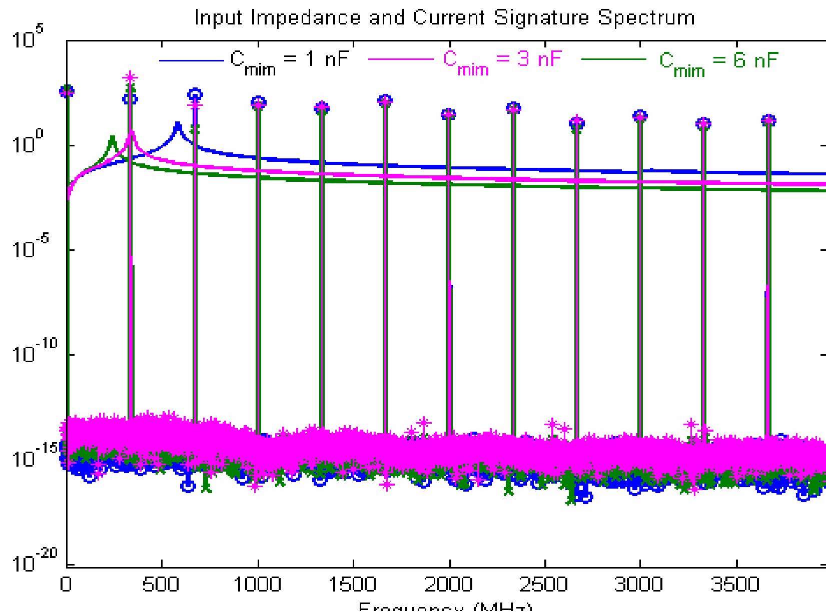


Figure 13. Input impedances and frequency spectrum of switching currents

The frequency spectrum of switching currents through power and ground are plotted as shown in Figure. 13. By superimposing the input impedance characteristics of the IO-PDN also in Figure 13, it can be noticed that for C_{mim} = 3 nF, the resonant peak of the input impedance indeed coincides with the 330 MHz frequency component of the current signature. This confirms the cause of increased power ground noise voltage for C_{mim} = 3 nF connected across the power bus of the DDR-IOs switching at 333 MHz. As the resonance noise is caused by the on-die High-K MIM DECAP C_{mim} and the effective loop inductance of the IO-PDN, the value of this loop inductance can be computed as 76 pH for C_{mim} = 3 nF and resonant frequency equal to 330 MHz. As shown in Figure 13, this effective loop inductance value correlates well with the simulated effective loop inductance value of 74.6 pH of the IO-PDN at 330 MHz. The effective self and mutual loop inductances of PDNs defined in the package layout are also obtained by simulations as shown in Figure 14.

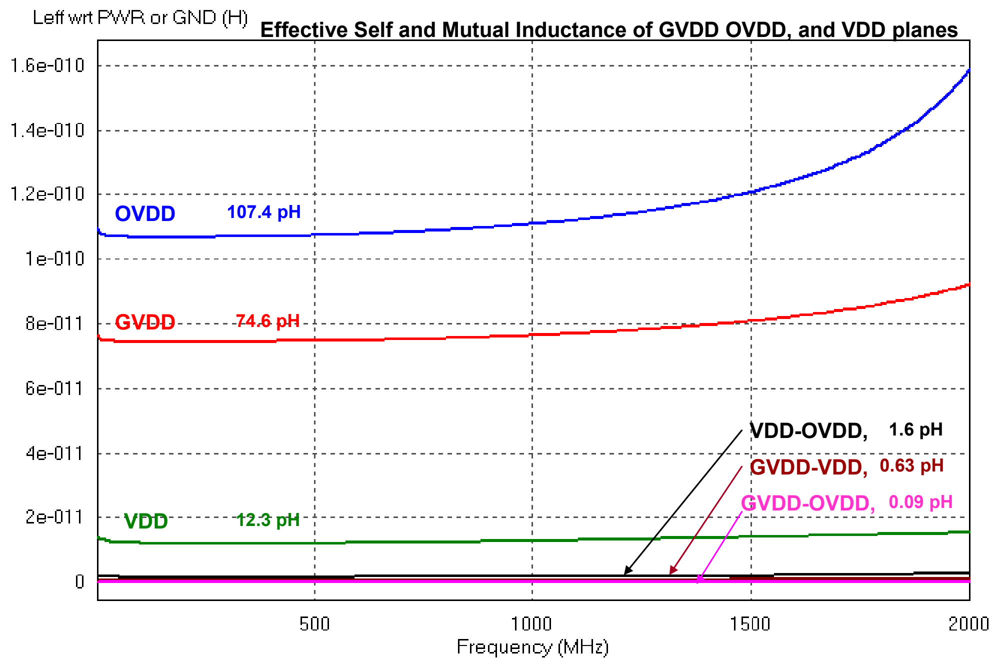


Figure 14. Effective Loop-inductance of PDN's

Therefore, based on this interesting feature, it can be inferred that for a given value of effective loop inductance of the IO-PDN, certain value of the on-die High-K MIM DECAP can always cause increased noise voltage across the power bus of the DDR-IOs switching at some frequency. Assuming that the effective loop inductance value of the IO-PDN of a package is known by simulation or measurement, the on-die High-K MIM DECAP value can be obtained from the resonant frequency equal to the switching frequency of the IOs.

Figure 15 illustrates those values of C_{mim}, which may cause increased power-ground noise voltage across the power bus of the DDR IOs switching simultaneously. For example, from Figure 14 it can be observed that for IO-PDN loop inductance of 76 nH, C_{mim} = 2 nF may generate increased power-ground noise voltage with DDR-IOs switching at 400 MHz.

Based on the time domain simulation of the FCBGA package with C_{mim} = 2 nF across the power bus, the increasing power-ground noise voltage with 64 DDR-IOs switching simultaneously at 400 MHz is found as shown in Figure 16. Note that the peak-peak power-ground noise voltage is reduced for C_{mim} = 1 nF and C_{mim} = 4 nF with 64 DDR-IOs switching simultaneously. It is critical to notice that the on-die High-K

MIM DECAP value, which may generate more noise voltage at a switching frequency, increases if the effective loop inductance of the IO-PDN is reduced.

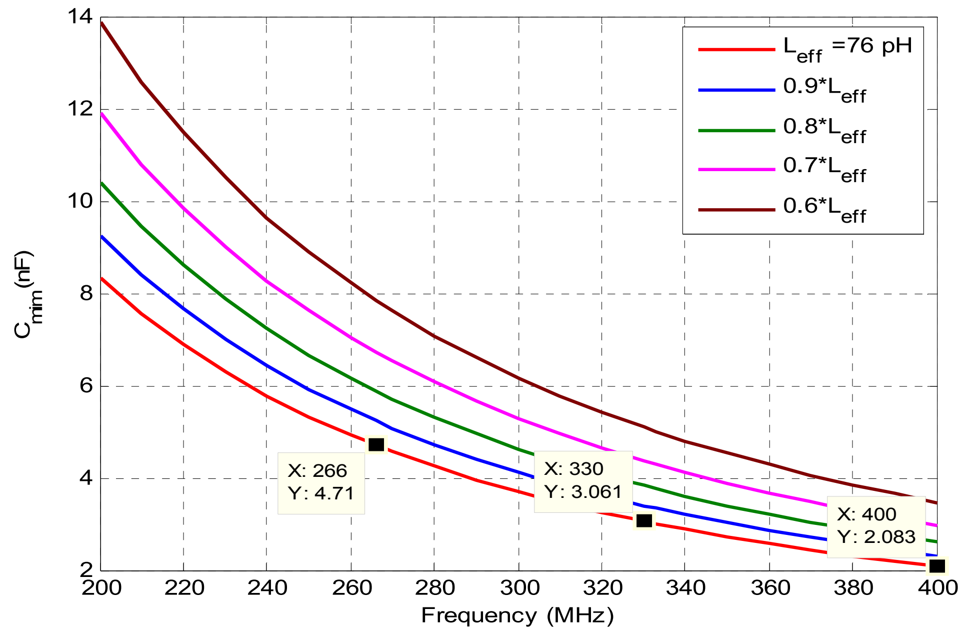


Figure 15. MIM Capacitance for increased power bus noise at specific switching frequency

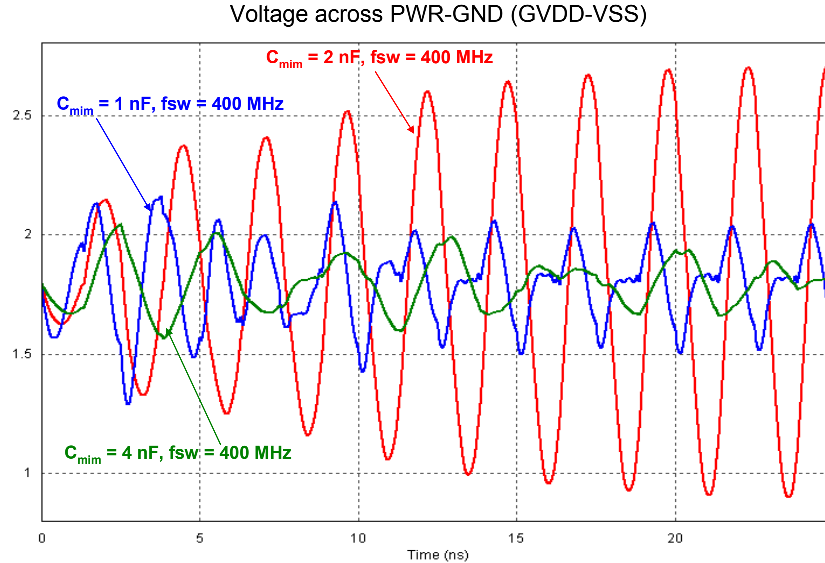


Figure 16 Power-ground noise voltages for switching DDR-IOs with certain values of on-die High-K MIM DECAP

The increasing noise voltage for certain values of C_{mim} can be prevented by incorporating a resistance R_{c4} of small value in the power-ground path of the IO-PDN of the package, as shown in Figure 8. As shown in Figure 17, the power-ground noise voltages considering R_{c4} = 0.1 Ω and 0.25 Ω with C_{mim} = 3 nF across the power bus are obtained from the time domain simulation with 64 DDR-IOs switching

simultaneously at 333 MHz. The peak to peak noise voltage ripple is reduced more with $R_{c4} = 0.1\ \Omega$ as compared to $R_{c4} = 0.25\ \Omega$.

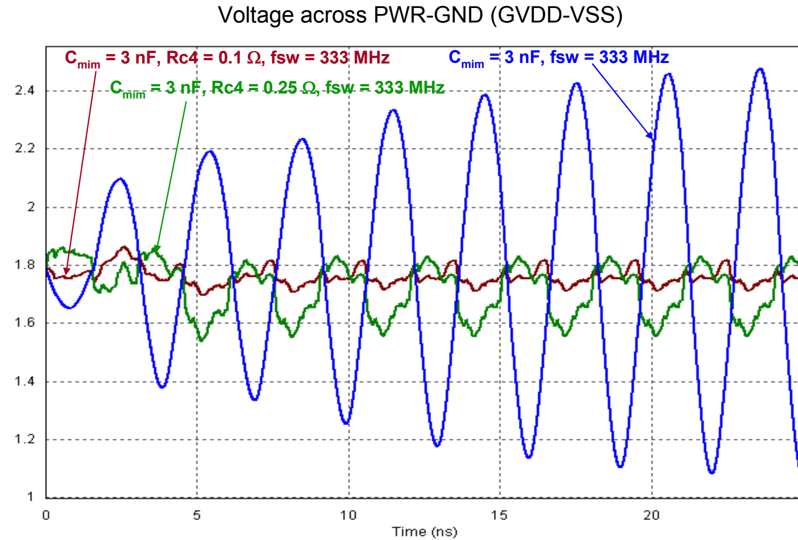


Figure 17 Power-ground noise voltage for DDR-IOs switching at 333 MHz for $C_{mim} = 3$ nF and Rc4 = 0.1 Ω

Notice that if $C_{mim} = 3$ nF is assumed as the on-die capacitance to completely decouple the effective loop inductance, $L_{eff} = 74.6$ H, then the resistance R_{c4} can be estimated from $\sqrt{\frac{L_{eff}}{C_{mim}}} = 0.16\ \Omega$ [6].

Based on the time domain simulation using different values of MIM capacitance, such as $C_{mim} = 0$ (red color plots), 1 nF (green color plot), 10 nF (brown color plots), and 20 nF (black color plots) with 64 DDR-IOs switching simultaneously at 333 MHz, corresponding to 101010 bit pattern, the voltage waveforms at the receiver end for a switching signal, a victim signal held high and a victim signal held low are shown in Figure 18.

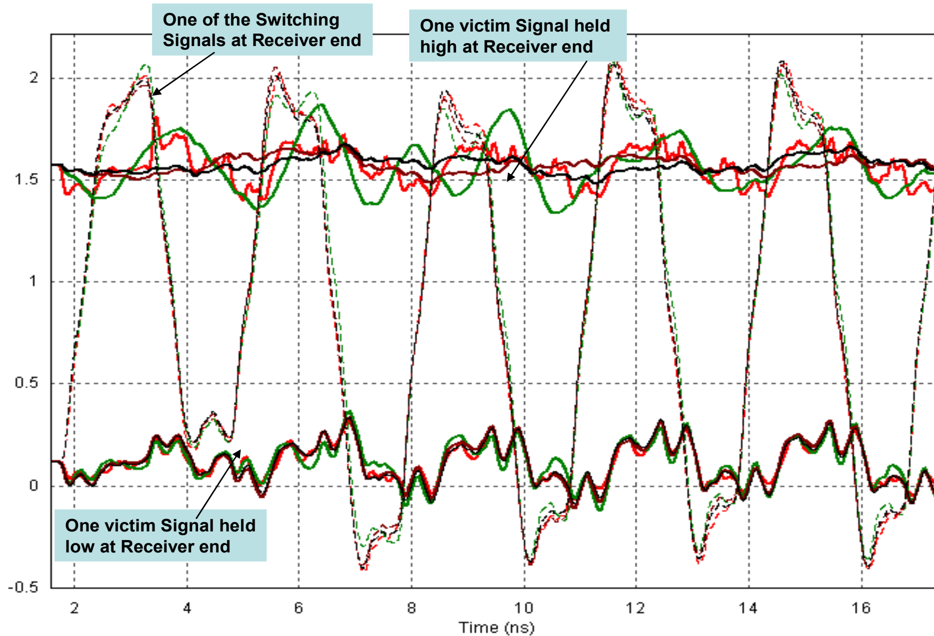
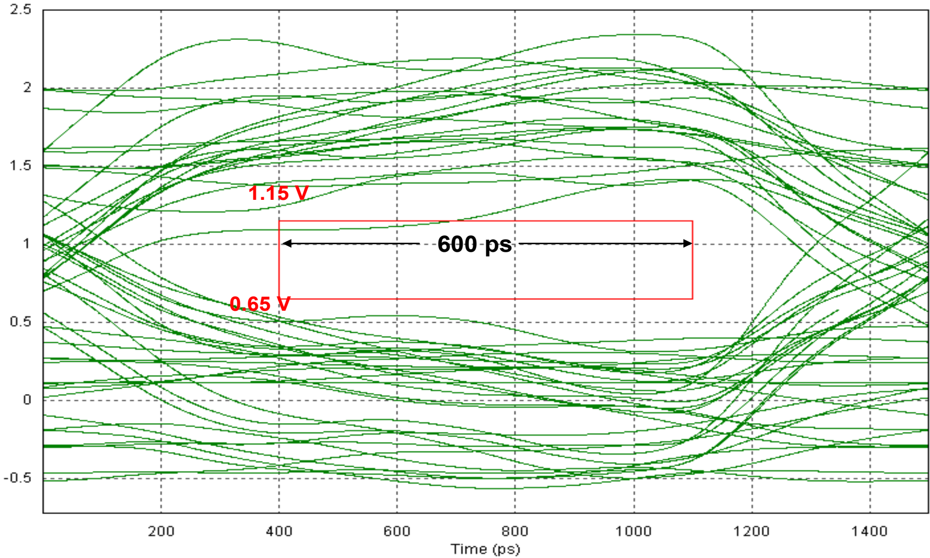
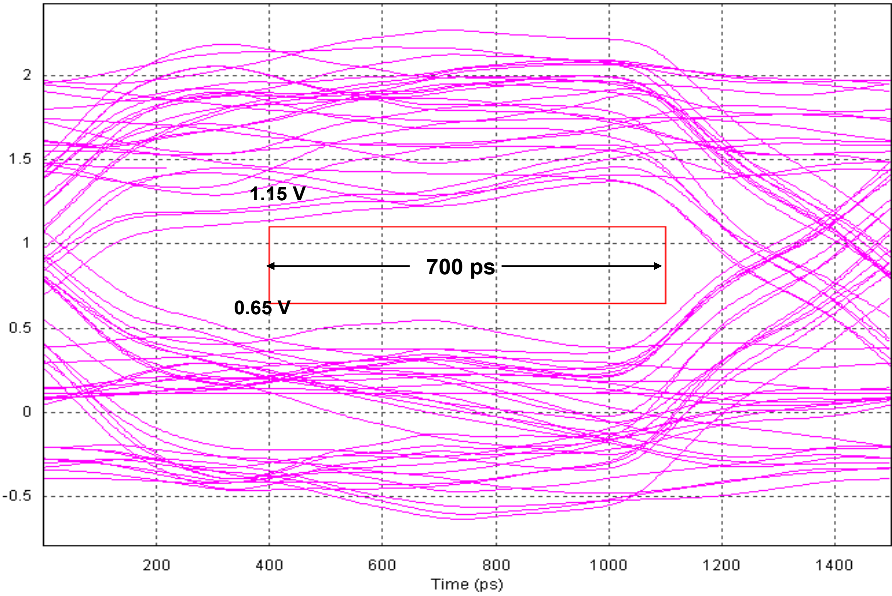


Figure 18 Output voltages for a switching signal, a victim signal held high and a victim signal held low

Next, a comparative study of SSN for FCBGA package due to different values of on-die High-K MIM DECAP added to the IO-PDN is described using data eye-diagram as a figure of merit. In order to generate the data-eye diagram, long time simulation is performed with pseudo random bit pattern for each of the 64/144 drivers switching at 333 MHz. Such simulations are performed for different types of terminations and switching patterns. The eye diagrams corresponding to a switching output signal at the receiver end for C_{mim} = 1nF and 10 nF respectively are shown in Figure 19.



(a)



(b)

Figure 19 Eye diagrams for a switching signal with (a) C_{mim} = 1 nF, (b) C_{mim} = 10 nF

The eye diagram in Figure 19 (a), with less signal distortion and wider data valid window, is cleaner than that in Figure 19 (b).

Part 2

The block diagram representation of the model to study the effect of on-die High-K MIM DECAP per IO in reducing SSN due to DDR IO drivers is shown in Figure 20. In this section frequency domain and time domain simulation results are described considering the on-die High-K MIM DECAP per IO with its distributed circuit model as shown in Figure 3.

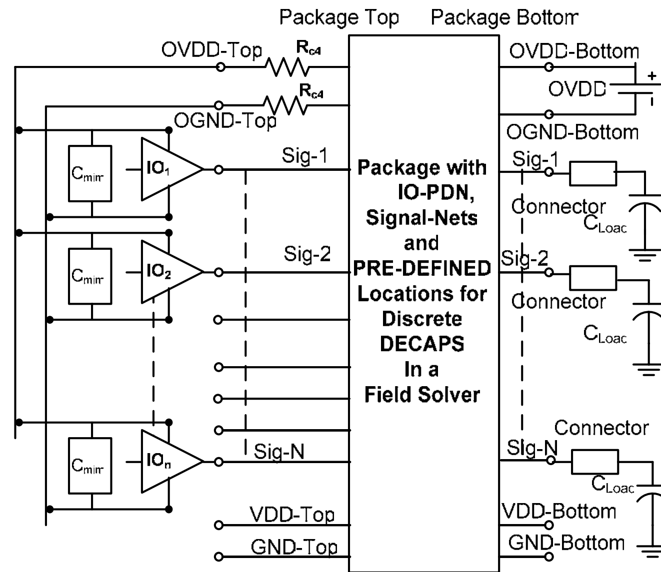


Figure 20. SSN simulation setup considering MIM-capacitance per IO

Based on frequency domain simulations, plots for self input impedances of the IO-PDN at the die location on the top of the package with/without R_{c4} and with lumped C_{mim} or distributed model of on-die High-K MIM DECAP are shown Figure 21.

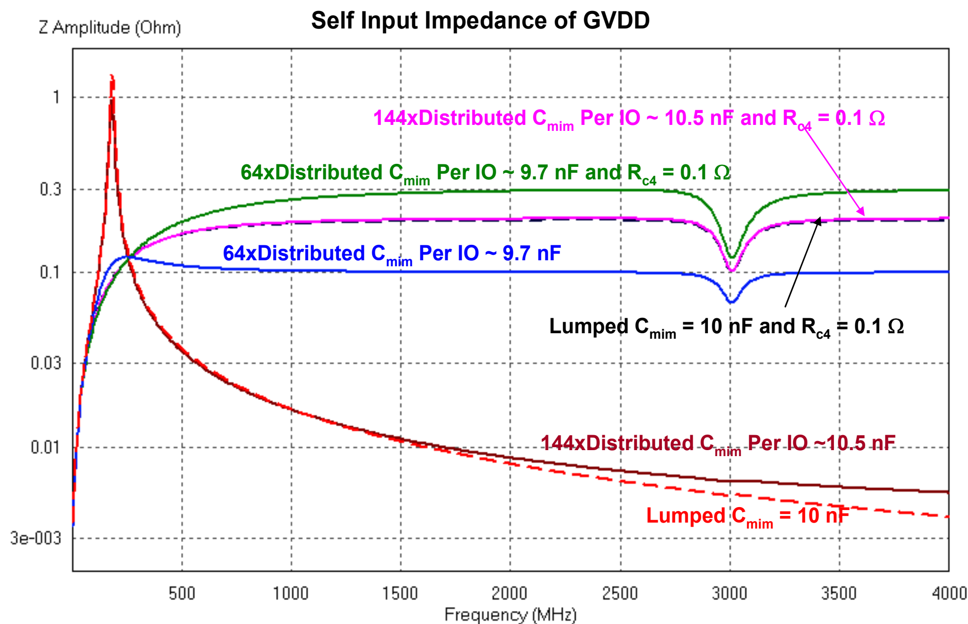


Figure 21 Input impedance of IO-PDN for lumped and distributed C_{mim}

It can be observed from Figure 21 that the input impedance characteristic with distributed on-die High-K MIM DECAP per IO based on its physically implementation as shown in Figure 3, coincides with that for the lumped C_{mim} = 10 nF. Also, the resonant peaks of these input impedance characteristics in the low frequency range are removed by using R_{c4} = 0.1 Ω. Thus, resonant free input impedance characteristic of the IO-PDN is realized over a wide frequency range.

Using distributed model of the on-die High-K MIM DECAP per IO, as shown in Figure 3, with R_{mim} = 10 Ω, C_{mim} = 37 pF, R_{metal} = 1.75 Ω, R_{c4} = 0, and considering 64 DDR-IOs switching simultaneously at 333 MHz, corresponding to 101010 bit pattern, Figure 22 shows the voltage waveforms at the receiver end for a switching signal, a victim signal held high and a victim signal held low.

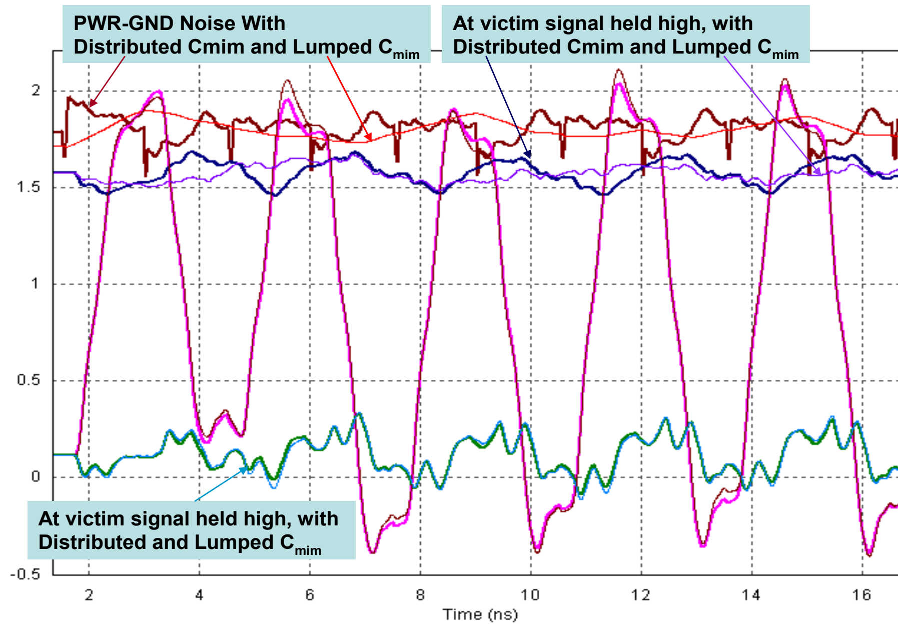


Figure 22. Output voltages for a switching signal, a victim signal held high and a victim signal held low using lumped and distributed C_{mim}

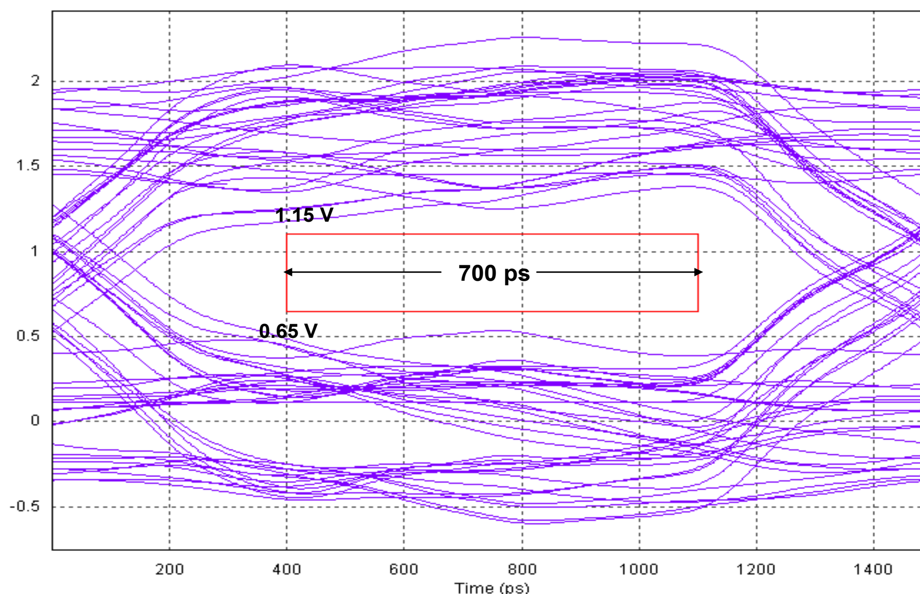


Figure 23 Eye diagrams for a switching signal with 64xdistributed C_{mim} per IO as shown in Figure 3

Considering 64 DDR-IOs switching simultaneously at 333 MHz, connected to the IO-PDN power bus with 64 times the distributed circuit model of the on-die High-K MIM DECAP per IO with $R_{mim} = 10\ \Omega$, $C_{mim} = 37$ pF, $R_{metal} = 1.75\ \Omega$, and $R_{c4} = 0$, the eye diagram for a switching signal at the receiver end is obtained as shown in Figure 23.

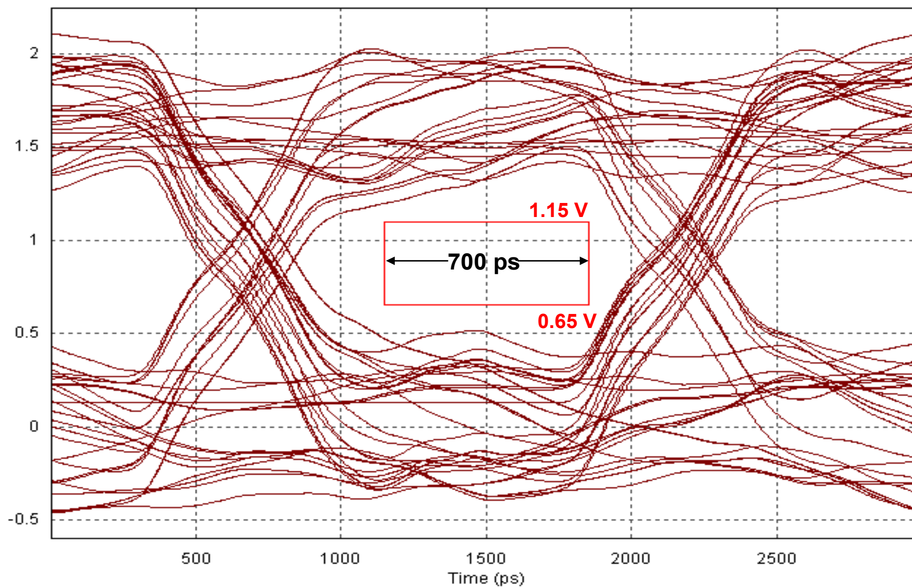


Figure 24 Eye diagrams for a switching signal with 144xdistributed C_{mim} per IO as shown in Figure 3

Next, considering 144 times the distributed circuit model of the on-die High-K MIM DECAP per IO across the IO-PDN power bus, with 64 DDR-IOs switching simultaneously at 333 MHz, the eye diagram corresponding to a switching signal at the receiver end is obtained from the time domain simulation as shown in Figure 24. The distributed circuit model parameters of the on-die High-K MIM DECAP per IO are approximated, corresponding to the distributed circuit models shown in Figure 5, as $R_{mim} = 0.1\ \Omega$, $C_{mim} = 18$ pF, and $R_{metal} = 1\ \Omega$. The eye diagram in Figure 24 is cleaner with more eye opened, which signifies better signal quality with less noise and more noise margin.

5. Conclusion

Considering a multilayer FCBGA package, the effect of on-die High-K MIM DECAP in reducing SSN due to several DDR-IOs switching simultaneously is discussed throughout this paper by means of efficient time domain and frequency domain simulations. The circuit models developed for on-die High-K MIM DECAP per IO is described based on the physical implementations in different ways to provide flexibility of integration in the die. Based on the package level modeling and simulation results described in this paper, it is found that the SSN reduction by the distributed model of the on-die High-K MIM DECAP per IO is close to that of an ideal capacitor. Methodology to estimate the critical value of the on-die High-K MIM DECAP for a given value of the effective IO-PDN loop inductance and the switching frequency of the IOs, which may give rise to increasing power-ground noise voltage, is discussed in the paper. This provides a design guide line for selecting a minimum value of the on-die High-K MIM DECAP to reduce the power-ground noise voltage and the resultant SSN. Based on these simulations, the interactions of the PDN with switching signals of the package is discussed in terms of the self and transfer input impedances, peak to peak noise voltage due to large switching current through the effective loop inductance of the IO-PDN and the eye diagram as the figure of merits. By means of the detailed SSN study described in this paper, it is found that on-die High-K MIM DECAP of significant amount is critical to realize the resonant free input impedance of the IO-PDN over a wide frequency range. The effective physical implementation of on-die High-K MIM DECAP is critical for mitigating the power-ground noise voltage generated in the package due to several DDR-IOs switching simultaneously. This in turn improves the SSN performance of the packages.

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