Study of Simultaneous Switching Noise Reduction for Microprocessor Packages by Application of High-K MIM Decoupling Capacitors

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Purpose

- Power Integrity (PI) performance improvement of packages due to On-Die High-K MIM DECAPs
- Simultaneous Switching Noise (SSN) performance improvement of microprocessor packages with DDR interface
- Importance of Effective Physical implementation of On-die High-K MIM DECAP
- Distributed Circuit Models of On-die High-K MIM DECAP for accurate analysis and to provide design guidelines
- System level modeling and simulation results for a package with On-die High-K MIM DECAPS and DDR-interface
Outline

- SSN-Basics/Background-Motivation for work
- On-die High-K MIM DECAP
  - Pros & Cons,
  - Physical implementation and
  - Distributed models for On-die High-K MIM DECAP
- Modeling and Simulation Methodology
  - Model of the Chip/DIE and Package interface
- Simulation Results to study SSN:
  - Input impedance of IO-PDN (IO-Power Delivery Network)
  - PWR-GND and Quite-line Noise voltages, and
  - EYE-diagram for an actively switching IO voltage
- Measured Results
- Conclusions
Background

Simple Schematic for Simultaneous Switching Noise (SSN)

On-Chip Switching & Off-chip Switching → 2 Major cases

This work focuses on On-chip level DECAPS

On-Chip/Onc-DIE

On-Chip Capacitance

On-Package Capacitance

System

Off-Chip Capacitance

Reference: Digital Signal Integrity by Brian Young

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Background

On-Chip Switching: Current paths to charge and discharge input capacitance of Driver-1 by Driver-3 for High to Low switching

Charge current for H-L switching uses $L_p-L_g$ loop

Discharge current is contained On-chip
Background

Off-Chip Switching (H to L of DRV-1):
Current paths to Charge/Discharge off-chip capacitances

Reference: Digital Signal Integrity by Brian Young
On-chip to Off-Chip Switching (DRV-1, H to L) with On-Chip Capacitance: Current paths to Charge/Discharge off-chip capacitances

Charge/discharge current for H-L switching uses \( L_{s1} \) and \( L_g \) loop

Additional charging current through On-chip cap uses \( L_p \) and \( L_{s1} \) loop

Peak PWR-GND noise is reduced by balancing the current through Package (during H-L and L-H switching)
Effective Loop Inductance for On-chip to Off-Chip Switching with On-Chip Capacitance:

- High-Low/Low-High switching involves two different effective loop inductances
  - Power-Signal loop for IO switching Low to High
    \[ L_{\text{eff, LH}} = L_p + L_s - 2M_{ps} \implies \text{Switching Noise}, \quad V_{\text{ssn, LH}} = L_{\text{eff, LH}} \frac{di}{dt} \]
  - Signal-GND loop for IO switching High to Low
    \[ L_{\text{eff, HL}} = L_g + L_s - 2M_{gs} \implies \text{Switching Noise}, \quad V_{\text{ssn, HL}} = L_{\text{eff, HL}} \frac{di}{dt} \]
  - PWR-GND loop between each transition periods (HL or LH)
    \[ L_{\text{eff, pg}} = L_p + L_g - 2M_{pg} \implies \text{Power Supply Noise}, \quad V_{\text{chip}} = V_s - L_{\text{eff, pg}} \frac{di}{dt} \]

⇒ \[ V_{\text{chip}} = V_s - \text{Rail Collapse/Supply voltage droop} \]
Rail Collapse Reduction using On-chip/die DECAPS

- Inductive voltage drop across PWR-GND loop inductance (due to total switching current of several IOs switching simultaneously)
  ⇒ Rail Collapse/Supply voltage droop across IO-PDN (during H-L and L-H switching and the transition between H-L and L-H)
  ⇒ Signal Integrity problems (ex: Delays)

- Adding DECAPS at several stages of the system
  ⇒ Most effective method to COMBAT Inductive voltage drop
  ⇒ Bypassing effective loop inductance of IO-PDN*
  ⇒ Reduced PDN-Loop Impedance over a wide frequency

- On-Chip/die DECAPS ⇒ Effective method for reducing high frequency noise

(* IO-PDN ⇒ IO Power Delivery Network)
Example

Consider 1.8 V, 18 Ω DDR-IOs with typical edge rate of 1 ns

⇒ 100 mA/ns of peak current per IO switching

⇒ 6.4 A/ns for 64 IOs switching simultaneously

\[
C = I \frac{dt}{dv} = I \frac{\text{Edge Rate}}{\text{Ripple} \times V_{\text{nominal}}} = 6.4 \times \frac{1 \text{ ns}}{0.1 \times 1.8 \text{ V}} = 35.36 \text{ nF}, \text{ assuming, Ripple} = 10\%
\]

⇒ Required internal capacitance to supply charge at high frequencies to keep power supply within 10% of the nominal voltage
Why On-die High-K MIM DECAP?

- More effective as compared to On-die Gate-Oxide DECAPS
- No Chip/Silicon area penalty for On-die High-K MIM DECAP as compared to Gate-Oxide DECAPs
- Can Exceed physical boundaries of IOs (may extend over non-IO areas of the DIE)
- Very significant amount of On-Die High-K MIM DECAP (> 20 nF) can be realized

- On-die High-K MIM DECAP with Capacitance density = 5 to 8fF/µm² for 90 nm SOI technology has been realized by vapor deposition of alternating dielectric Layers (HfO2 and Ta2O5) between TaN electrodes

Generic Cross sectional view of Process-stack

- LM GND
- LM PWR
- Top of MIM-Capacitance
- Insulator
- Bottom of MIM-Capacitance
- LM-1 GND
- LM-1 PWR
- LM-2
- LM-3
- Transistors
- Oxides

MIM DECAP is located below last thick metal (between LM & LM-1)

Vias are used to make contacts from LM to top and bottom of MIM DECAP

Top MIM layer is cut out to allow vias from LM GND to bottom MIM layer
On-die High-K MIM DECAP modules are connected to IOs at an effective Pitch dictated by PWR/GND C4 bumps.

Electrical parameters of interest are:

- \( R_{\text{mim}} \rightarrow \text{MIM plate resistance} + \text{Via Resistance} \text{ [50 } \Omega \text{/sq] } \)
- \( C_{\text{mim}} \rightarrow \text{MIM Capacitance} = \text{Capacitance Per unit area} \text{ (fF/} \mu \text{m}^2) \times \text{Area (} \mu \text{m}^2) \)
- \( R_{\text{metal}} \rightarrow \text{Metal resistance connecting IOs to PWR/GND C4's} \)
Distributed Circuit Model of On-die High-K MIM DECAP
(for improved Physical implementation-2)

• On-die High-K MIM DECAP Module is divided in small subsections
• Next, each subsection is modeled as a distributed R-C network
• Vias from metal to plates have significant resistances
  - Must be modeled carefully

Each IO’s PWR/GND terminal is connected to On-die High-K MIM DECAP using an extra last metal line

⇒ Improved $R_{metal}$ and $R_{mim}$
Distributed Circuit Model of On-Die High-K MIM DECAP

- Appropriate strapping of DIE-layer is required to make On-die High-K MIM DECAP available to all IOs
Circuit representation of On-die High-K MIM DECAP
(for further improved Physical implementation-3)
- By reducing Via-MIM spacing between PWR-GND plates and
- By Custom integration of On-die high-K MIM DECAP into IO itself – as in Fig (a)
⇒ Electrical performance → Ideal capacitor

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LM to LM-1 power grid for Several (6/7) I/O cks

Image of MIM for one IO ckt

MIM-CAP section for Distributed Model

All figures shown here are not to the scale
Estimating R and C of MIM-CAP for developing a Distributed CKT Model
Distributed Model of ‘M’ section of MIM-CAP
Distributed Model of ‘V’ section of MIM-CAP
Distributed Circuit Model Per-IO

7 ‘V’ and 17 ‘M’ Section in Parallel Per IO
12 Layer Ceramic FCBGA Package used for SSN study
Block diagram model used for Time domain and Frequency domain simulation and analysis to study effect of On-die High-K MIM DECAP

Both PDN and IO Signal nets are considered to account all inductive and capacitive coupling of the Package imported in the EM Field solver
- SPEED2000 and
- PowerSI from Sigrity
DDR2/DDR3 System Level Modeling and Simulation:

- Detailed Package Model inside the Field Solver
  (Speed2K & PowerSI with built in SPICE Circuit simulator)
- Simultaneous switching of 62 out of 64 I/Os
- Full strength 18 Ω IBIS(3.2) model of DDR2/DDR3 IOs
- DDR2/DDR3 data load connector model
- Off-chip Capacitances representing Receivers
- On-Die High-K MIM DECAPS as
  - First as Lumped Model, and
  - Next as Distributed models (for physical implementation 1-3)
DDR2 data load Connector circuit
SSN simulation setup considering Lumped model of On-die High-K MIM DECAP
Self and transfer Input Impedance of PDNs

Self and Transfer-Input Impedance of GVDD, OVDD, and VDD planes

|Z| (Ohm)

- OVDD
- GVDD
- VDD
- VDD-OVDD
- VDD-GVDD
- OVDD-GVDD

Frequency (GHz)

1 2 3 4
Self Input Impedance of IO-PDN with different values of On-chip DECAPS

Self Input Impedance of GVDD with different values of $C_{\text{mim}}$

- $C_{\text{mim}} = 0$
- $C_{\text{mim}} = 330$ pF
- $C_{\text{mim}} = 1$ nF
- $C_{\text{mim}} = 3$ nF
- $C_{\text{mim}} = 6$ nF
- $C_{\text{mim}} = 10$ nF

Frequency (MHz)

$|Z|$ (Ohm)

$C_{\text{mim}} = 0$

$C_{\text{mim}} = 330$ pF

$C_{\text{mim}} = 1$ nF

$C_{\text{mim}} = 3$ nF

$C_{\text{mim}} = 6$ nF

$C_{\text{mim}} = 10$ nF

$C_{\text{mim}} = 0$

$C_{\text{mim}} = 330$ pF

$C_{\text{mim}} = 1$ nF

$C_{\text{mim}} = 3$ nF

$C_{\text{mim}} = 6$ nF

$C_{\text{mim}} = 10$ nF

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PWR-GND Noise Voltage vs. DIE-DECAP for DDR667

Voltage across PWR-GND with $R_{c4} = 0$

- $C_{mim} = 330 \text{ pF}$
- $C_{mim} = 1 \text{ nF}$
- $C_{mim} = 3 \text{ nF}$
- $C_{mim} = 6 \text{ nF}$
- $C_{mim} = 10 \text{ nF}$
- $C_{mim} = 15 \text{ nF}$
- $C_{mim} = 20 \text{ nF}$

Increasing $PWR-GND$ noise voltage @ 333 MHz

$3 \text{ ns} \Rightarrow f = 333 \text{ MHz}$
PWR-GND Input impedances and Frequency Spectrum (FFT) of Switching current through PWR-GND

Input impedance Peak is shifted @333 MHz due to $C_{\text{mim}} = 3 \text{ nF}$

FFT of switching Current through PWR-GND $\rightarrow$ 333 MHz comp. coincides with Impedance peak

$f_0 = 333 \text{ MHz}$, and $C_{\text{mim}} = 3 \text{ nF}$

$\Rightarrow L_{\text{eff}} = 76 \text{ pH}$

Simulated PWR-GND loop inductance correlates
Effective Loop Inductances of Package PDNs

Effective Self and Mutual Inductance of GVDD, OVDD, and VDD planes

- OVDD: 107.4 pH
- GVDD: 74.6 pH
- VDD: 12.3 pH
- VDD-OVDD: 1.6 pH
- GVDD-VDD: 0.63 pH
- GVDD-OVDD: 0.09 pH

Graph showing inductance values over frequency range 0 to 2000 MHz.
$C_{\text{die/mim}}$ vs. Clock frequency for a given $L_{\text{eff}}$ of Package
PDN to avoid increasing PWR-GND noise voltage

$\Rightarrow$ for $L_{\text{eff}} = 76 \text{ pH}$, $C_{\text{mim}} = 2 \text{ nF}$ generates increased noise voltage with DDR800 IOs switching at 400 MHz.

X-axis label 'Frequency (MHz)'
$\Rightarrow$ Half of the clock frequency
Voltage across PWR-GND

C_{mim} = 2 \text{nF}
\quad f_{sw} = 400 \text{ MHz}

C_{mim} = 3 \text{nF}
\quad f_{sw} = 333 \text{ MHz}

C_{mim} = 4.7 \text{nF}
\quad f_{sw} = 266 \text{ MHz}
Power-ground noise voltages for DDR800-IOs switching @ 400 MHz for $C_{\text{die/mim}} = 1 \text{ nF}, 2 \text{ nF and 4 nF}$

- $C_{\text{mim}} = 2 \text{ nF}$
- Increasing PWR-GND noise voltage @ 400 MHz

Voltage across PWR-GND with $R_{c4} = 0$

- $C_{\text{mim}} = 1 \text{ nF}, f_{sw} = 400 \text{ MHz}$
- $C_{\text{mim}} = 2 \text{ nF}, f_{sw} = 400 \text{ MHz}$
- $C_{\text{mim}} = 4 \text{ nF}, f_{sw} = 400 \text{ MHz}$
Increasing noise voltage for $C_{\text{mim}}$’s generating resonance can be prevented by incorporating resistance $R_{c4}$ of small value in PWR-GND path of IO-PDN of PKG.
Voltage across PWR-GND with $R_{c4} = 0.1 \, \Omega$

- $C_{\text{mim}} = 330 \, \text{pF}$
- $C_{\text{mim}} = 1 \, \text{nF}$
- $C_{\text{mim}} = 3 \, \text{nF}$
- $C_{\text{mim}} = 10 \, \text{nF}$
- $C_{\text{mim}} = 6 \, \text{nF}$
- $C_{\text{mim}} = 15 \, \text{nF}$
- $C_{\text{mim}} = 20 \, \text{nF}$
Peak Noise Voltage across PWR-GND of DDR667-IOs vs. DIE-Capacitance ($C_{\text{die}}$).

$\Rightarrow$ No Voltage Oscillation for $C_{\text{die}} = 3 \text{ nF}$ and $R_{c4} = 0.1 \Omega$

$\Rightarrow$ Voltage Oscillation for $C_{\text{die}} = 3 \text{ nF}$ and $R_{c4} \neq 0$
Simulated voltages at a Receiver load of an actively switching IO with 62 DDR2-667-I0s switching simultaneously at 333 MHz, as 101010
Simulated voltages at a Receiver load of an actively switching IO with 62 DDR2-667-IOs switching simultaneously at 333 MHz, as 101010

Noise at signal held high reduces with increasing $C_{mim}$

Noise at signal held low remains unchanged with increasing $C_{mim}$
EYE diagrams for switching output signal at the receiver end with \( C_{\text{mim}} = 1\text{nF} \) and 64 DDR2 IOs switching simultaneously at 333 MHz.
EYE diagrams for switching output signal at the receiver end with $C_{\text{mim}} = 10\,\text{nF}$ and 64 DDR2 IOs switching simultaneously at 333 MHz.

EYE with $C_{\text{mim}} = 10\,\text{nF}$ has wider and cleaner data Valid window as compared to $C_{\text{mim}} = 1\,\text{nF}$.
Load-connector Model for DDR3

![Load-connector Model for DDR3 Diagram]
Eye diagram with $C_{\text{mim}} = 3 \text{ nF}$, $Rc4 = 0.25 \, \Omega$ and 64 DDR3 IOs switching simultaneously at 400 MHz

EYE is Cleaner With valid data for $C_{\text{mim}} = 3 \text{ nF}$
Eye diagram with $C_{\text{mim}} = 3 \text{ nF}$, $Rc4 = 0.25 \ \Omega$ and 62 DDR3 IOs switching simultaneously at 400 MHz.
Eye diagram with $C_{\text{mim}} = 10 \text{ nF}$, $R_c = 0.25 \Omega$ and 62 DDR3 IOs switching simultaneously at 400 MHz.

Noise at signal held high reduces with $C_{\text{mim}} = 3 \text{ nF}$. 
Eye diagram with $C_{\text{mim}} = 10 \text{ nF}$, $Rc4 = 0.25 \, \Omega$ and 62 DDR3 IOs switching simultaneously at 400 MHz

For $Rc4 = 0.15 \, \Omega$ shows improvement as compared to $Rc4 = 0.25 \, \Omega$

$Rc4 = 0.15 \, \Omega$ shows improves EYE opening and jitter as to $Rc4 = 0.25 \, \Omega$
Eye diagram with $C_{\text{mim}} = 10 \text{ nF}$, $Rc4 = 0.25 \Omega$ and 62 DDR3 IOs switching simultaneously at 400 MHz
SSN Simulation setup considering
Distributed model of On-die High-K MIM DECAP

Package with IO-PDN, Signal-Nets and PRE-DEFINED Locations for Discrete DECAPS In a Field Solver

Parameter values:
- C_{mim}
- R_{c4}
- IO_1
- IO_2
- IO_n
- VDD-Top
- GND-Top
- OVDD-Top
- OGND-Top
- OVDD-Bottom
- OGND-Bottom
- Sig-1
- Sig-2
- Sig-N
- Connector
- C_{Load}
Input impedance for both lumped Distributed $C_{\text{mim}}$

Lumped $C_{\text{mim}} = 10 \text{ nF, } R_{c4} = 0.1 \Omega$

64x Distributed $C_{\text{mim}}$ Per IO $\sim 9.7 \text{ nF, } R_{c4} = 0.1 \Omega$

64x Distributed $C_{\text{mim}}$ Per IO $\sim 9.7 \text{ nF and } R_{c4} = 0.25 \Omega$

Lumped $C_{\text{mim}} = 10 \text{ nF and } R_{c4} = 0.25 \Omega$

Lumped $C_{\text{mim}} = 10 \text{ nF}$
EYE diagrams for switching signal with 144x Distributed $C_{\text{mim}}$ per IO (Total $C_{\text{mim}} \sim 18 \text{ nF}$), and 64 IOs switching at 333 MHz.

EYE with Distributed $C_{\text{mim}}$ has valid data Window with more margin and less jitter.
Measured voltage across quite lines with 64 DDR2-667 IOs switching: MIM vs non-MIM results

<table>
<thead>
<tr>
<th>Bits Switching</th>
<th>MIM Pk-Pk mV</th>
<th>non-MIM Pk-Pk mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>184</td>
<td>620</td>
</tr>
<tr>
<td>32</td>
<td>144</td>
<td>536</td>
</tr>
<tr>
<td>16</td>
<td>133</td>
<td>520</td>
</tr>
<tr>
<td>8</td>
<td>71</td>
<td>414</td>
</tr>
</tbody>
</table>

BIG DELTA between MIM part and Non-MIM part!
CONCLUSION

• From results described in this paper, we have concluded that On-die High-K MIM DECAP of significant amount is critical
  - to realize the resonant free input impedance of the IO-PDN, and
  - to mitigate the PWR-GND noise voltage generated in PKG

• Increased amount of Capacitance density of On-die High-K MIM capacitors as compared to Gate-Oxide DECAPS provide significant improvements in noise, speed, power, Silicon-to-design correlation, debug time and time to market!

• Large amount of effective capacitance (~ 20 nF) can be obtained from On-die High-K MIM DECAP with appropriate physical implementation

• We have shown significant reduction in rail collapse and SSN by implementing On-die High-K MIM DECAP in a 90nm SOI microprocessor
Conclusion (Contd)

• Distributed circuit models for On-die High-K MIM DECAPs are discussed in detail

• We have shown that SSN reduction by the distributed model of the On-die High-K MIM DECAP is close to that of an ideal capacitor.

• It is shown that value of $R_{C4}$ ($R_{metal}$ plus PWR/GND resistance of C4’s) resistance is critical for SSN reduction using On-die High-K MIM DECAP.

• We have shown a Methodology to estimate critical value of
  
  - On-die High-K MIM DECAP for a known value of effective IO-PDN loop inductance and the switching frequency of IOs, and
  
  - Critical value of $R_{c4}$ resistance for known a known value of effective loop inductance of IO-PDN and DIE/MIM capacitance.
References


[4] [www.sigrity.com](http://www.sigrity.com)
