# Study of Simultaneous Switching Noise Reduction for Microprocessor Packages by Application of High-K MIM Decoupling Capacitors

By

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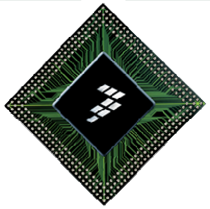

## DesignCon 2007, Santa Clara, CA

**January 29-Feb 2, 2007**

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# Purpose

- **Power Integrity (PI) performance improvement of packages due to On-Die High-K MIM DECAPs**
- **Simultaneous Switching Noise (SSN) performance improvement of microprocessor packages with DDR interface**
- **Importance of Effective Physical implementation of On-die High-K MIM DECAP**
- **Distributed Circuit Models of On-die High-K MIM DECAP for accurate analysis and to provide design guidelines**
- **System level modeling and simulation results for a package with On-die High-K MIM DECAPS and DDR-interface**

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# Outline

- **SSN-Basics/Background-Motivation for work**
- **On-die High-K MIM DECAP**
    - **- Pros & Cons,**
    - **- Physical implementation and**
    - **- Distributed models for On-die High-K MIM DECAP**
- **Modeling and Simulation Methodology**
    - **- Model of the Chip/DIE and Package interface**
- **Simulation Results to study SSN:**
    - **- Input impedance of IO-PDN (IO-Power Delivery Network)**
    - **- PWR-GND and Quite-line Noise voltages, and**
    - **- EYE-diagram for an actively switching IO voltage**
- **Measured Results**
- **Conclusions**

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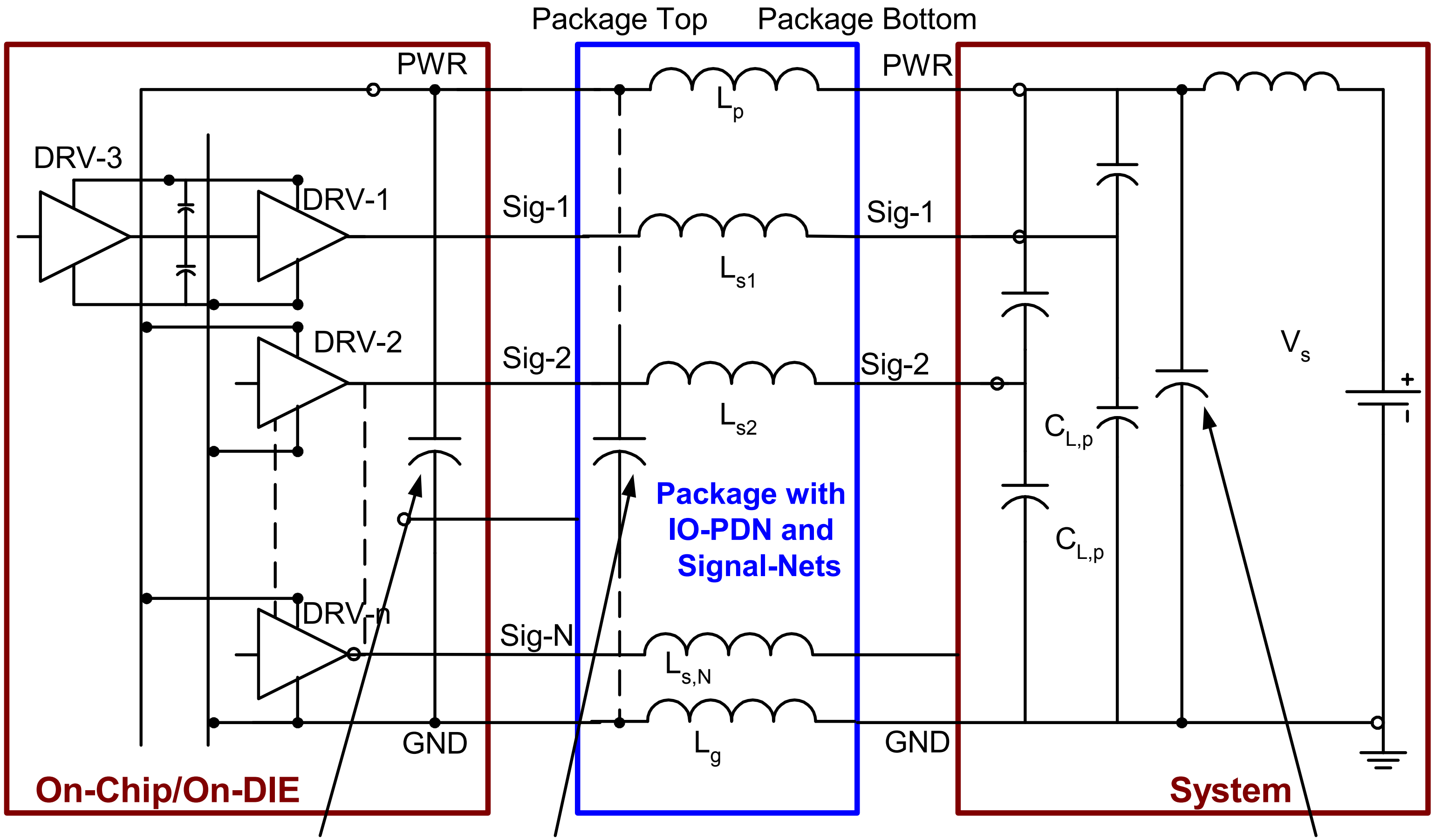
# Background

## Simple Schematic for Simultaneous Switching Noise (SSN)

## On-Chip Switching & Off-chip Switching ➔ 2 Major cases

This work focuses on On-chip level DECAPS



**On-Chip Capacitance** **On-Package Capacitance** **Off-Chip Capacitance**

**Reference: Digital Signal Integrity by Brian Young**

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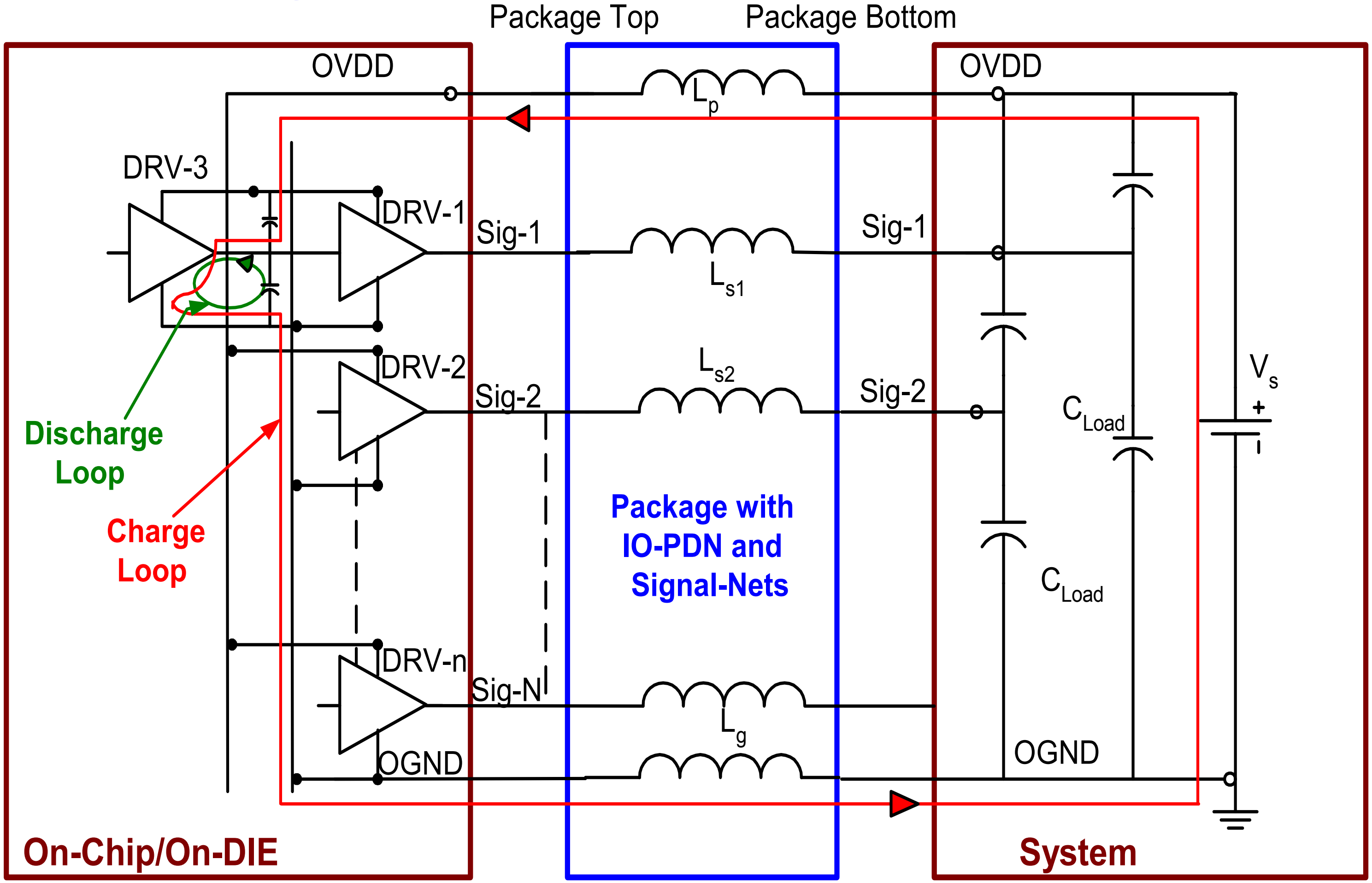
# Background

## On-Chip Switching: Current paths to charge and discharge input capacitance of Driver-1 by Driver-3 for High to Low switching



**Charge current for H-L switching uses $L_p$-$L_g$ loop**

**Discharge current is contained On-chip**

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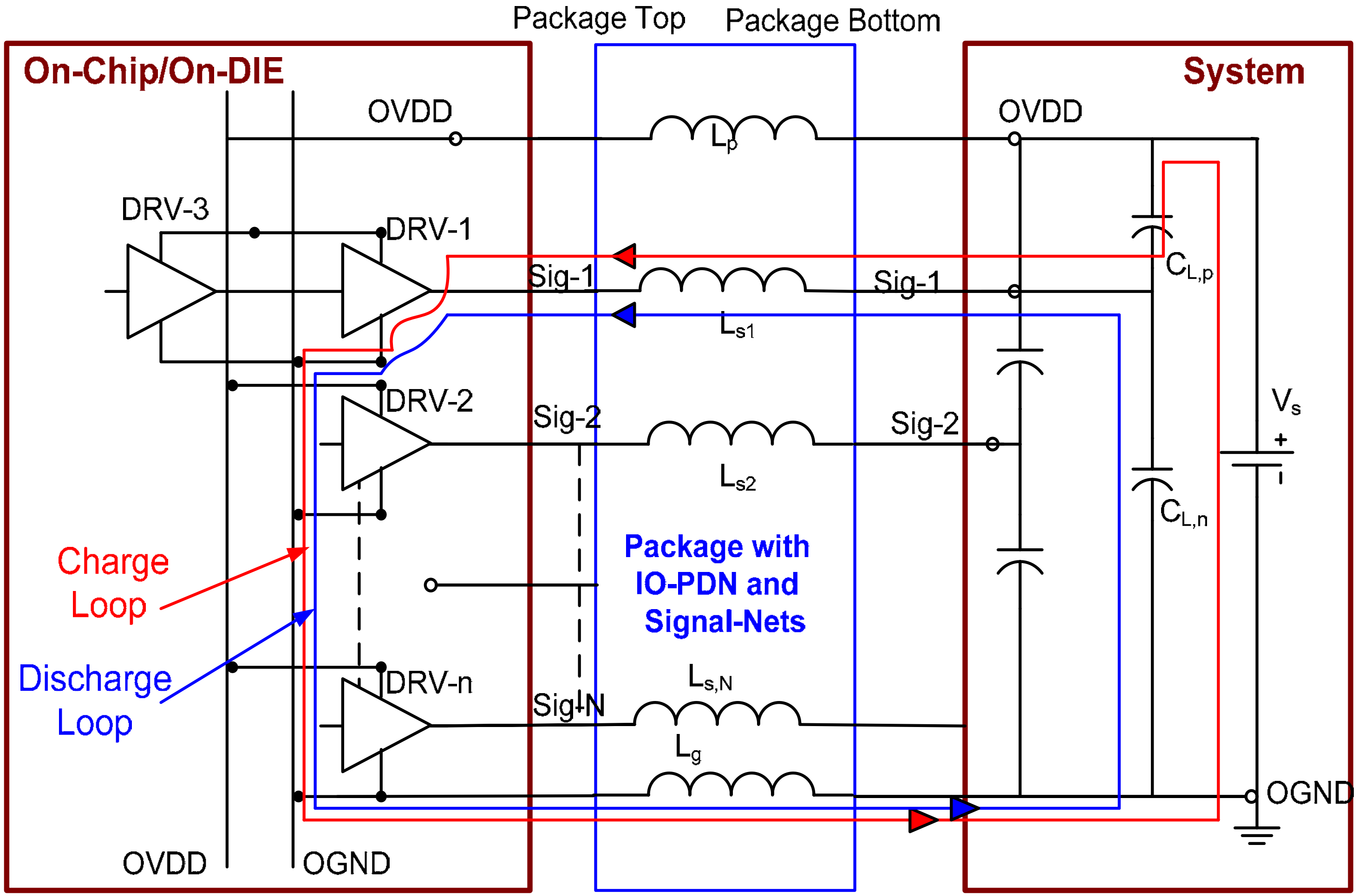
# Background

## Off-Chip Switching (H to L of DRV-1):

## Current paths to Charge/Discharge off-chip capacitances



**Charge/discharge current for H-L switching uses $L_{s1}$-$L_g$ loop**

**Reference: Digital Signal Integrity by Brian Young**

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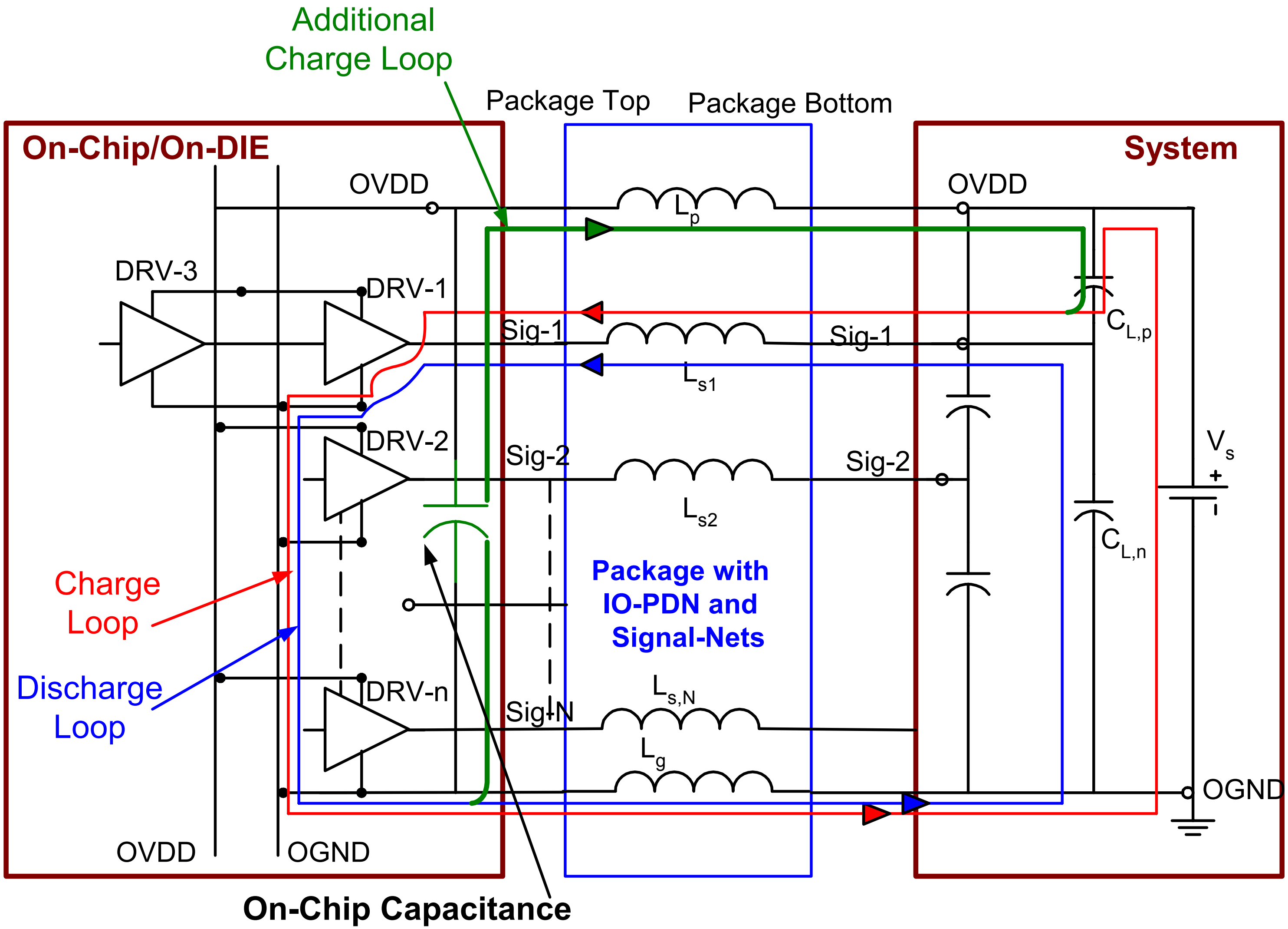
# On-chip to Off-Chip Switching (DRV-1, H to L) with On-Chip Capacitance: Current paths to Charge/Discharge off-chip capacitances



**Charge/discharge current for H-L switching uses $L_{s1}$ and $L_g$ loop**

**Additional charging current through On-chip cap uses $L_p$ and $L_{s1}$ loop**

⇓

**Peak PWR-GND noise is reduced by balancing the current through Package (during H-L and L-H switching )**

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# Effective Loop Inductance for On-chip to Off-Chip Switching with On-Chip Capacitance:

- High-Low/Low-High switching involves two different effective loop inductances

-Power-Signal loop for IO switching Low to High

$L_{eff,LH} = L_p + L_s - 2M_{ps}$ $\Rightarrow$ **Switching Noise,** $V_{ssn,LH} = L_{eff,LH} \frac{di}{dt}$

-Signal-GND loop for IO switching High to low,

$L_{eff,HL} = L_g + L_s - 2M_{gs}$ $\Rightarrow$ **Switching Noise,** $V_{ssn,HL} = L_{eff,HL} \frac{di}{dt}$

- PWR-GND loop between each transition periods (HL or LH)

$L_{eff,pg} = L_p + L_g - 2M_{pg}$ $\Rightarrow$ **Power Supply Noise,** $V_{chip} = V_s - L_{eff,pg} \frac{di}{dt}$

$\Rightarrow V_{chip} = V_s$ – Rail Collapse/Supply voltage droop

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# Rail Collapse Reduction using On-chip/die DECAPS

- Inductive voltage drop across PWR-GND loop inductance

(due to total switching current of several IOs switching simultaneously)

⇒ Rail Collapse/Supply voltage droop across IO-PDN

(during H-L and L-H switching and the transition between H-L and L-H)

⇒ Signal Integrity problems (ex: Delays)

- Adding DECAPS at several stages of the system

⇒ Most effective method to COMBAT Inductive voltage drop
⇒ Bypassing effective loop inductance of IO-PDN*
⇒ Reduced PDN-Loop Impedance over a wide frequency

- On-Chip/die DECAPS ⇒ Effective method for reducing high frequency noise

(* IO-PDN ⇒ IO Power Delivery Network)

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# Example

**Consider 1.8 V, 18 Ω DDR-IOs with typical edge rate of 1 ns**

**⇒ 100 mA/ns of peak current per IO switching**

**⇒ 6.4 A/ns for 64 IOs switching simultaneously**

$$C = I * \frac{dt}{dv} = I * \frac{\text{Edge Rate}}{\text{Ripple} * V_{\text{nominal}}}$$

$$= 6.4 * \frac{1\ \text{ns}}{0.1 * 1.8\text{V}} = 35.36\ \text{nF}$$ **, assuming, Ripple = 10%**

**⇒Required internal capacitance to supply charge at high frequencies to keep power supply within 10% of the nominal voltage**

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# Why On-die High-K MIM DECAP ?

- **More effective as compared to On-die Gate-Oxide DECAPS**

- **No Chip/Silicon area penalty for On-die High-K MIM DECAP as compared to Gate-Oxide DECAPs**

- **Can Exceed physical boundaries of IOs (may extend over non-IO areas of the DIE)**

- **Very significant amount of On-Die High-K MIM DECAP (> 20 nF) can be realized**

- **On-die High-K MIM DECAP with Capacitance density = 5 to 8fF/µm$^2$ for 90 nm SOI technology has been realized by vapor deposition of alternating dielectric Layers (HfO2 and Ta2O5) between TaN electrodes***

* Roberts, D.; Johnstone, W.; Sanchez, H.; Mandhana, O.; et.al, "Application of on-chip MIM decoupling capacitor for 90nm SOI microprocessor", Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, 5-7 Dec. 2005 Page(s): 72-75

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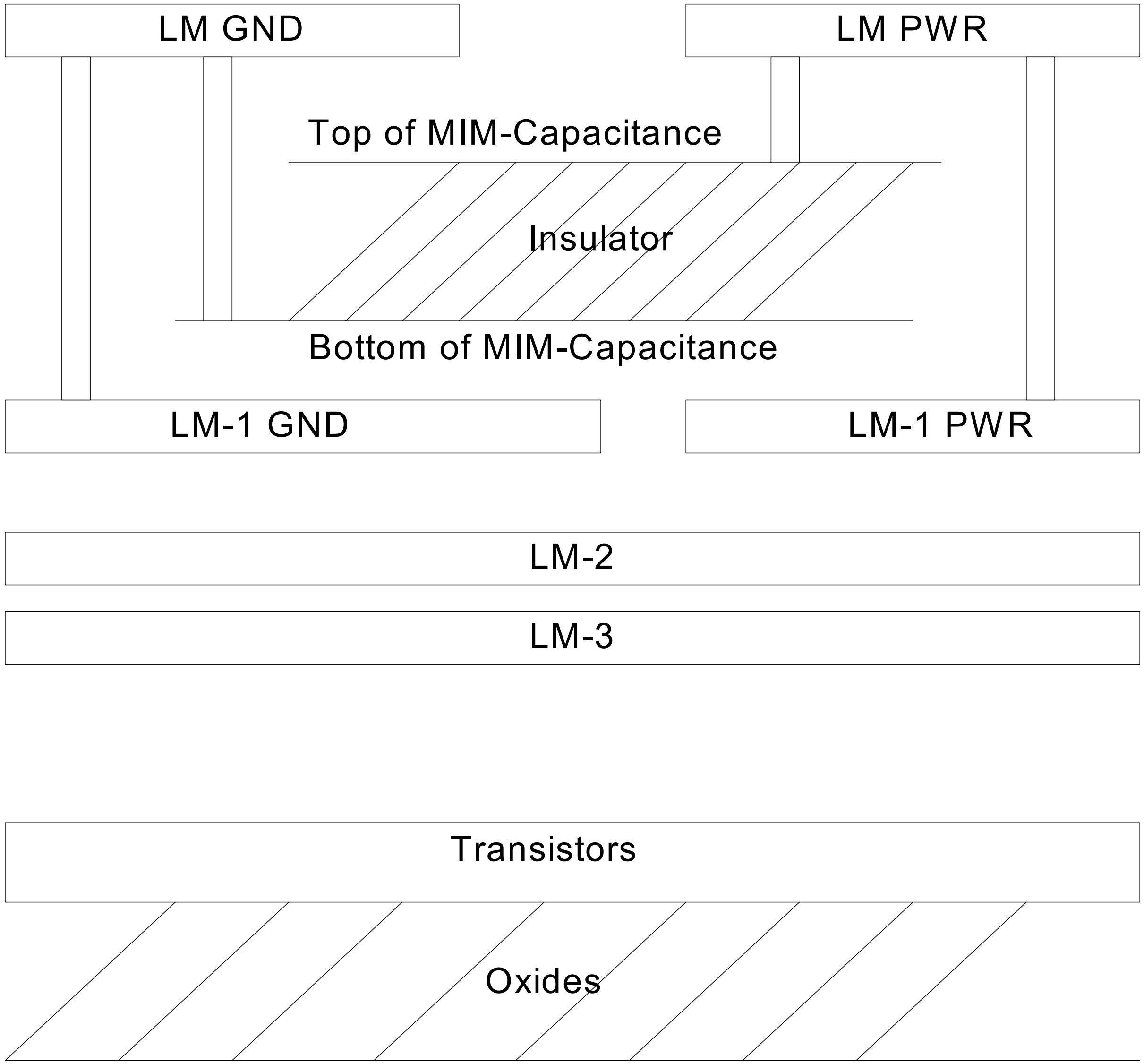
# Generic Cross sectional view of Process-stack



**MIM DECAP is located below last thick metal (between LM & LM-1)**

**Vias are used to make contacts from LM to top and bottom of MIM DECAP**

**Top MIM layer is cut out to allow vias from LM GND to bottom MIM layer**

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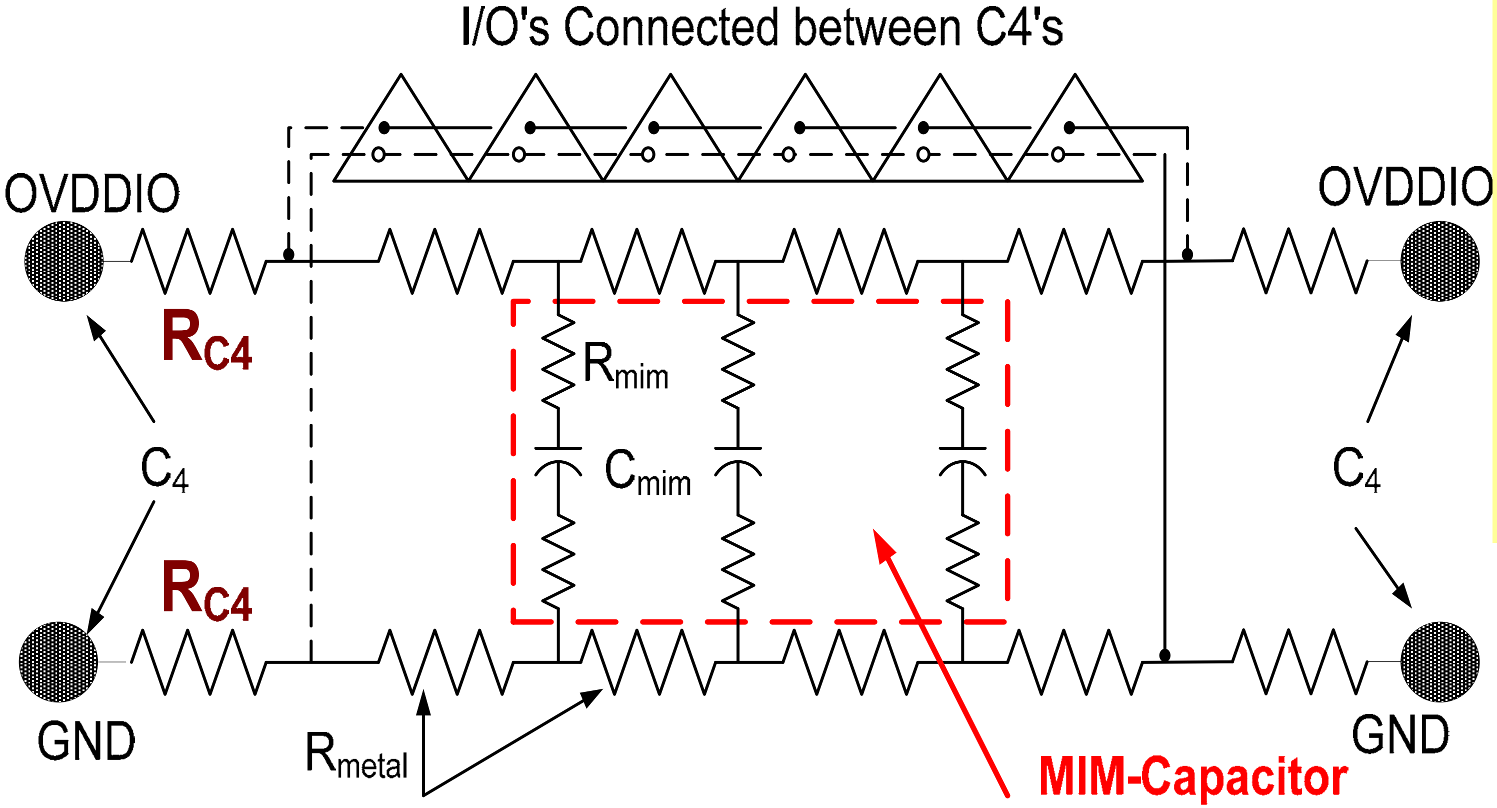
# Circuit representation of On-die High-K MIM DECAP

## for Physical implementation-1



**On-die High-K MIM DECAP modules are connected to IOs at an effective Pitch dictated by PWR/GND C4 bumps**

**$R_{c4}$ ➔$R_{metal}$ + PWR/GND Resistance of C4's**

**Electrical parameters of interest are**

**$R_{mim}$ ➔ MIM plate resistance + Via Resistance [50 Ω/sq]**

**$C_{mim}$ ➔ MIM Capacitance = Capacitance Per unit area (fF/μm$^2$)*Area(μm$^2$)**

**$R_{metal}$ ➔Metal resistance connecting IOs to PWR/GND C4's**

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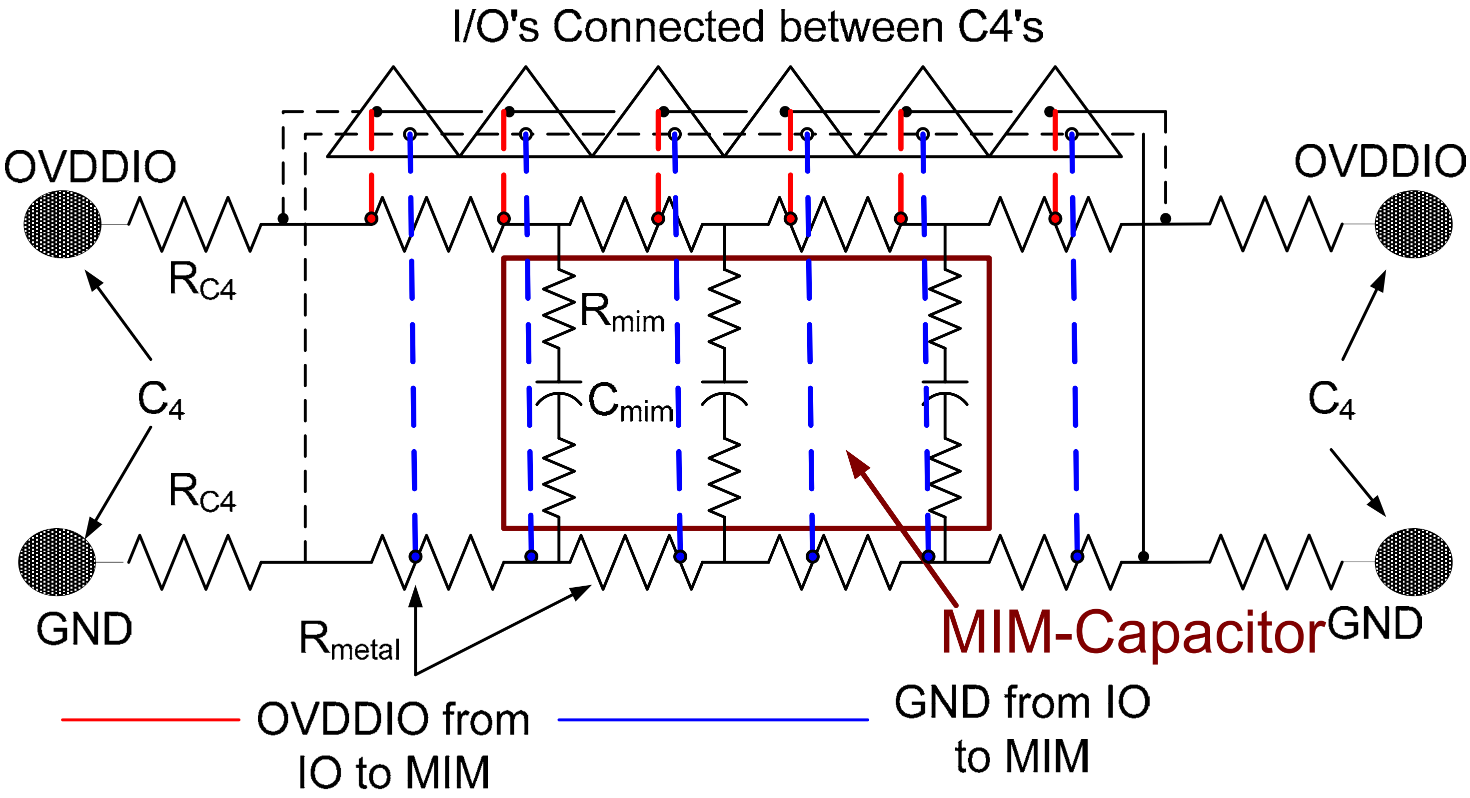
# Distributed Circuit Model of On-die High-K MIM DECAP

## (for improved Physical implementation-2)



**Each IO's PWR/GND terminal is connected to On-die High-K MIM DECAP using an extra last metal line**

**⇒ Improved $R_{metal}$ and $R_{mim}$**

- **On-die High-K MIM DECAP Module is divided in small subsections**
- **Next, each subsection is modeled as a distributed R-C network**
- **Vias from metal to plates have significant resistances**

  **- Must be modeled carefully**

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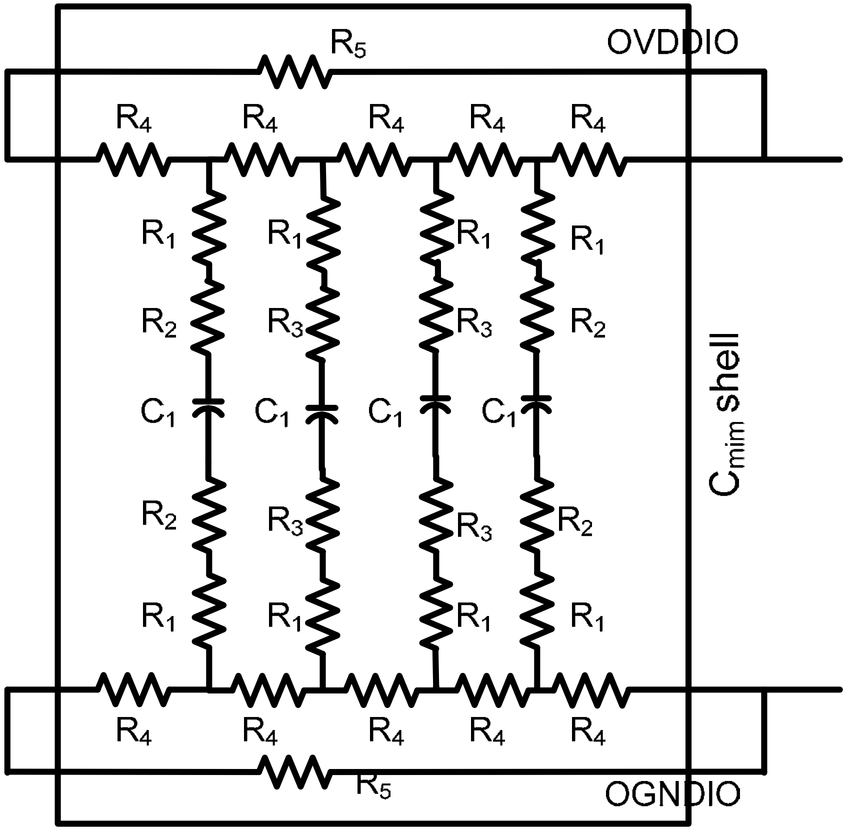
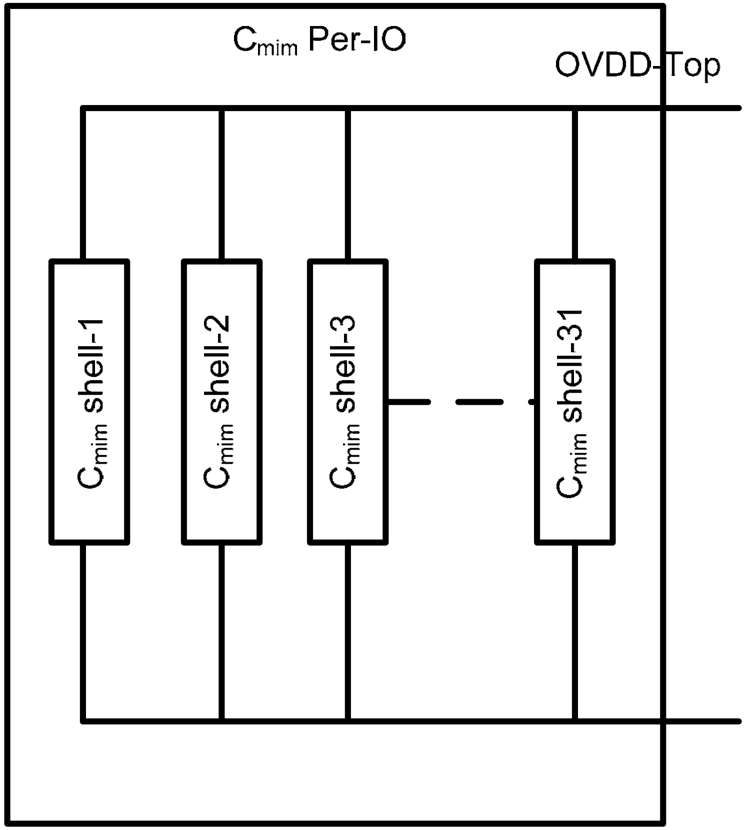
# Distributed Circuit Model of On-Die High-K MIM DECAP

- **Appropriate strapping of DIE-layer is required to make On-die High-K MIM DECAP available to all IOs**





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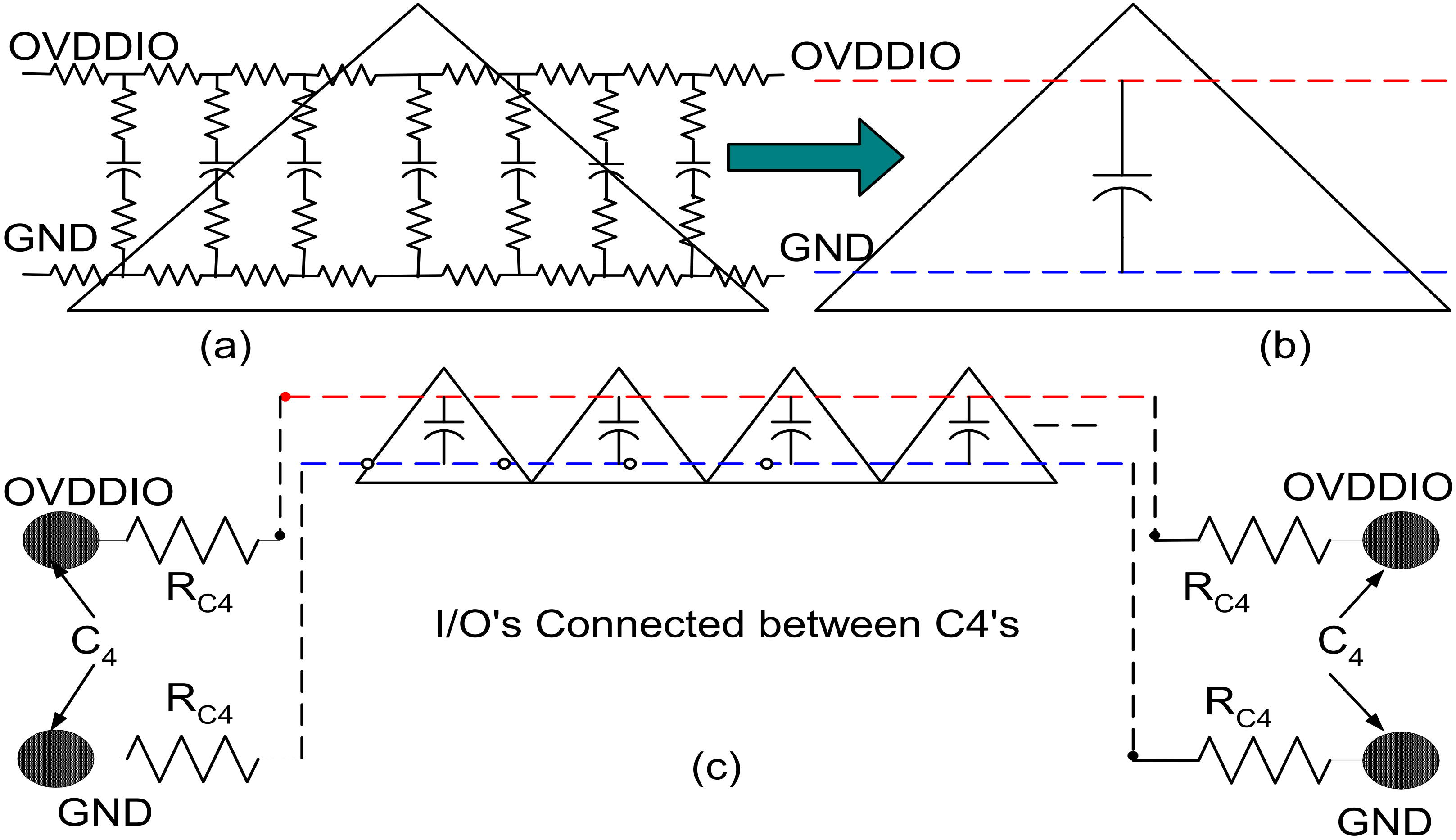
# Circuit representation of On-die High-K MIM DECAP

## (for further improved Physical implementation-3)

- By reducing Via-MIM spacing between PWR-GND plates and
- By Custom integration of On-die high-K MIM DECAP into IO itself – as in Fig (a)

$\Rightarrow$ **Electrical performance → Ideal capacitor**



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LM to LM-1 power grid for Several (6/7) I/O ckts

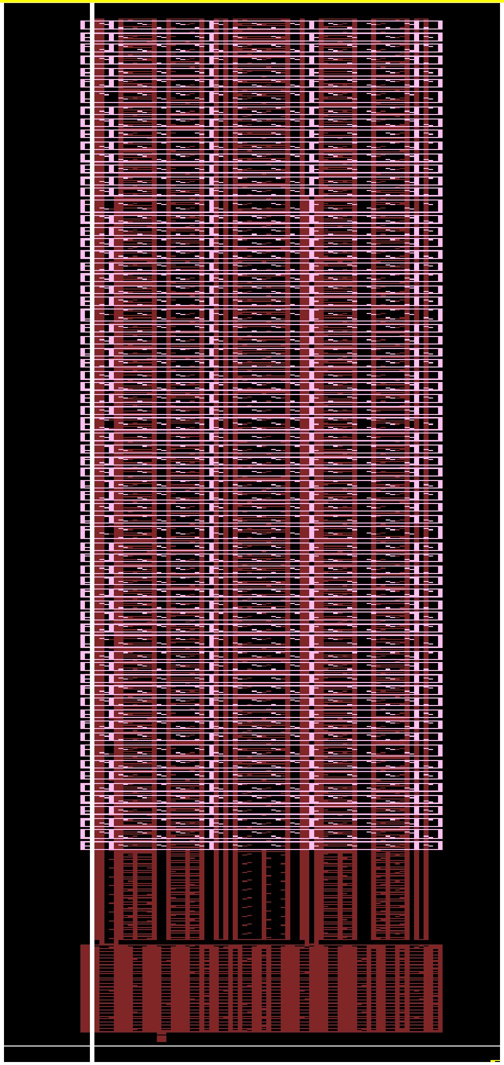
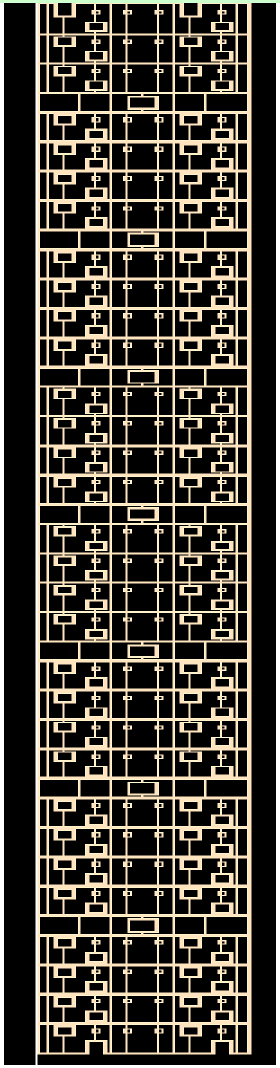
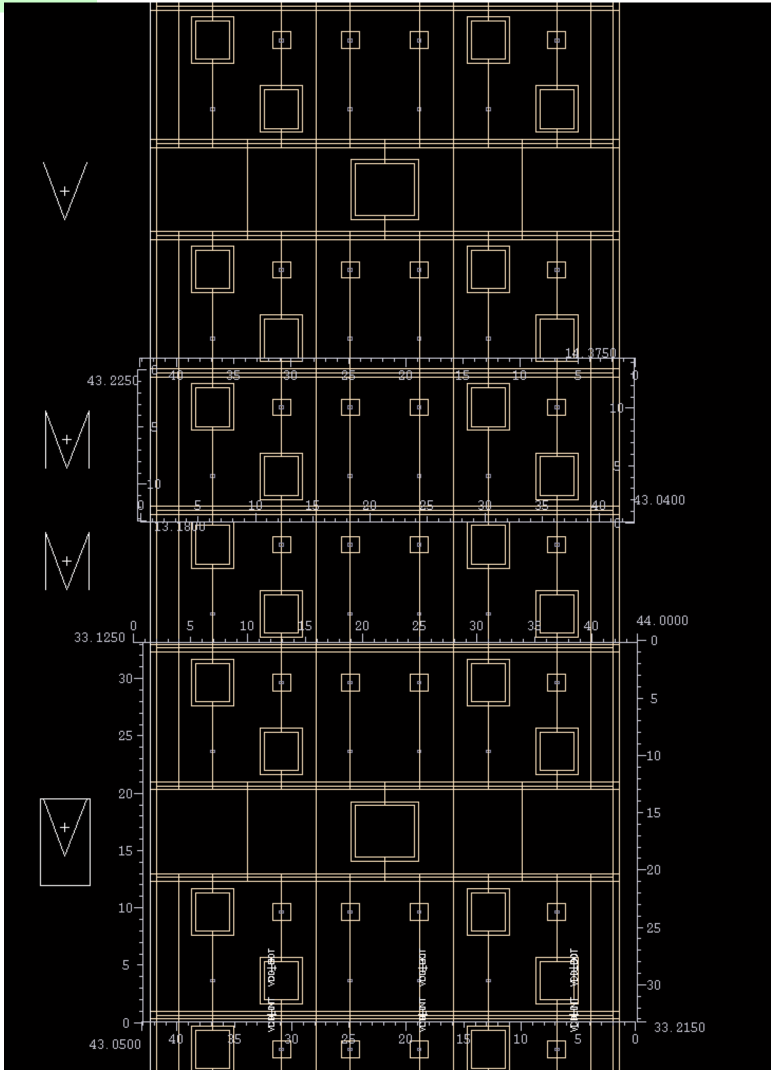


Image of MIM for one IO ckt



**MIM-CAP section for Distributed Model**



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**All figures shown here are not to the scale**

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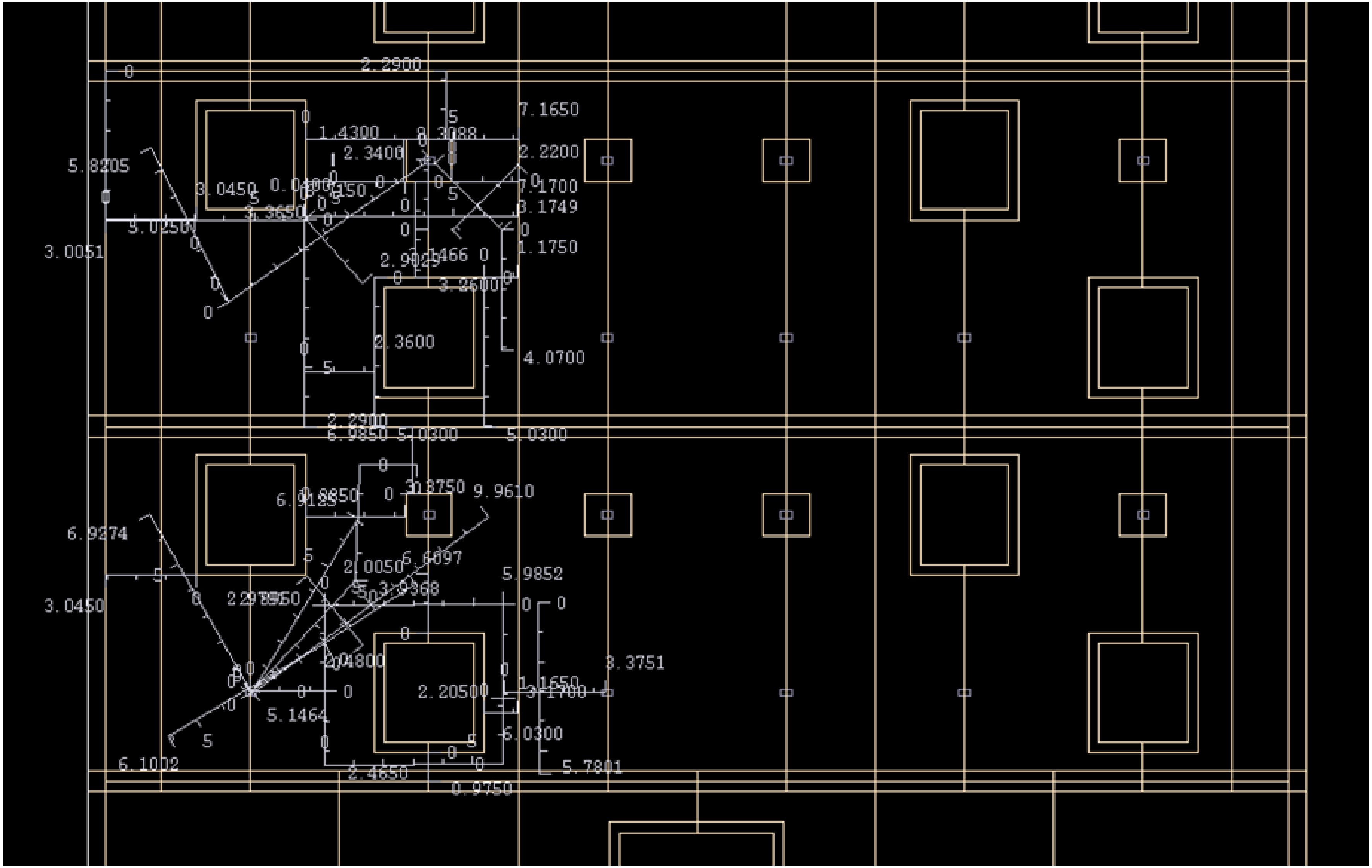
# Estimating R and C of MIM-CAP for developing a Distributed CKT Model



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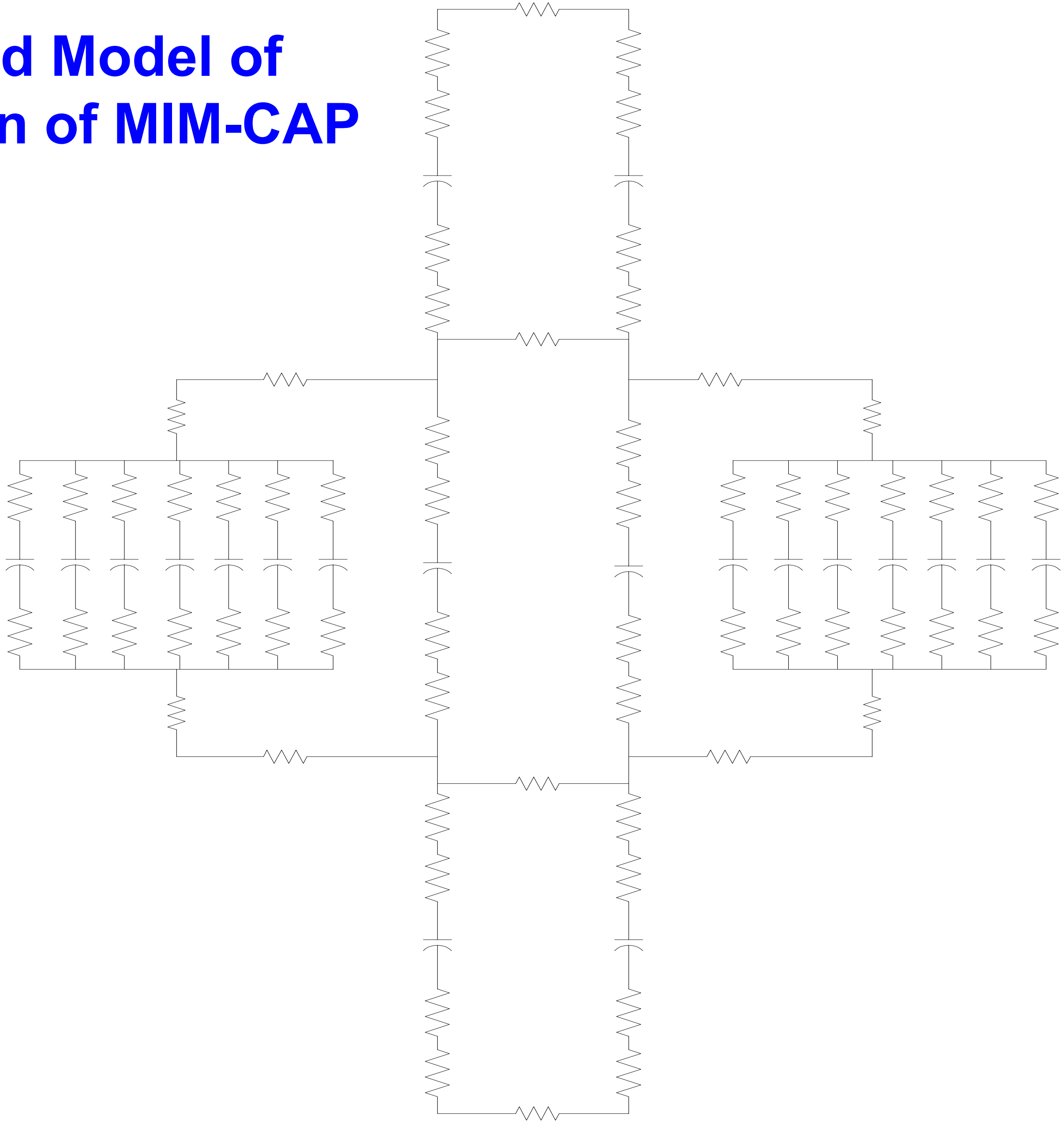
# Distributed Model of ‘M’ section of MIM-CAP



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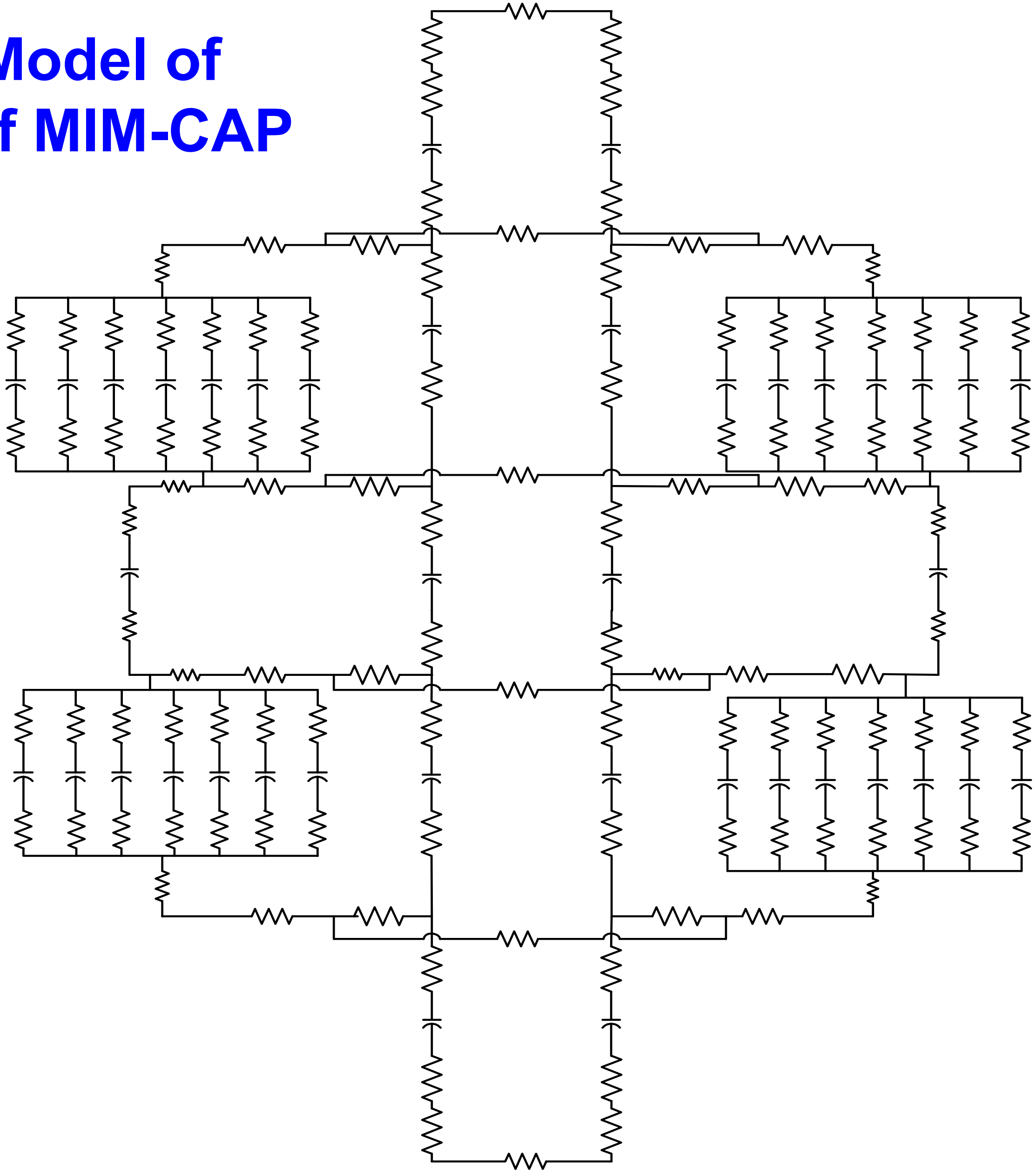
# Distributed Model of ‘V’ section of MIM-CAP



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# Distributed Circuit Model Per-IO

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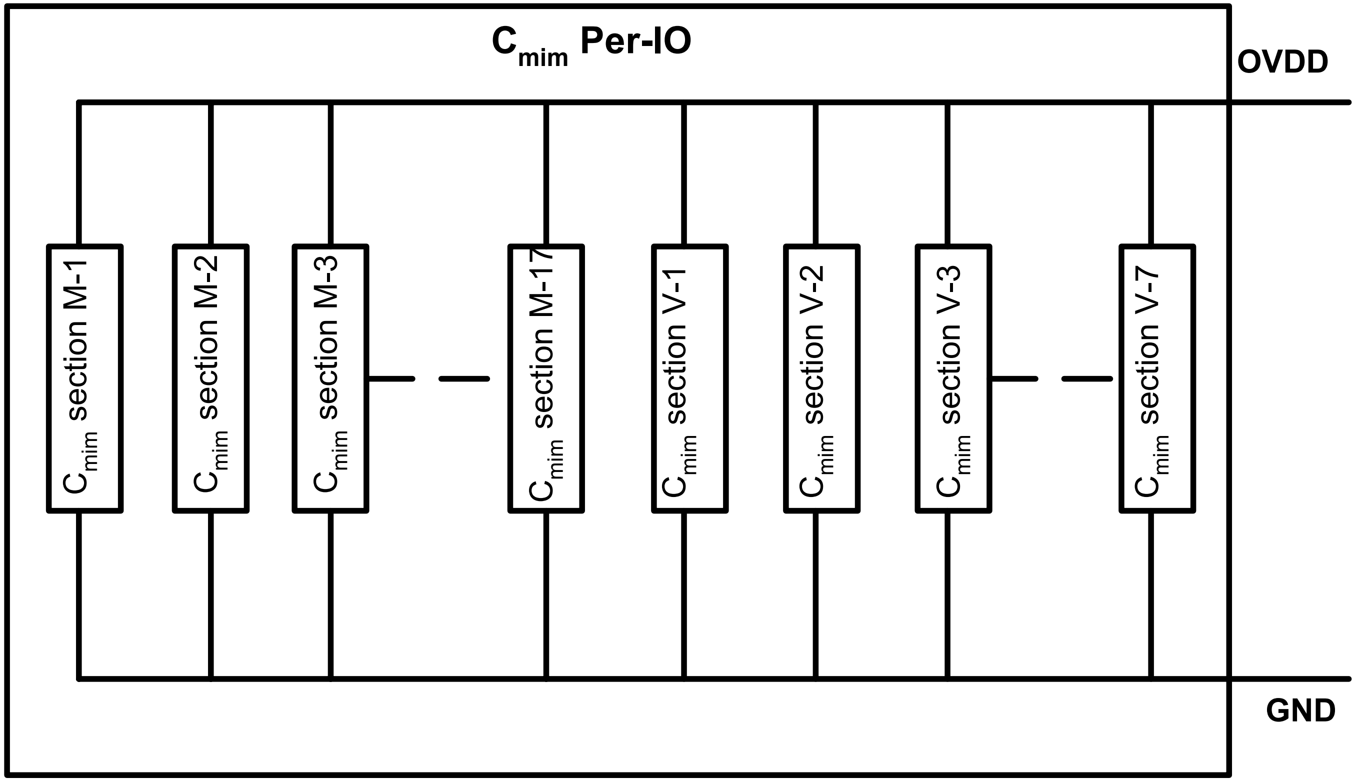

**7 'V' and 17 'M' Section in Parallel Per IO**

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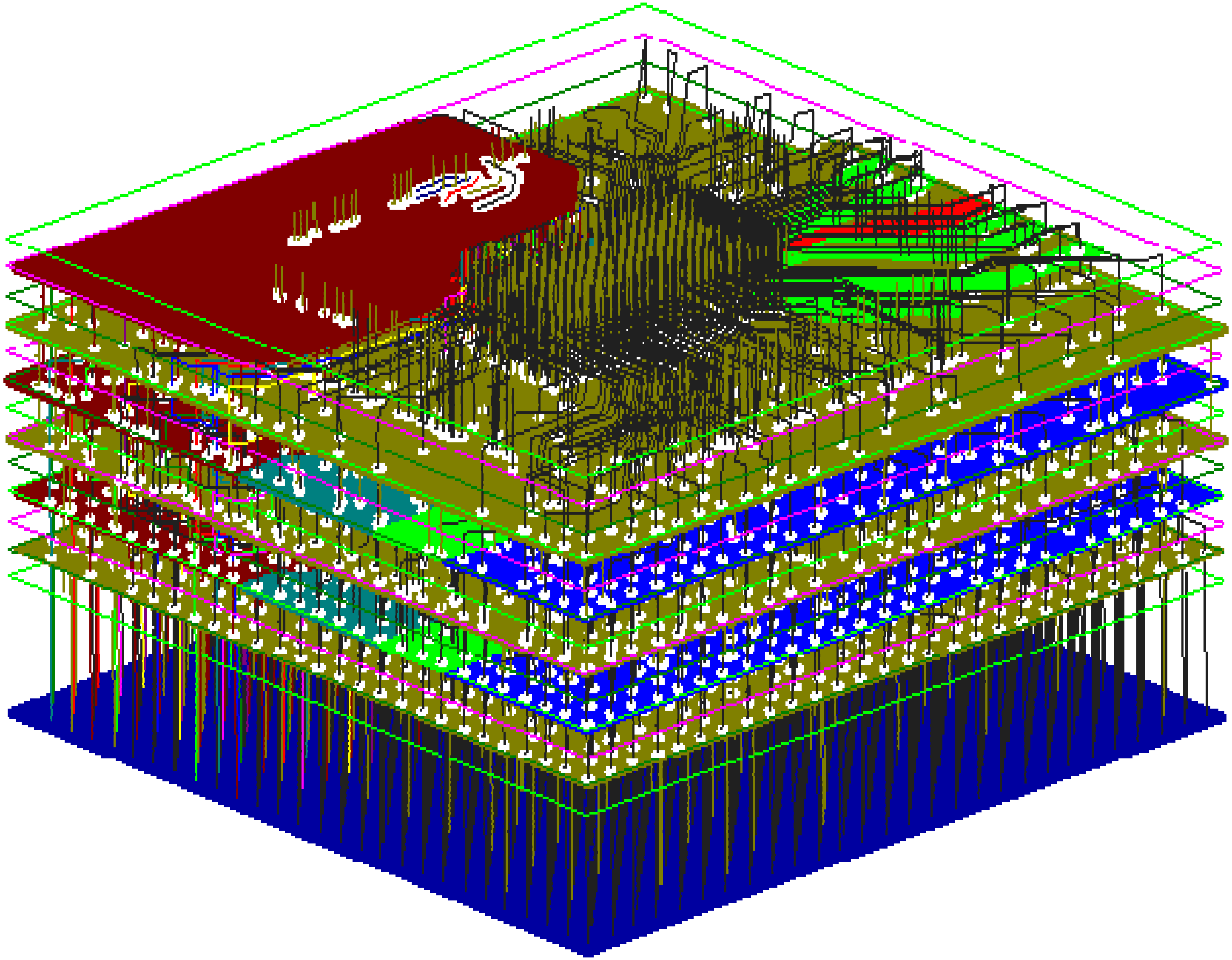
# 12 Layer Ceramic FCBGA Package used for SSN study



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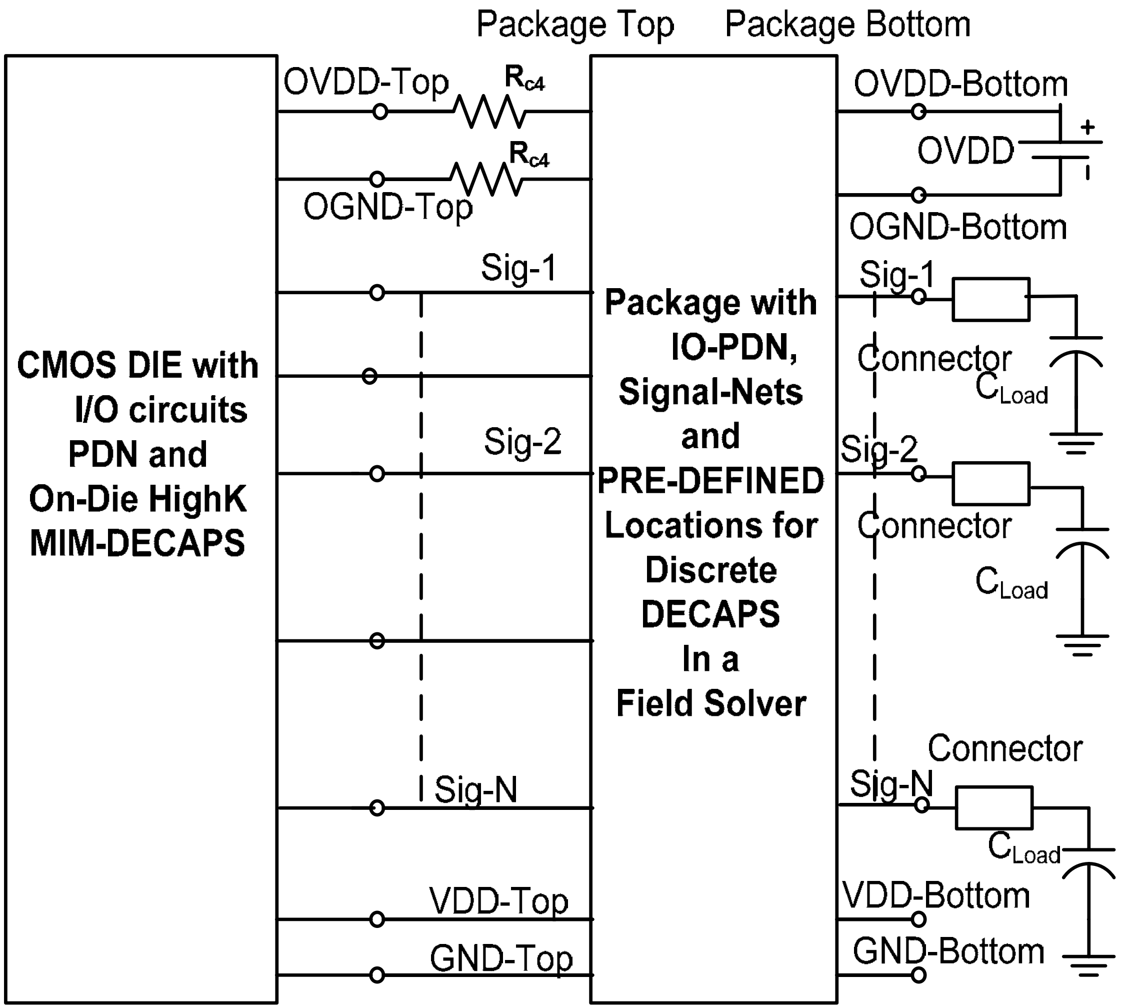
# Block diagram model used for Time domain and Frequency domain simulation and analysis to study effect of On-die High-K MIM DECAP



Both PDN and IO Signal nets are considered to account all inductive and capacitive coupling of the Package imported in the EM Field solver

- **SPEED2000 and**
- **PowerSI** from Sigrity

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# DDR2/DDR3 System Level Modeling and Simulation:

- Detailed Package Model inside the Field Solver

(Speed2K & PowerSI with built in SPICE Circuit simulator)

- Simultaneous switching of 62 out of 64 I/Os
- Full strength 18 Ω IBIS(3.2) model of DDR2/DDR3 IOs
- DDR2/DDR3 data load connector model
- Off-chip Capacitances representing Receivers
- On-Die High-K MIM DECAPS as
  - First as Lumped Model, and
  - Next as Distributed models (for physical implementation 1-3)

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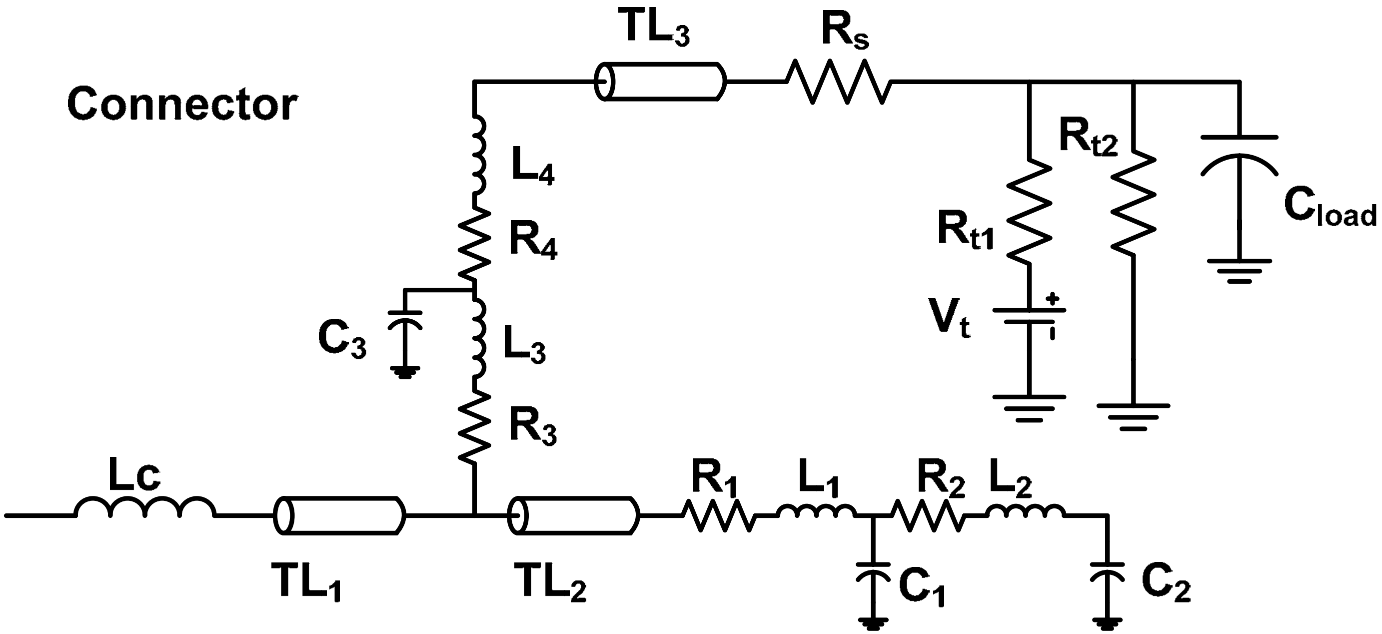
# DDR2 data load Connector circuit



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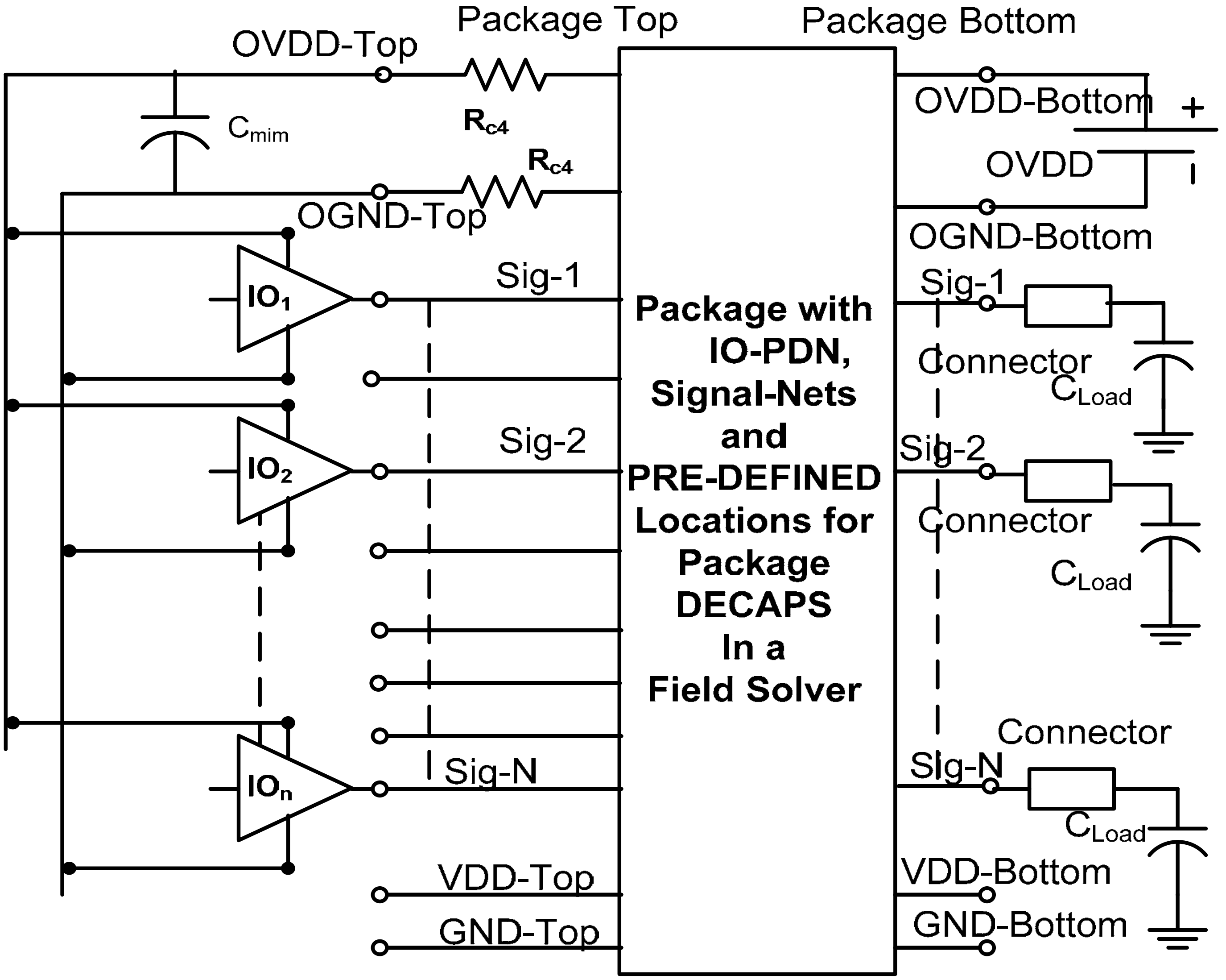
# SSN simulation setup considering Lumped model of On-die High-K MIM DECAP



**Package with IO-PDN, Signal-Nets and PRE-DEFINED Locations for Package DECAPS In a Field Solver**

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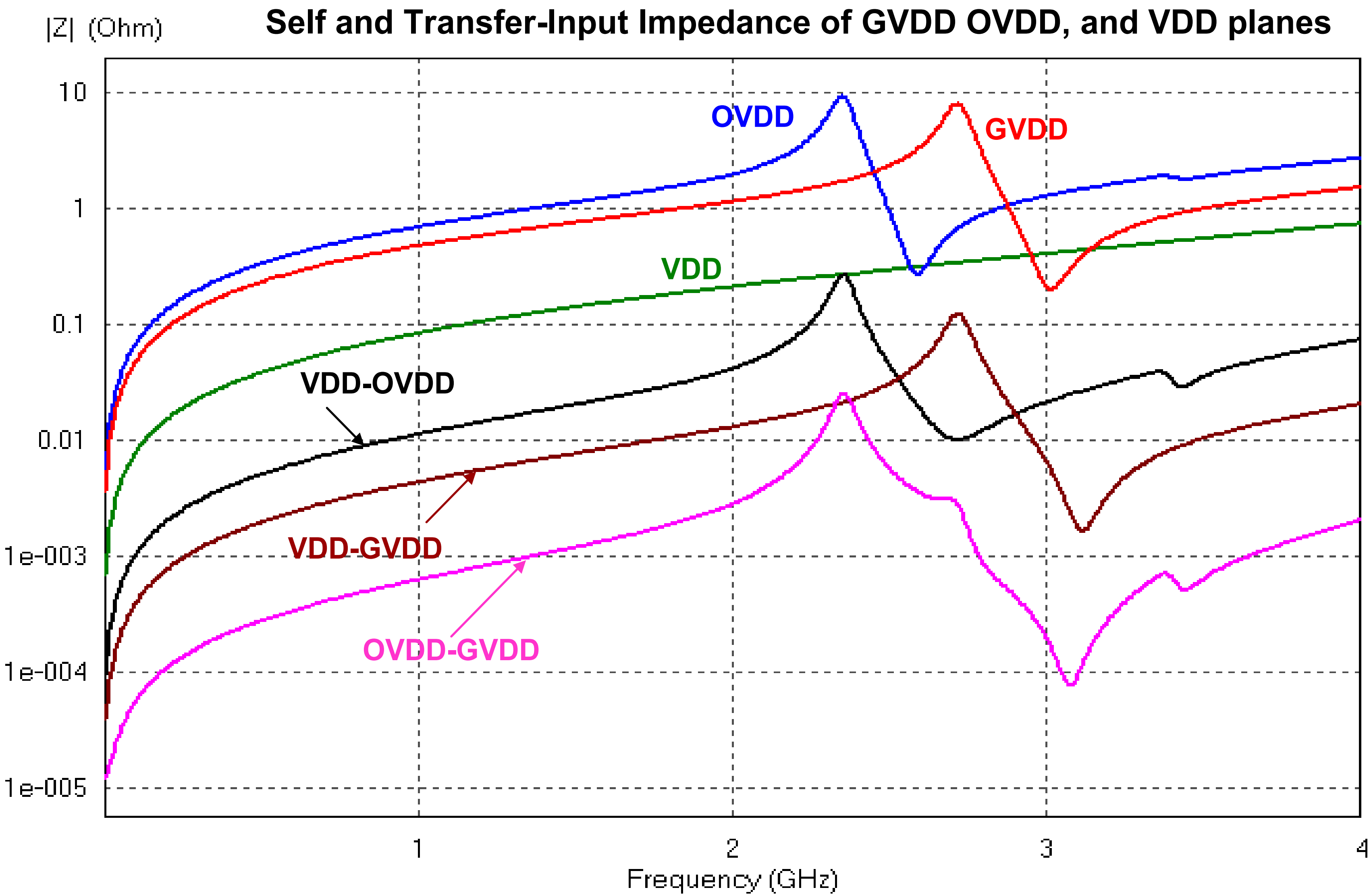
# Self and transfer Input Impedance of PDNs



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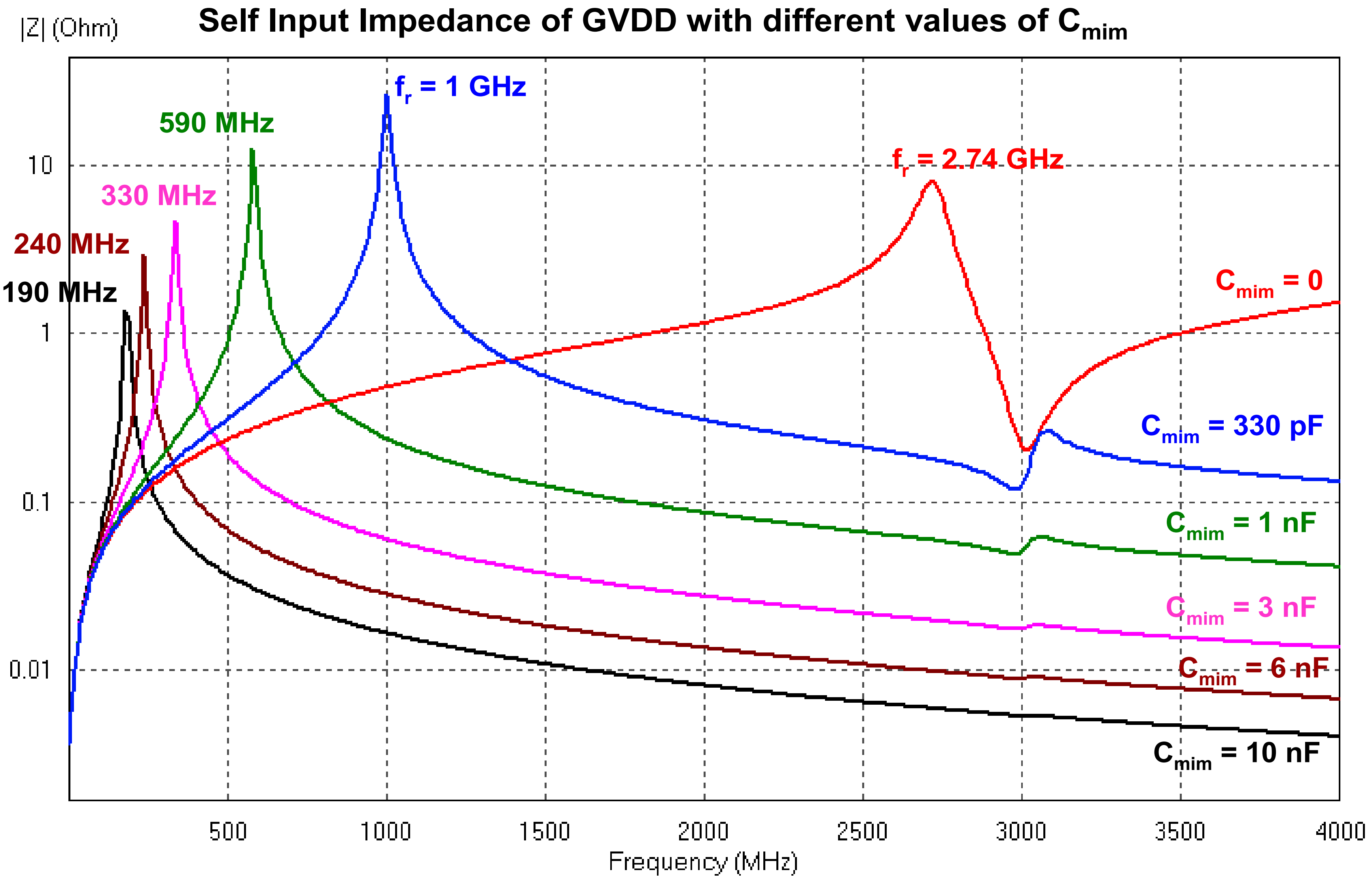
# Self Input Impedance of IO-PDN with different values of On-chip DECAPS



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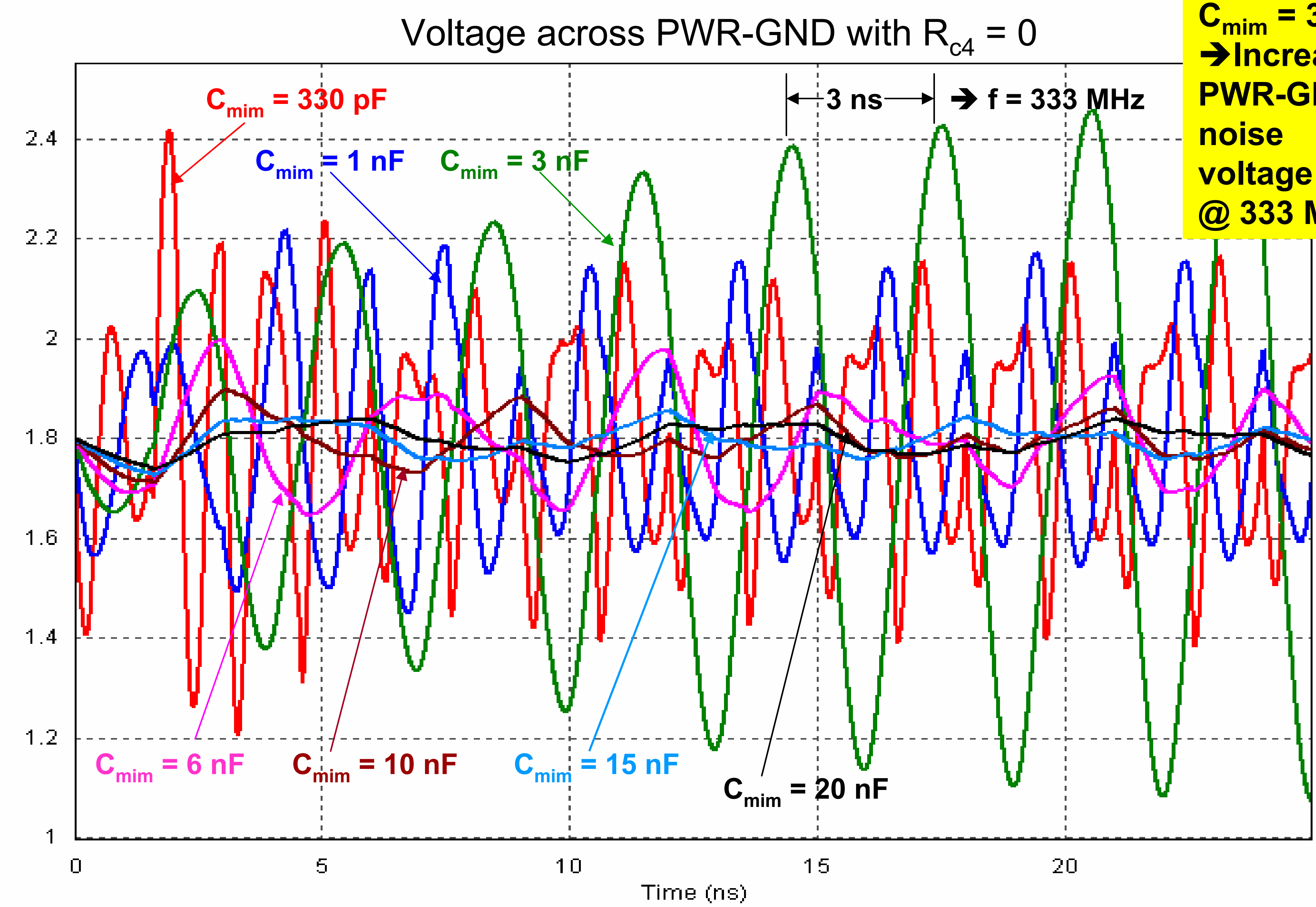
# PWR-GND Noise Voltage vs. DIE-DECAP for DDR667

**$C_{mim}$ = 3 nF → Increasing PWR-GND noise voltage @ 333 MHz**



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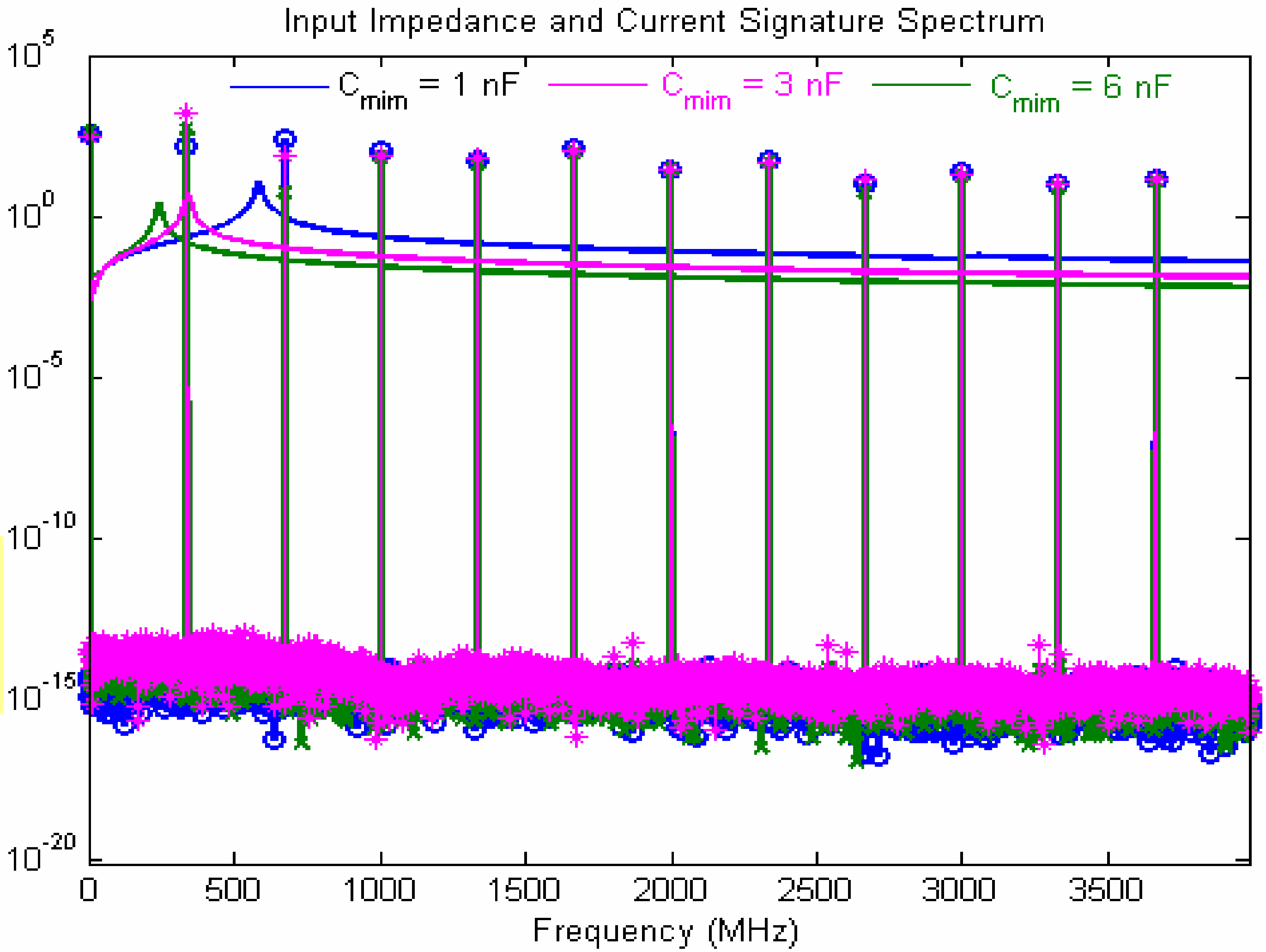
# PWR-GND Input impedances and Frequency Spectrum (FFT) of Switching current through PWR-GND

**Input impedance Peak is shifted @333 MHz due to $C_{mim}$ = 3 nF**

**FFT of switching Current through PWR-GND ➔ 333 MHz comp. coincides with Impedance peak**

$f_0$ = 333 MHz, and
$C_{mim}$ = 3 nF
➔ $L_{eff}$ = 76 pH

**Simulated PWR-GND loop inductance correlates**



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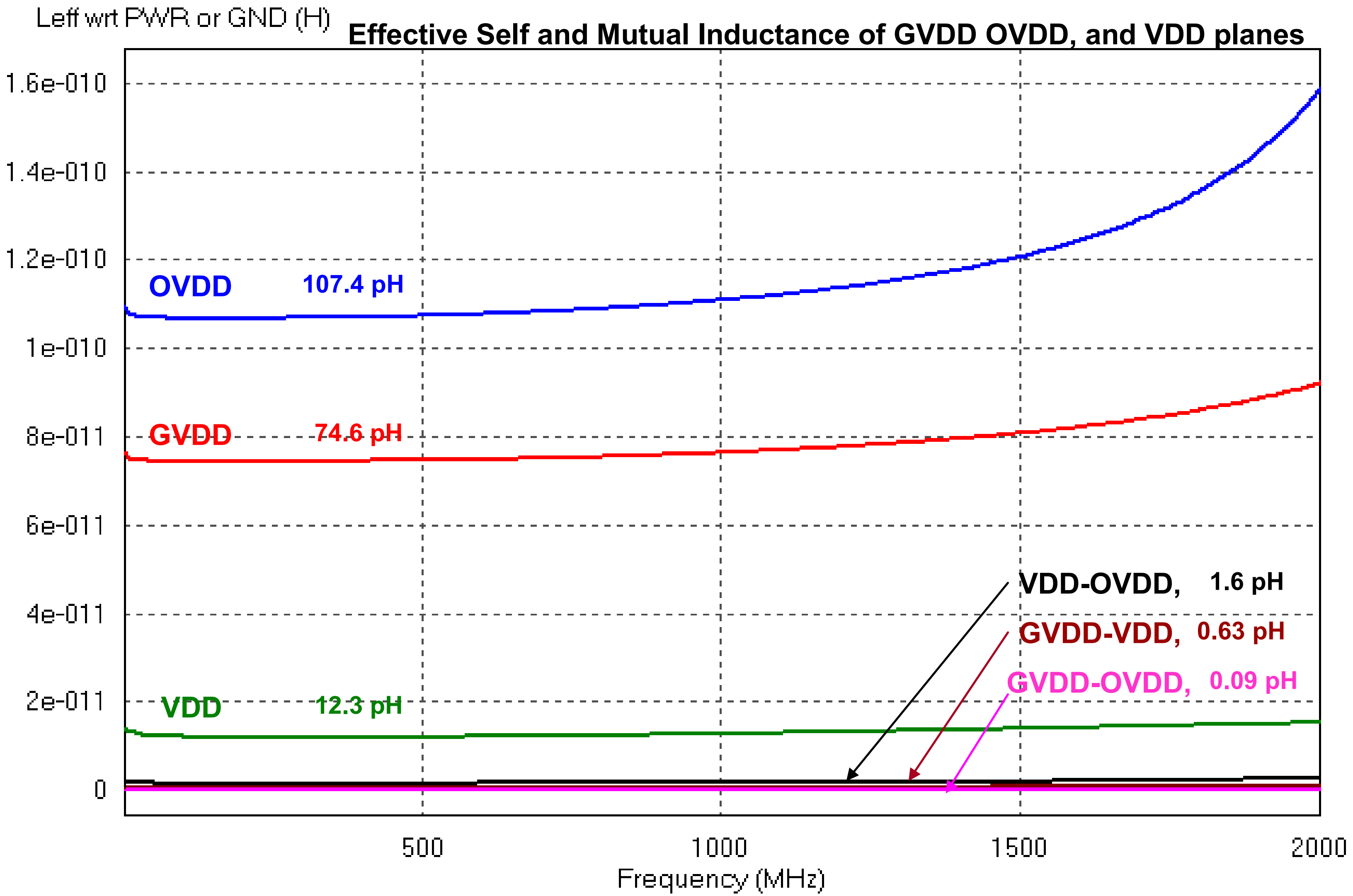
# Effective Loop Inductances of Package PDNs



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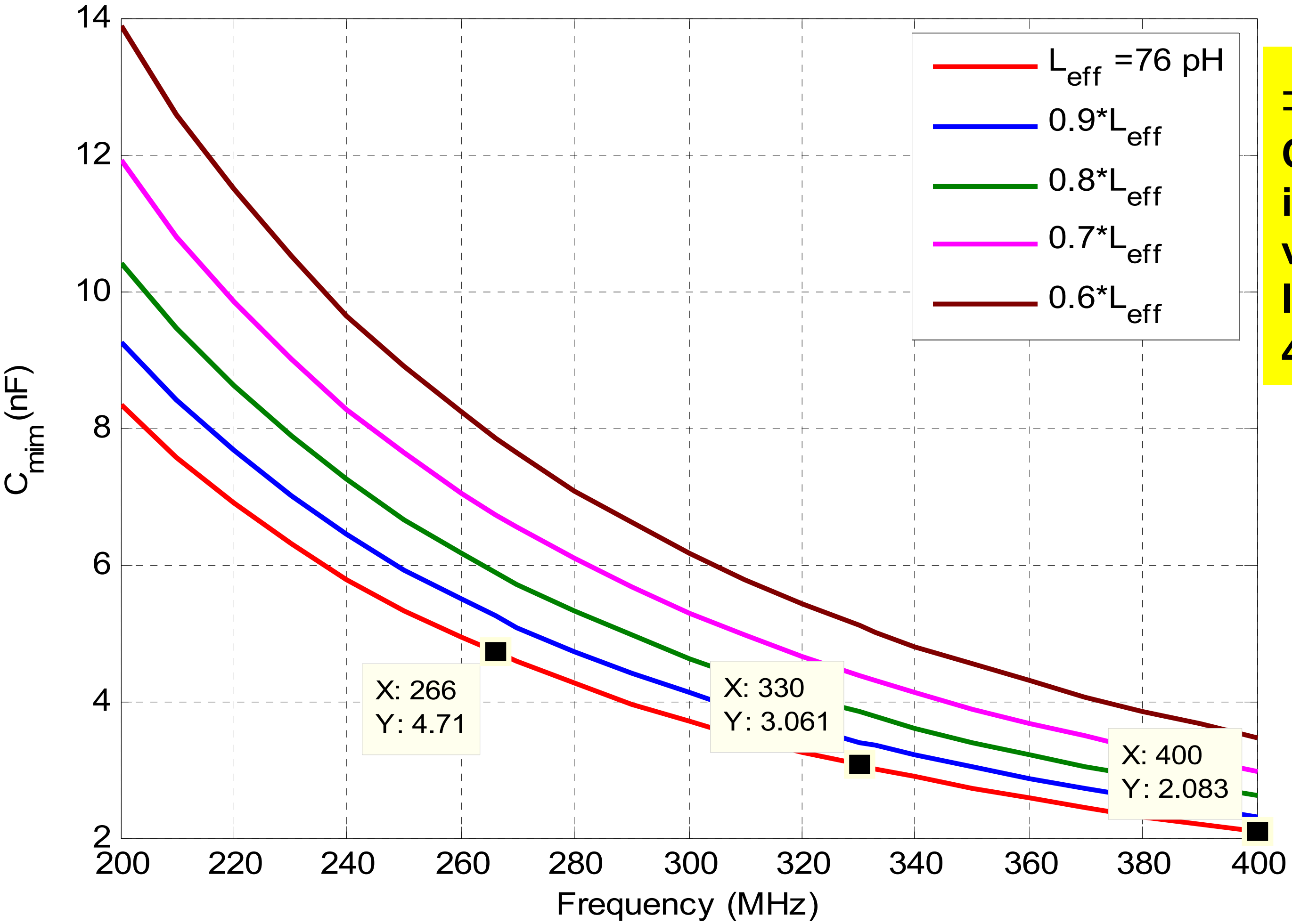
# $C_{die/mim}$ vs. Clock frequency for a given $L_{eff}$ of Package PDN to avoid increasing PWR-GND noise voltage



**⇒ for $L_{eff}$ = 76 pH, $C_{mim}$ = 2 nF generates increased noise voltage with DDR800 IOs switching at 400 MHz.**

**X-axis label 'Frequency (MHz)**

➔Half of the clock frequency

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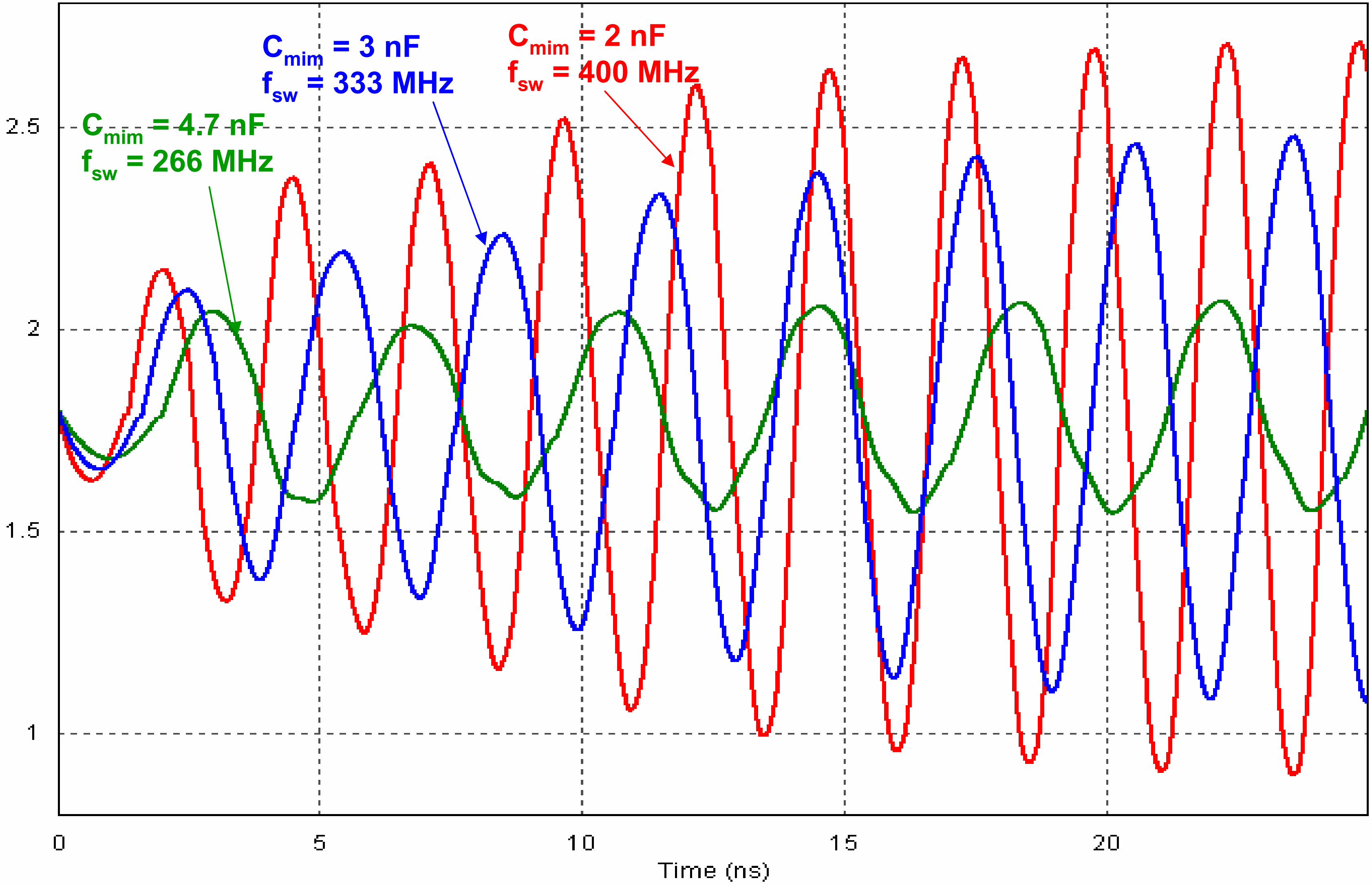
# Voltage across PWR-GND



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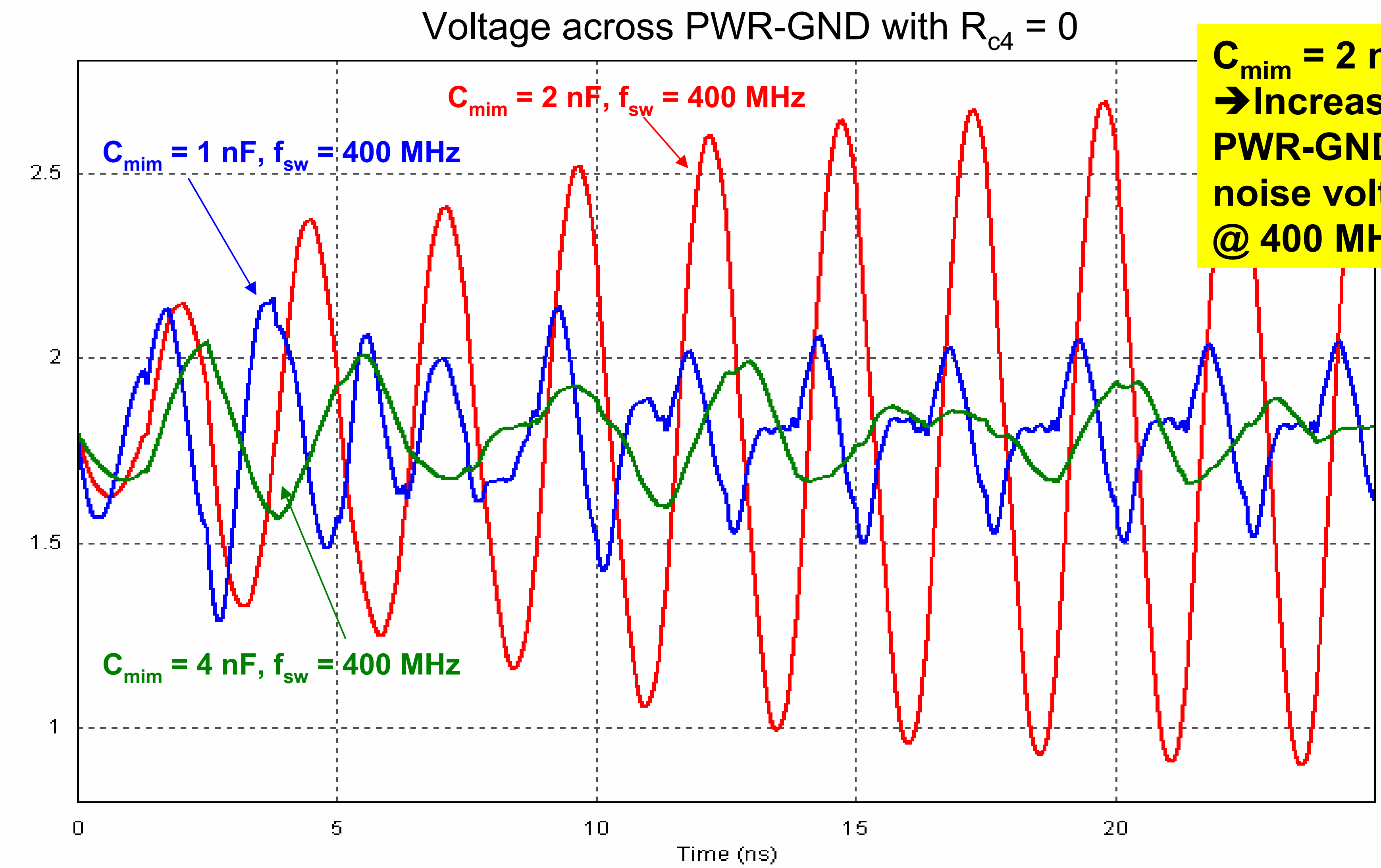
# Power-ground noise voltages for DDR800-IOs switching @ 400 MHz for $C_{die/mim}$ = 1 nF, 2 nF and 4 nF



**$C_{mim}$ = 2 nF**
**→Increasing PWR-GND noise voltage @ 400 MHz**

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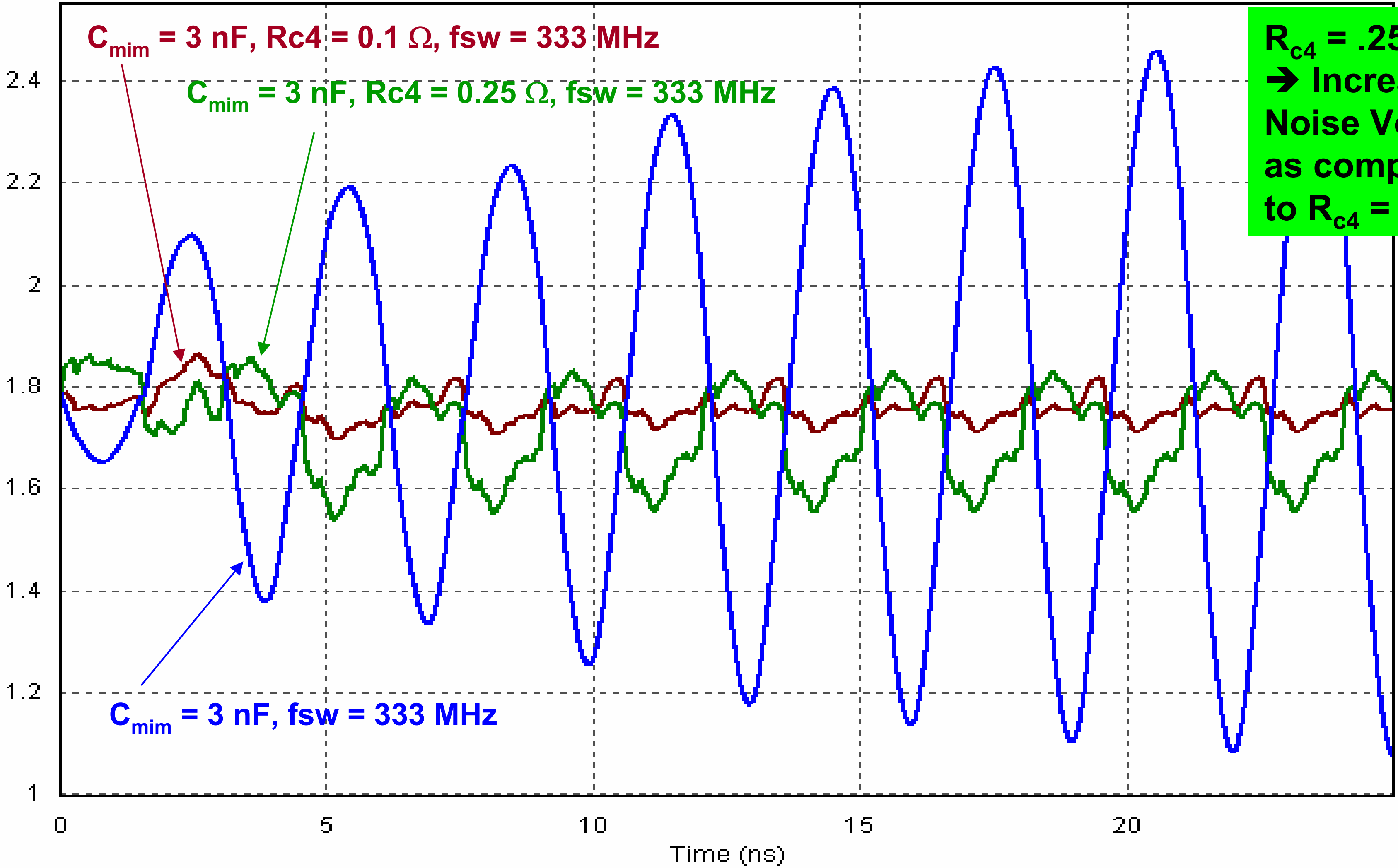
# Voltage across PWR-GND



**$R_{c4}$ = .25 Ω → Increased Noise Voltage as compared to $R_{c4}$ = 0.1Ω**

**Increasing noise voltage for $C_{mim}$'s generating resonance can be prevented by incorporating resistance $R_{c4}$ of small value in PWR-GND path of IO-PDN of PKG**

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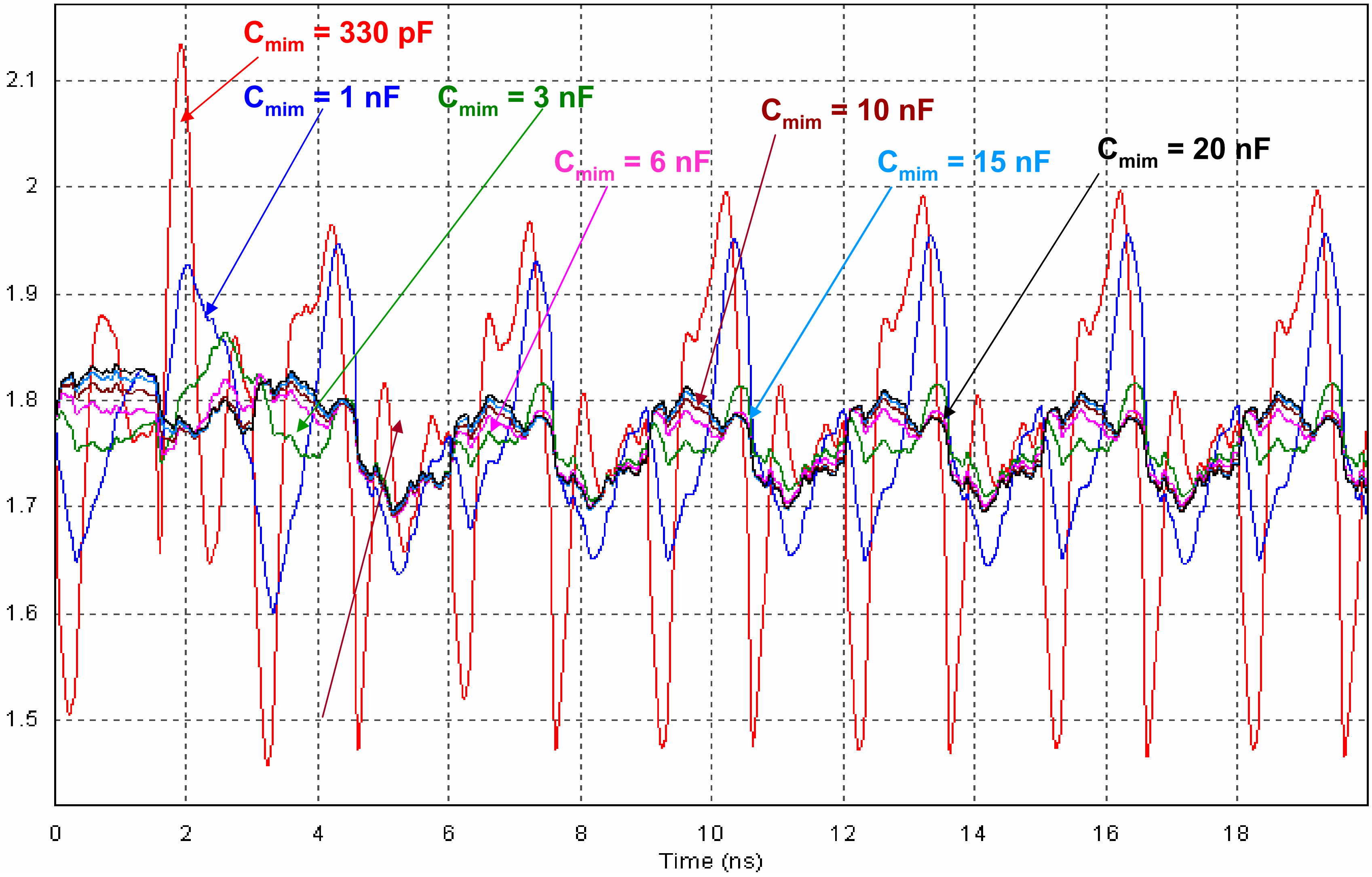
# Voltage across PWR-GND with $R_{c4}$ = 0.1 Ω



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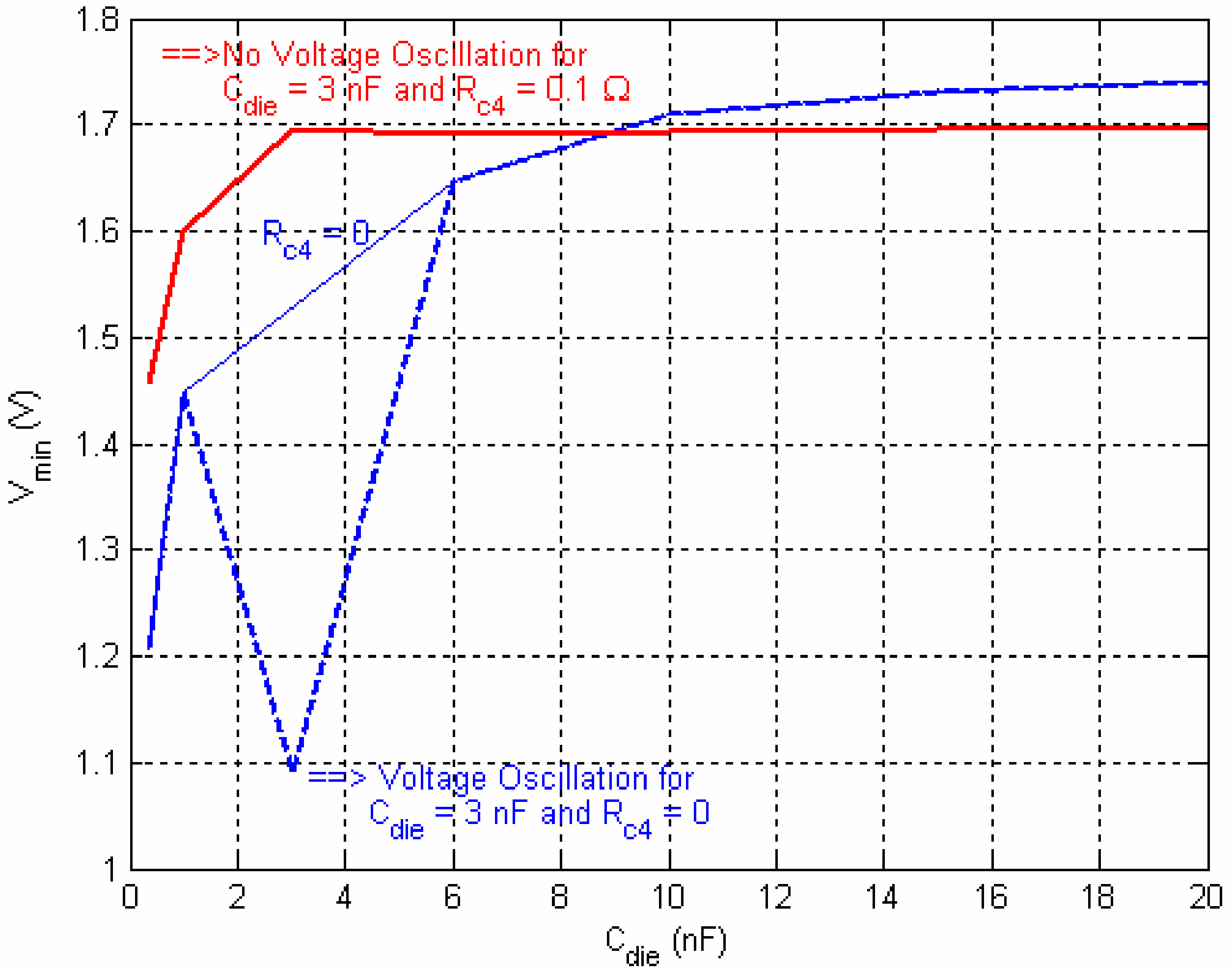
# Peak Noise Voltage across PWR-GND of DDR667-IOs vs. DIE-Capacitance ($C_{die}$).



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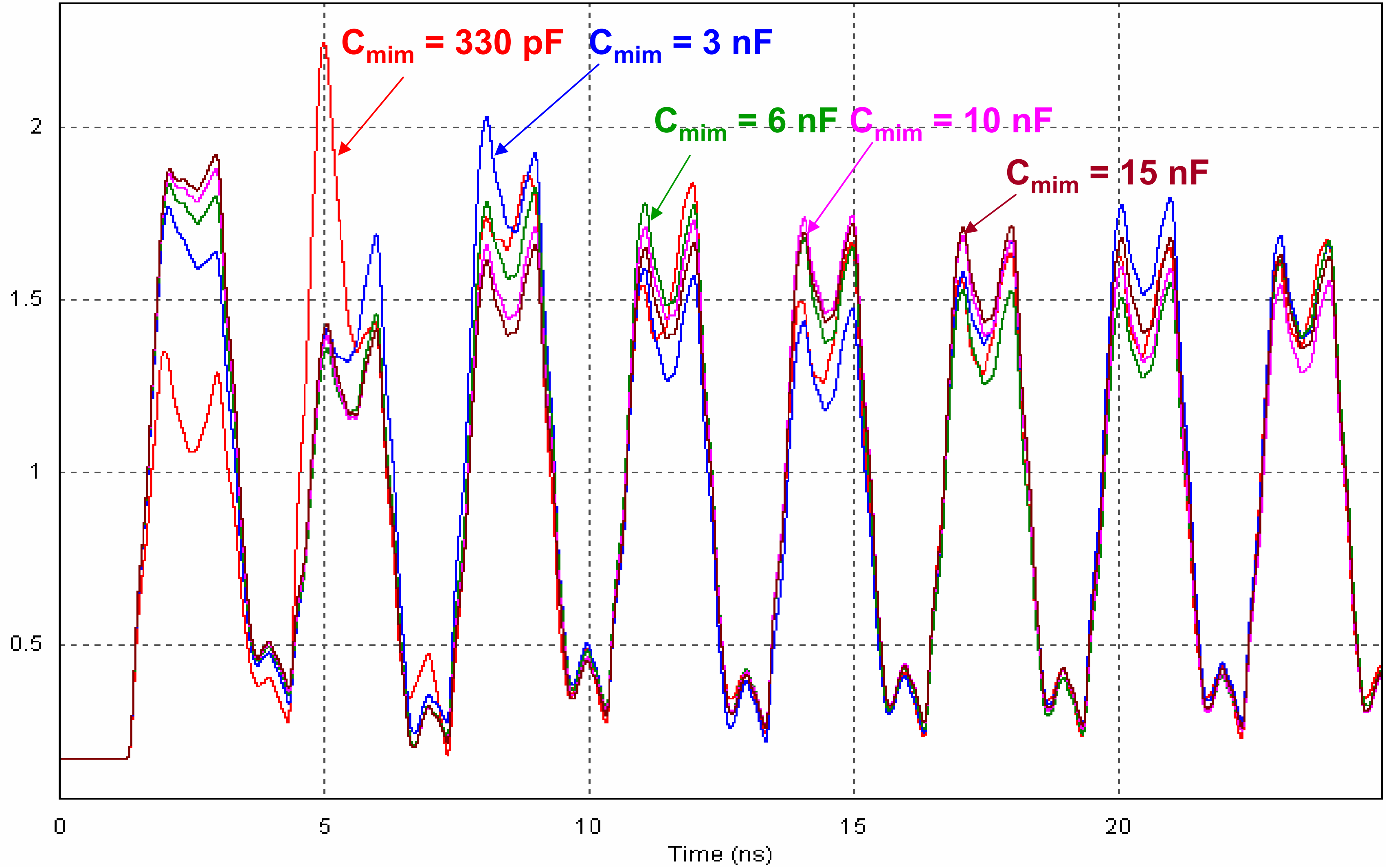
# Simulated voltages at a Receiver load of an actively switching IO with 62 DDR2-667-IOs switching simultaneously at 333 MHz, as 101010



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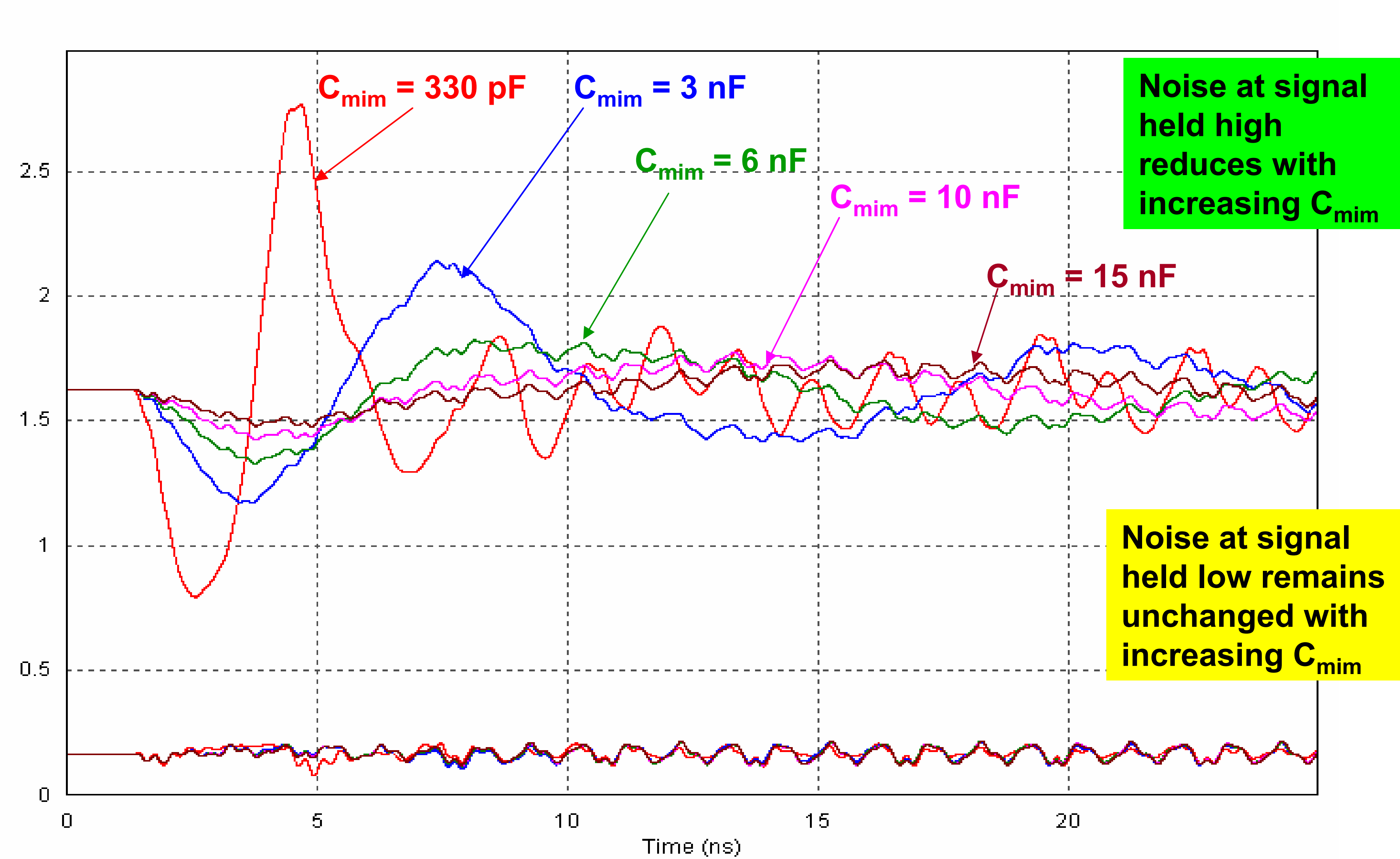
# Simulated voltages at a Receiver load of an actively switching IO with 62 DDR2-667-IOs switching simultaneously at 333 MHz, as 101010



Noise at signal held high reduces with increasing $C_{mim}$

Noise at signal held low remains unchanged with increasing $C_{mim}$

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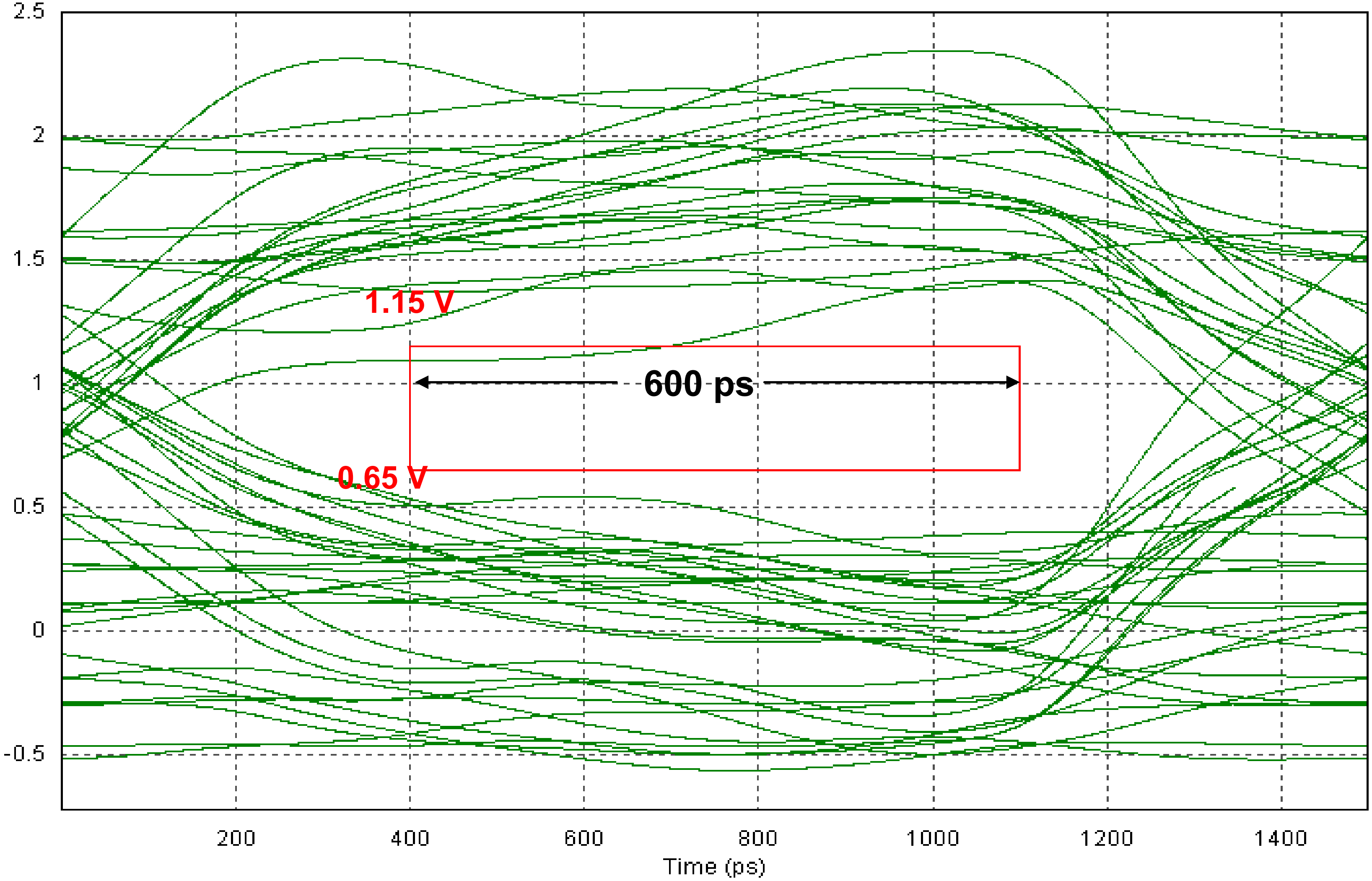
# EYE diagrams for switching output signal at the receiver end with $C_{mim}$ = 1nF and 64 DDR2 IOs switching simultaneously at 333 MHz



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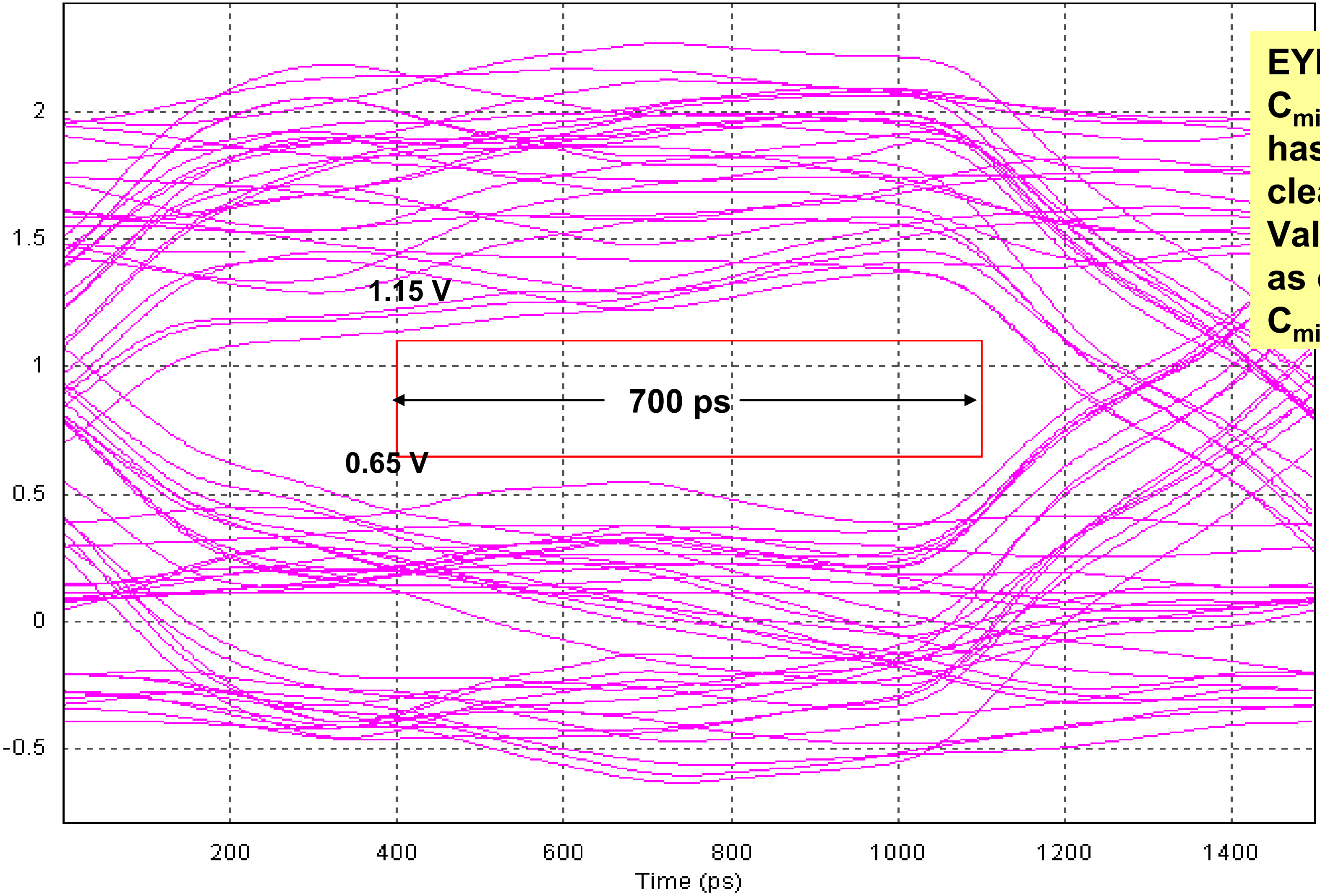
# EYE diagrams for switching output signal at the receiver end with $C_{mim}$ = 10nF and 64 DDR2 IOs switching simultaneously at 333 MHz



**EYE with $C_{mim}$ = 10 nF has wider and cleaner data Valid window as compared to $C_{mim}$ = 1 nF**

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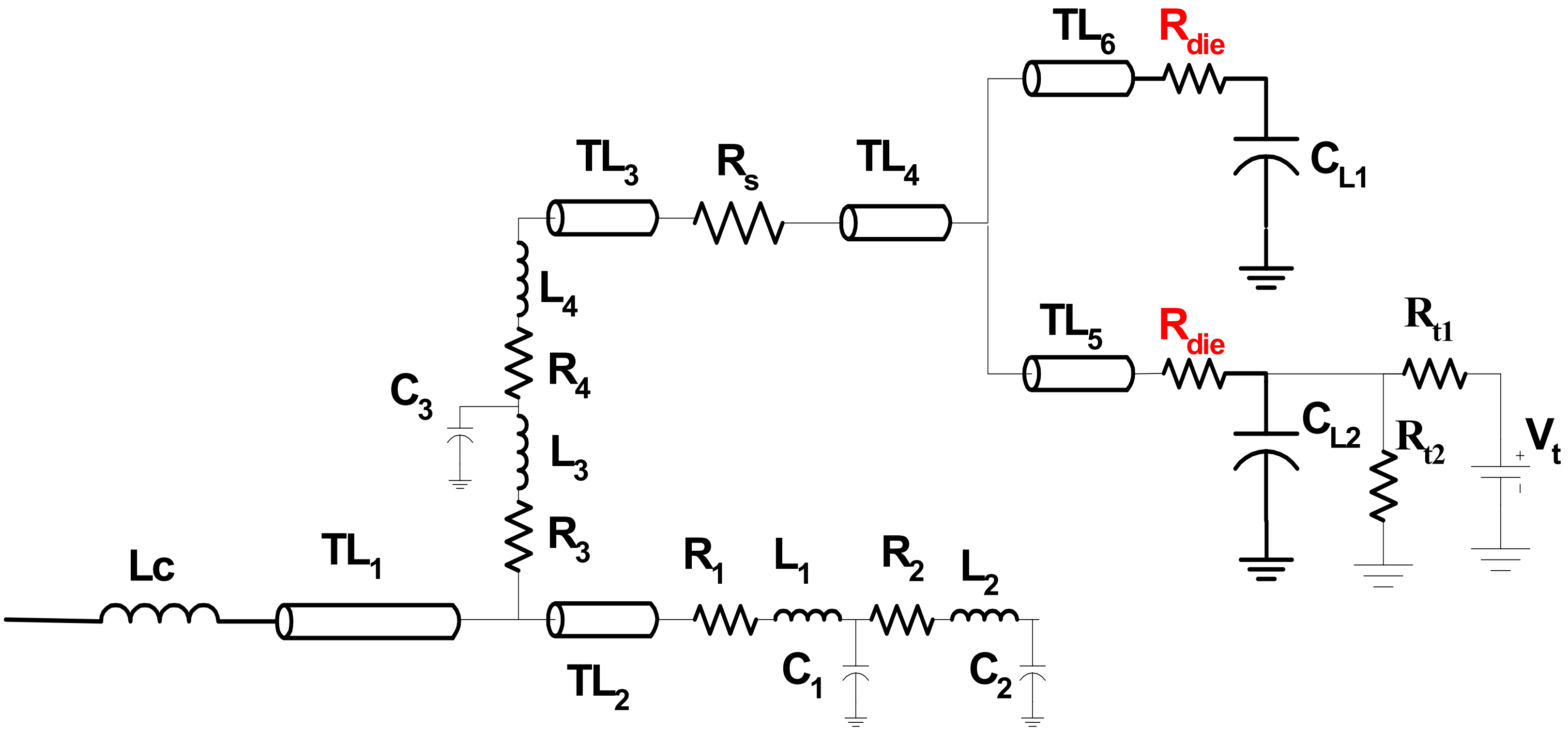
# Load-connector Model for DDR3



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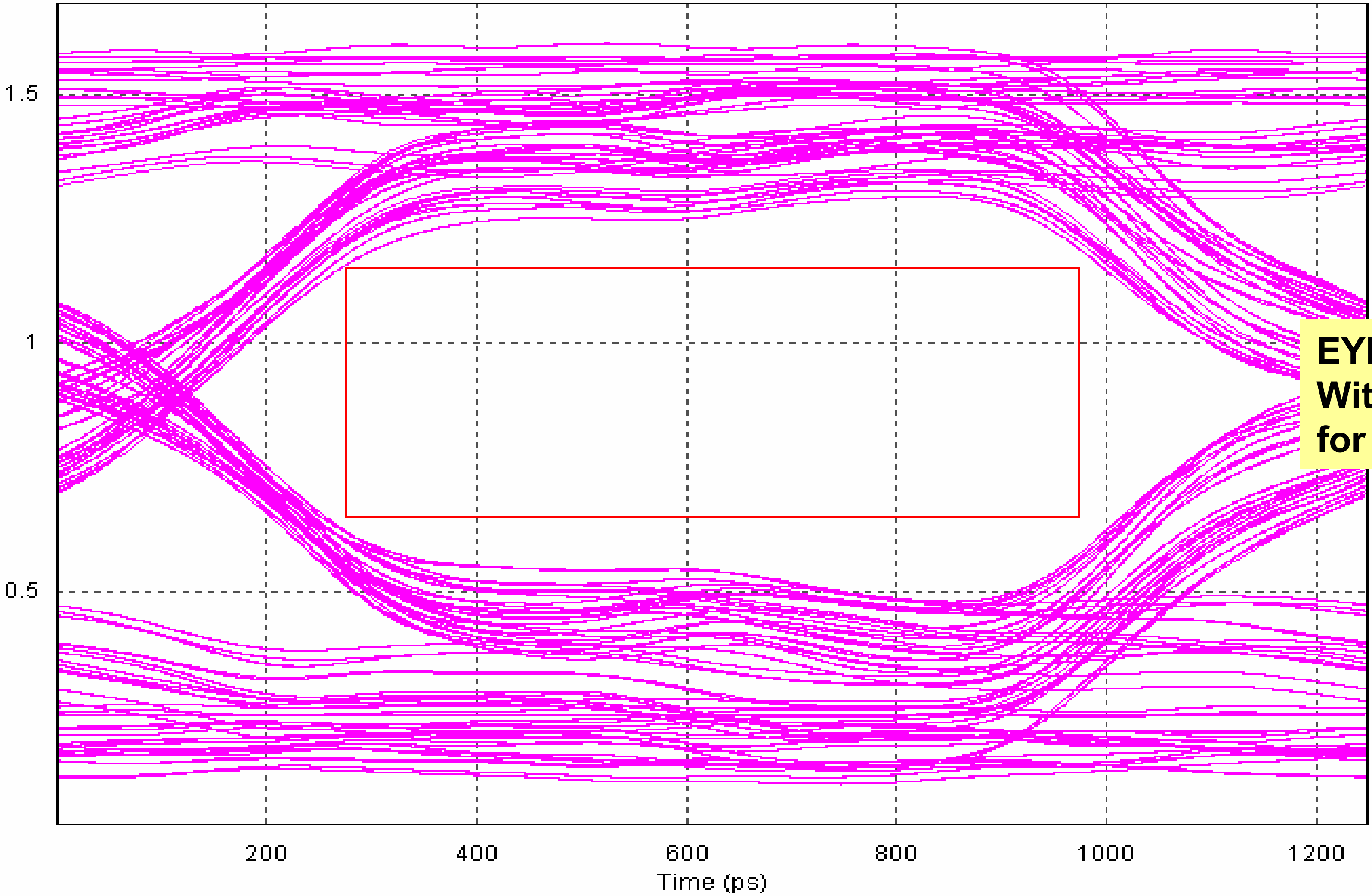
# Eye diagram with $C_{mim}$ = 3 nF, Rc4 = 0.25 Ω and 64 DDR3 IOs switching simultaneously at 400 MHz



**EYE is Cleaner With valid data for $C_{mim}$ = 3 nF**

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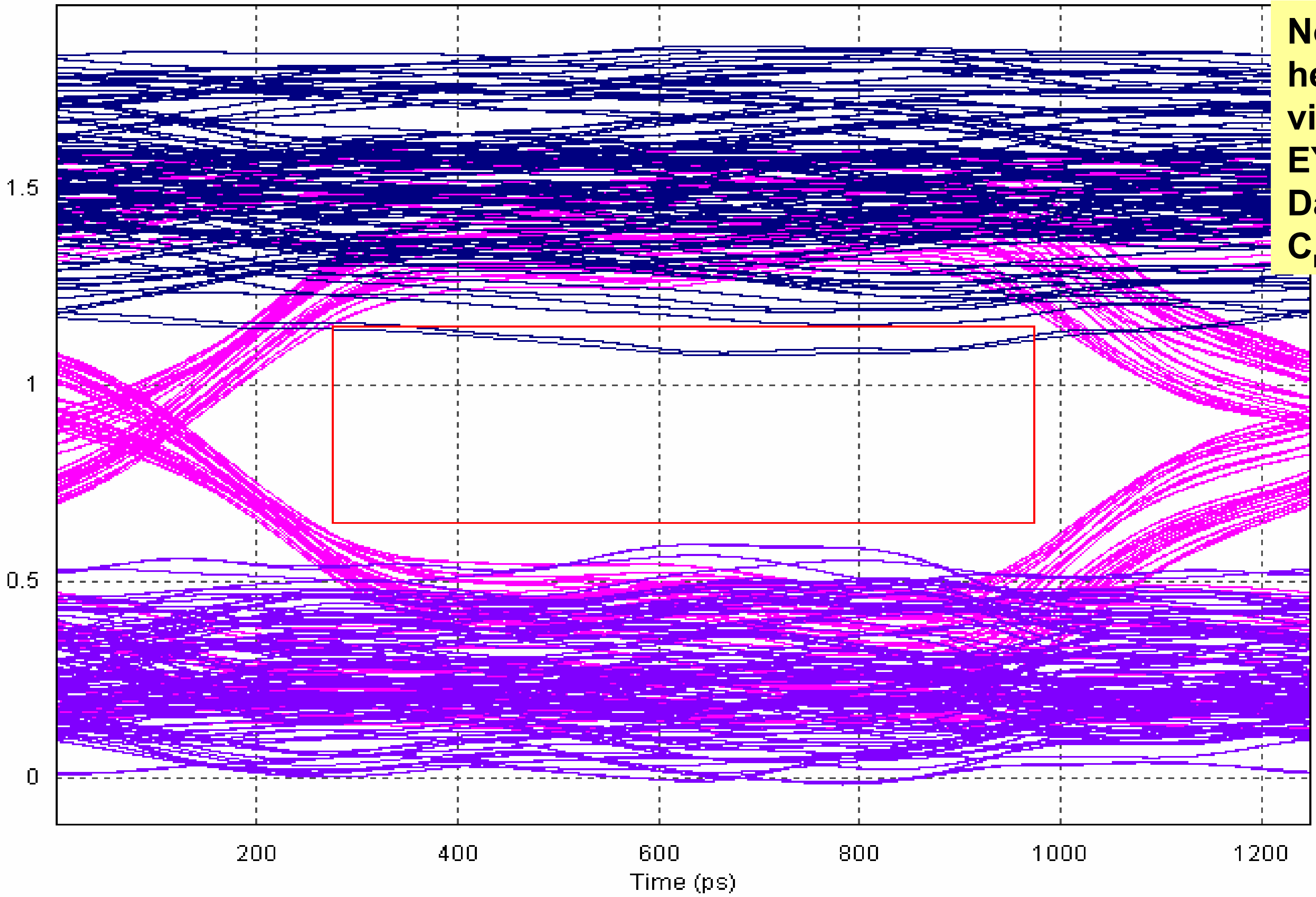
# Eye diagram with $C_{mim}$ = 3 nF, Rc4 = 0.25 Ω and 62 DDR3 IOs switching simultaneously at 400 MHz



Noise at signal held high violates the EYE with valid Data for $C_{mim}$ = 3 nF

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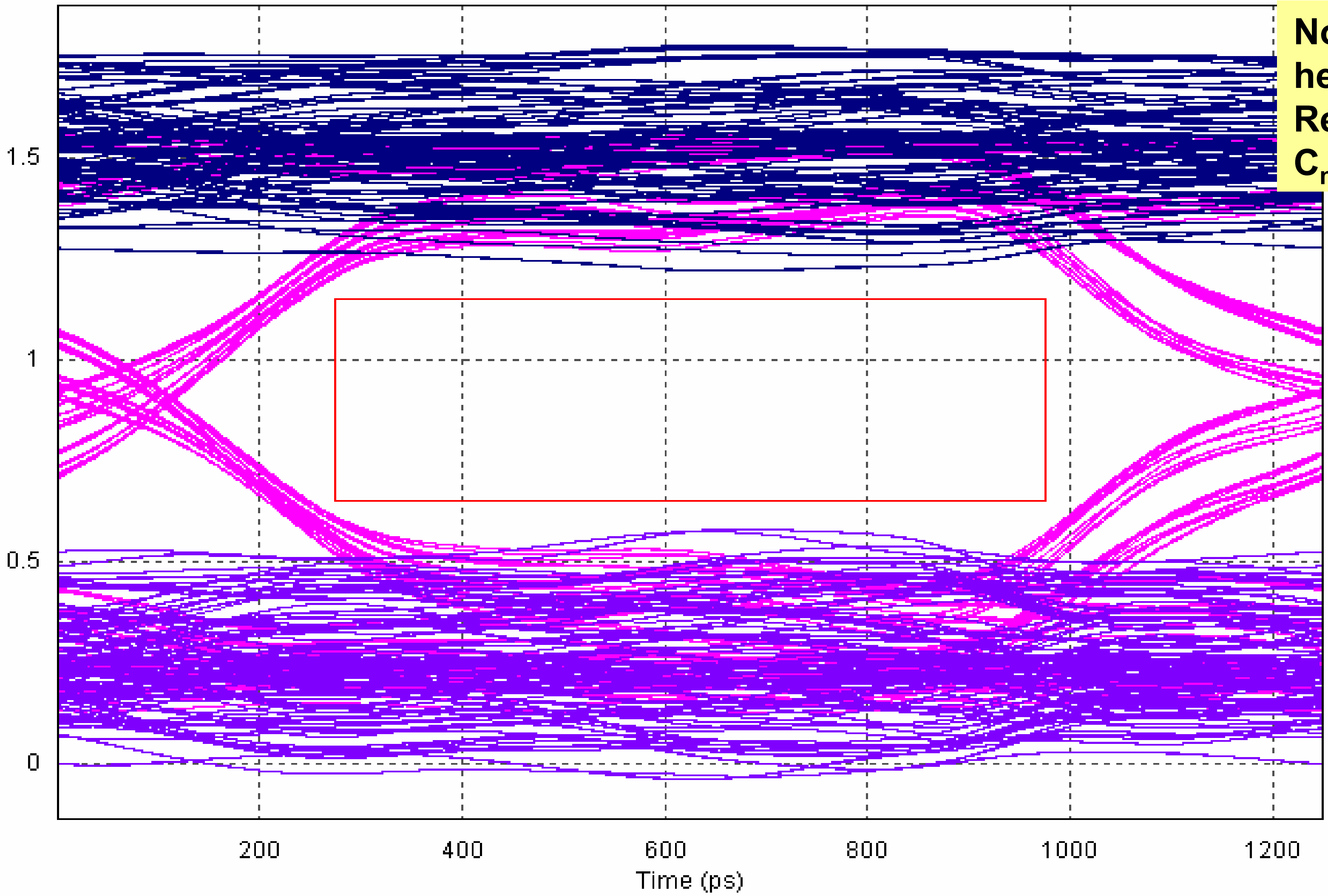
# Eye diagram with $C_{mim}$ = 10 nF, Rc4 = 0.25 Ω and 62 DDR3 IOs switching simultaneously at 400 MHz



**Noise at signal held high Reduces with $C_{mim}$ = 3 nF**

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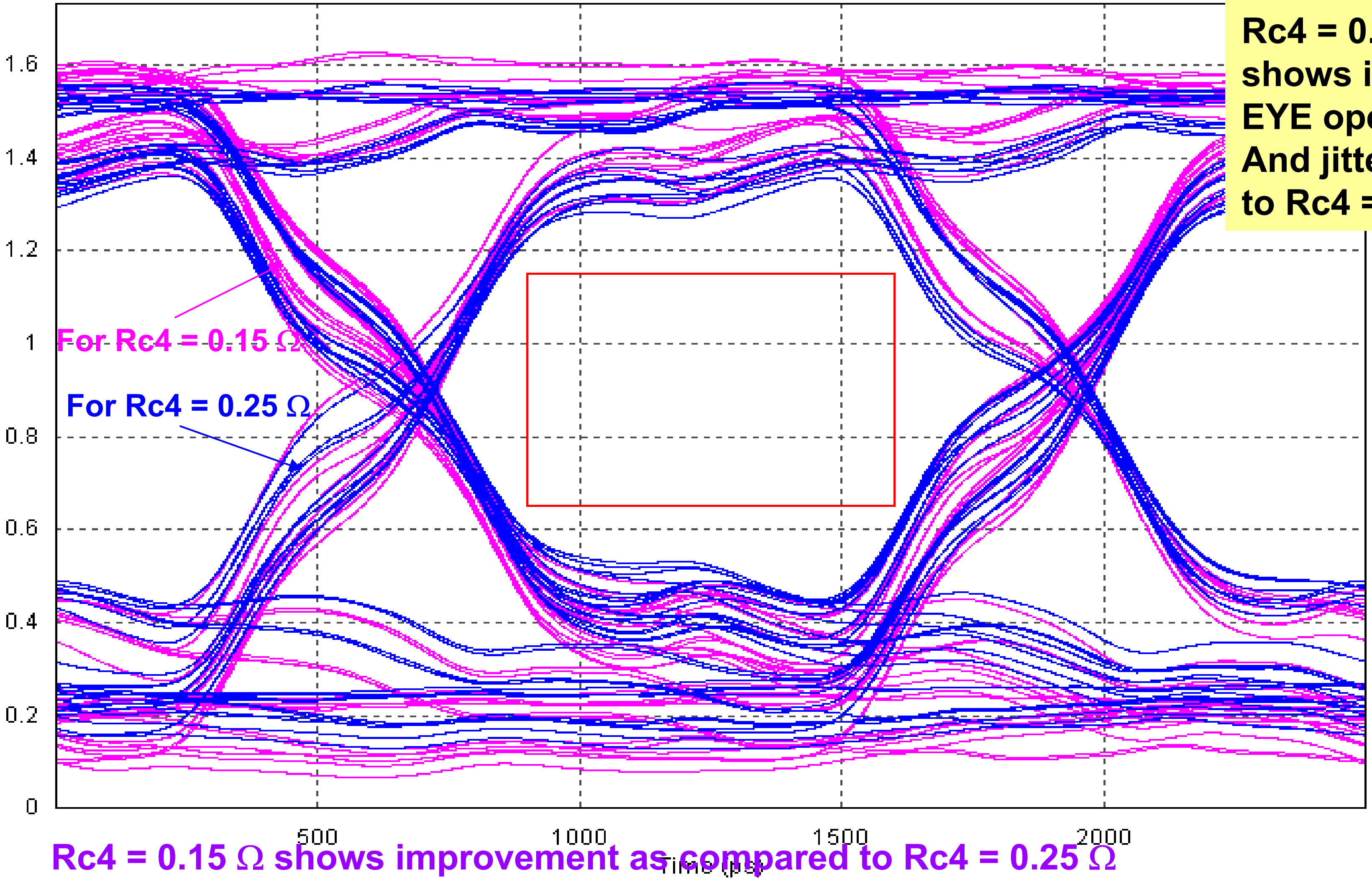
# Eye diagram with $C_{mim}$ = 10 nF, Rc4 = 0.25 Ω and 62 DDR3 IOs switching simultaneously at 400 MHz



**Rc4 = 0.15 shows improves EYE opening And jitter as to Rc4 = 0.25**

**Rc4 = 0.15 Ω shows improvement as compared to Rc4 = 0.25 Ω**

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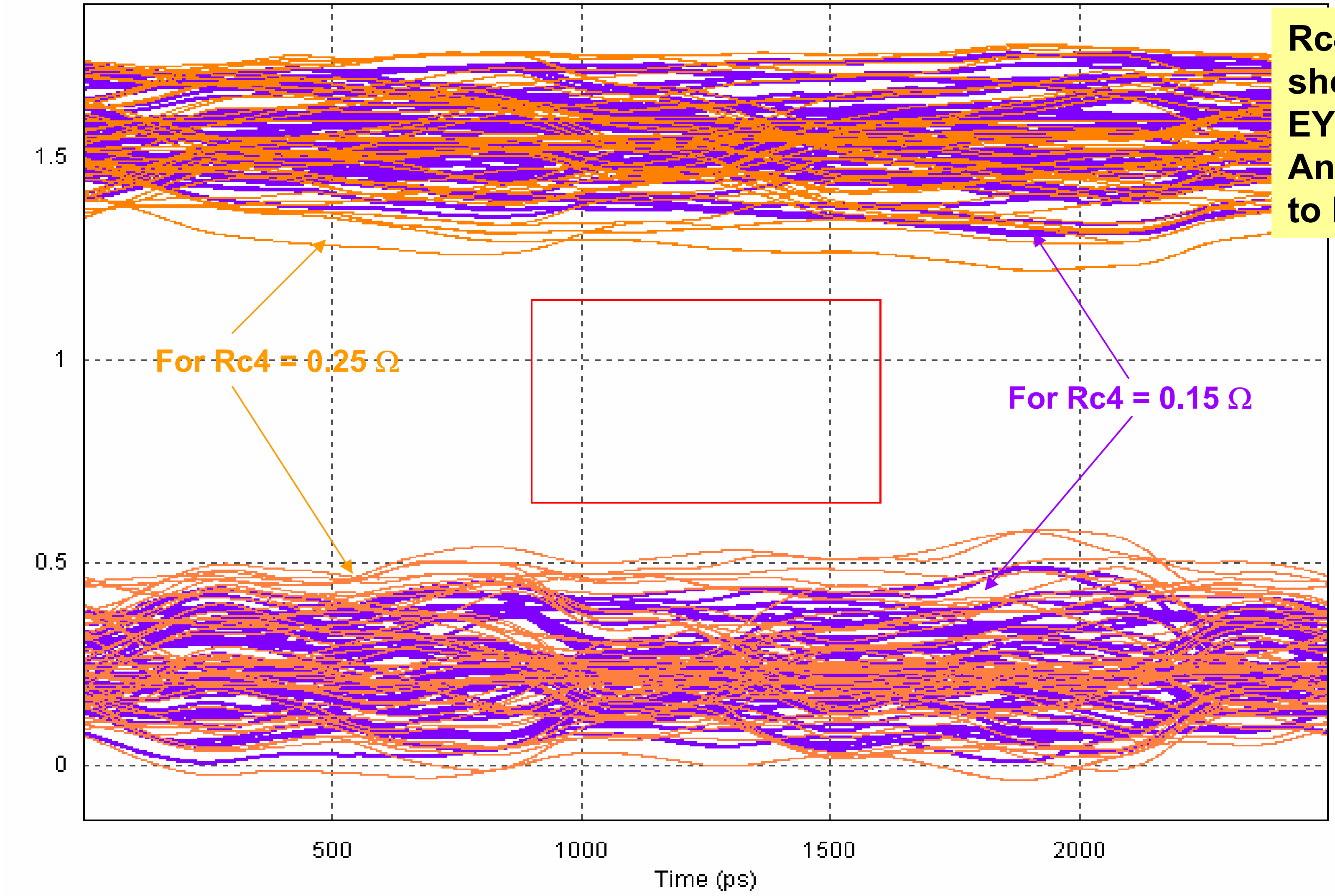
# Eye diagram with $C_{mim}$ = 10 nF, Rc4 = 0.25 Ω and 62 DDR3 IOs switching simultaneously at 400 MHz



For Rc4 = 0.25 Ω

For Rc4 = 0.15 Ω

**Rc4 = 0.15 shows improves EYE opening And jitter as to Rc4 = 0.25**

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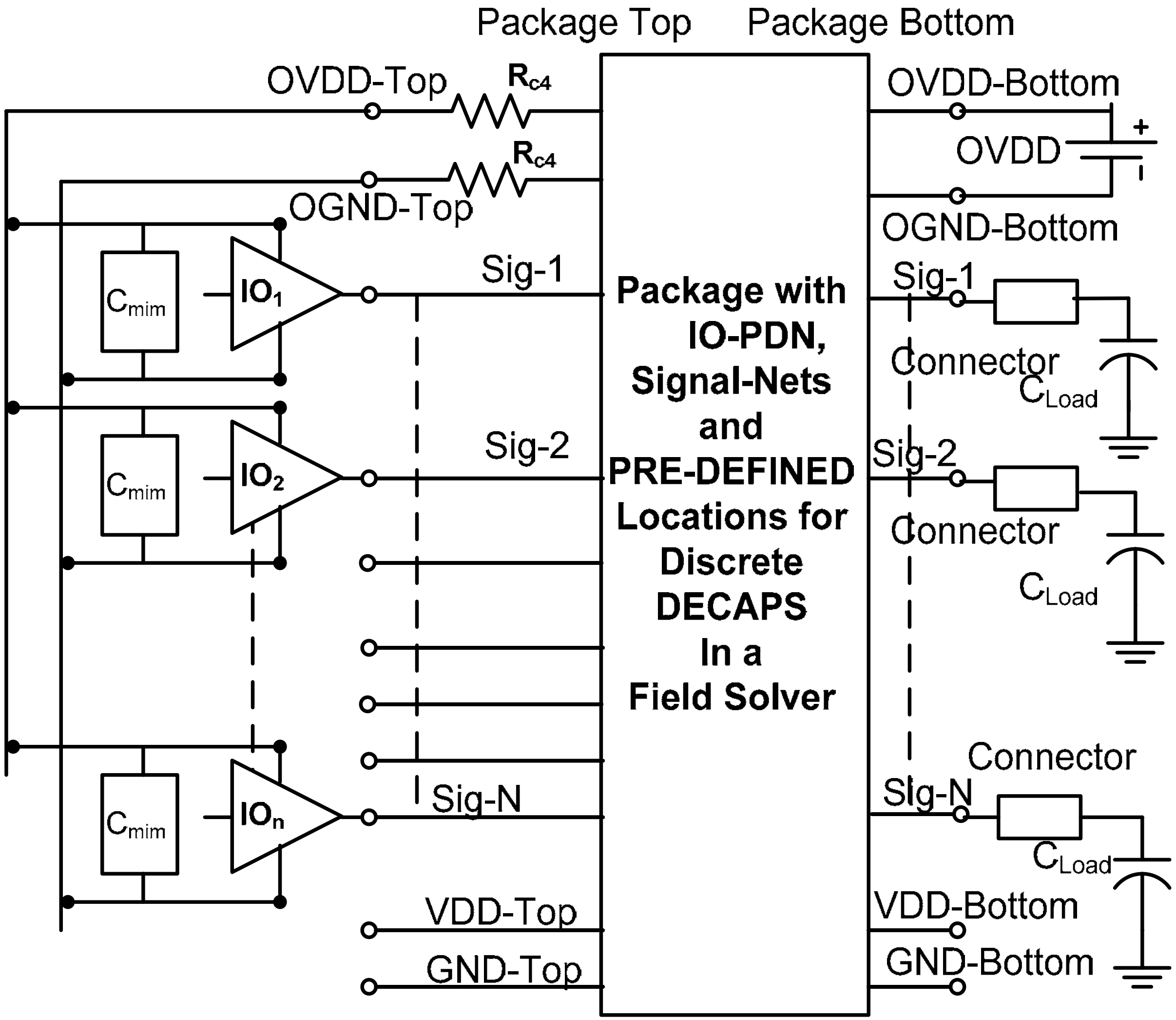
# SSN Simulation setup considering Distributed model of On-die High-K MIM DECAP



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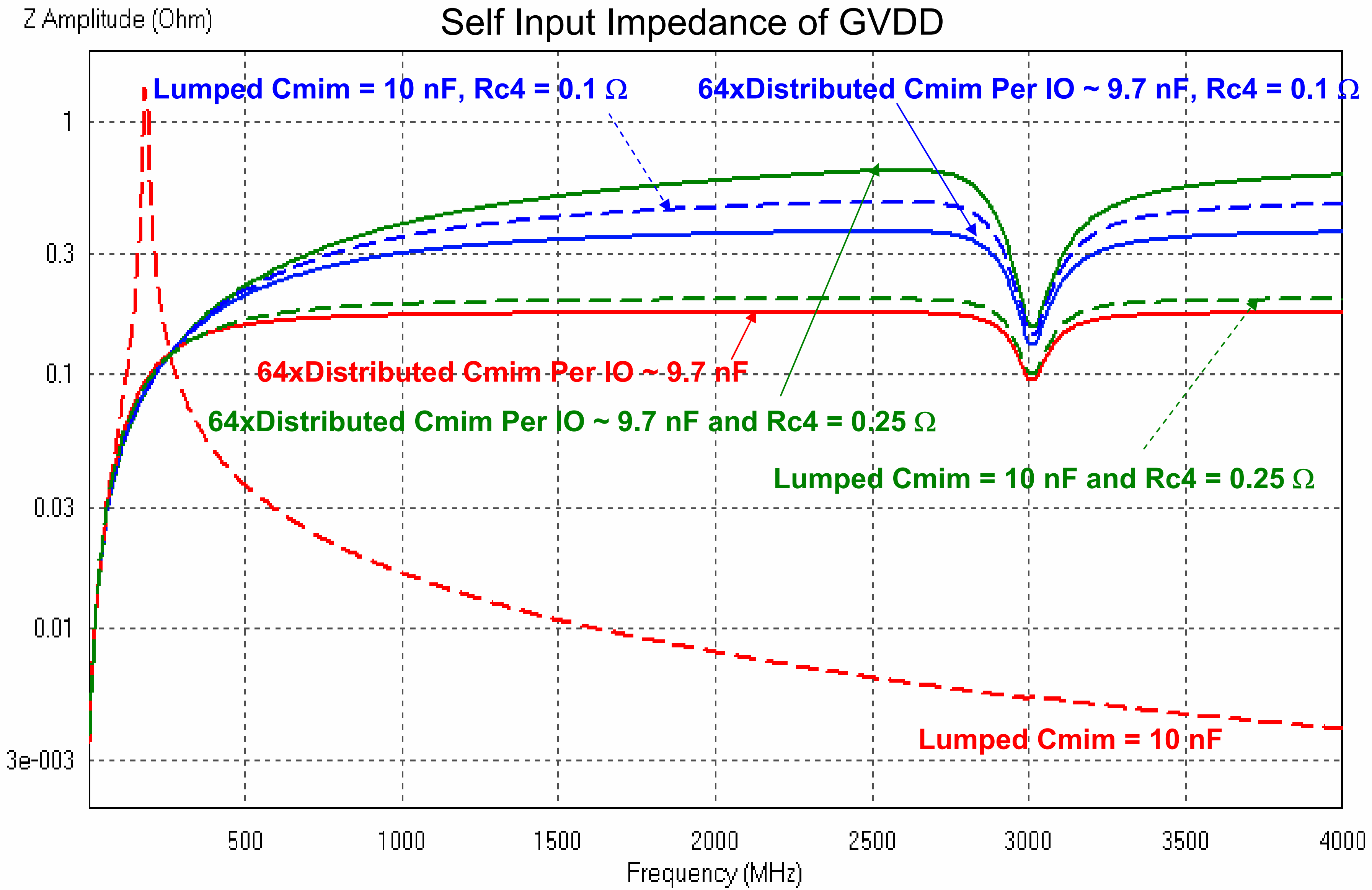
# Input impedance for both lumped Distributed $C_{mim}$



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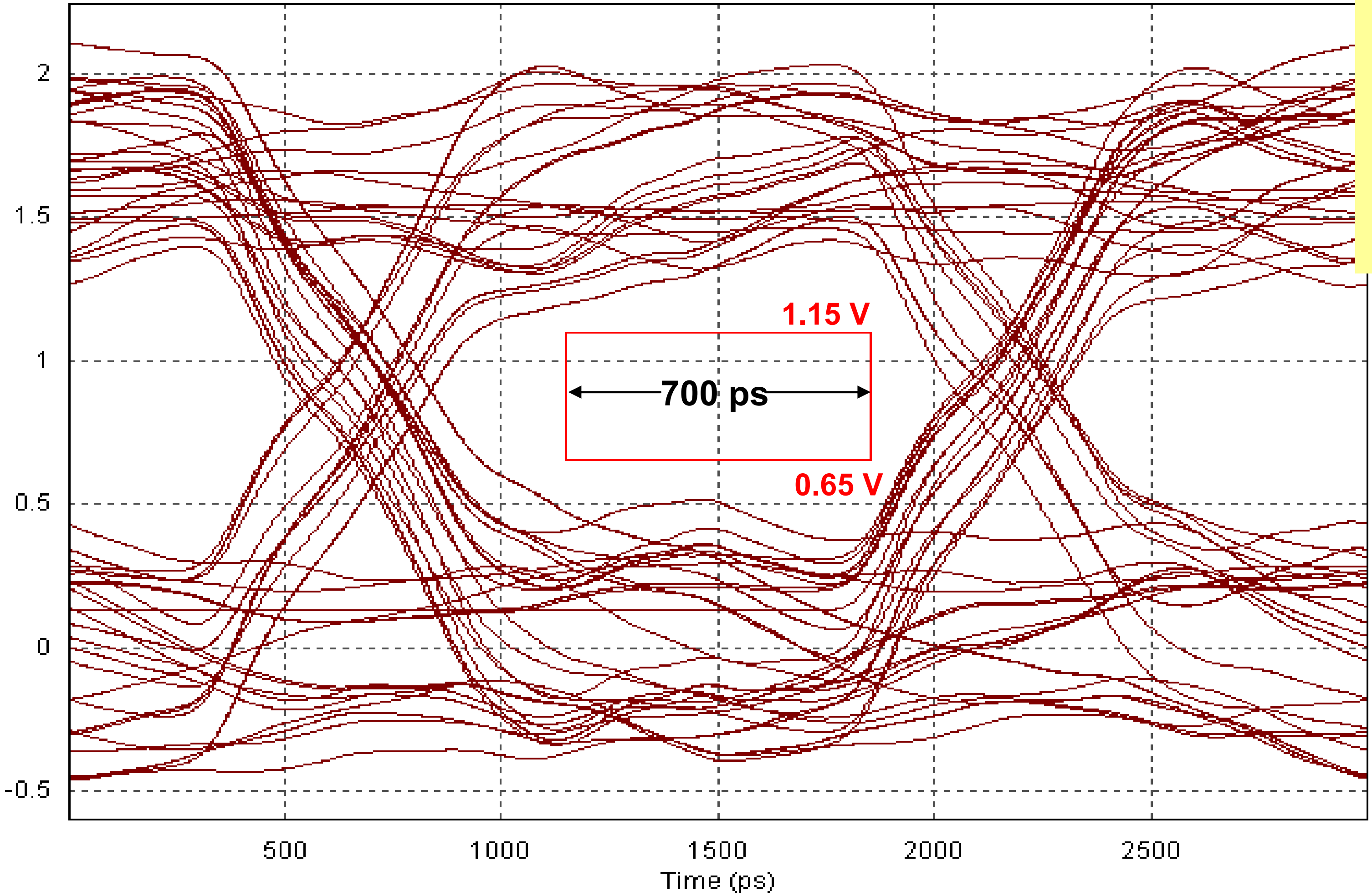
# EYE diagrams for switching signal with 144xDistributed $C_{mim}$ per IO (Total Cmim ~ 18 nF), and 64 IOs switching at 333 MHz



**EYE with Distributed $C_{mim}$ has valid data Window with more margin and less jitter**

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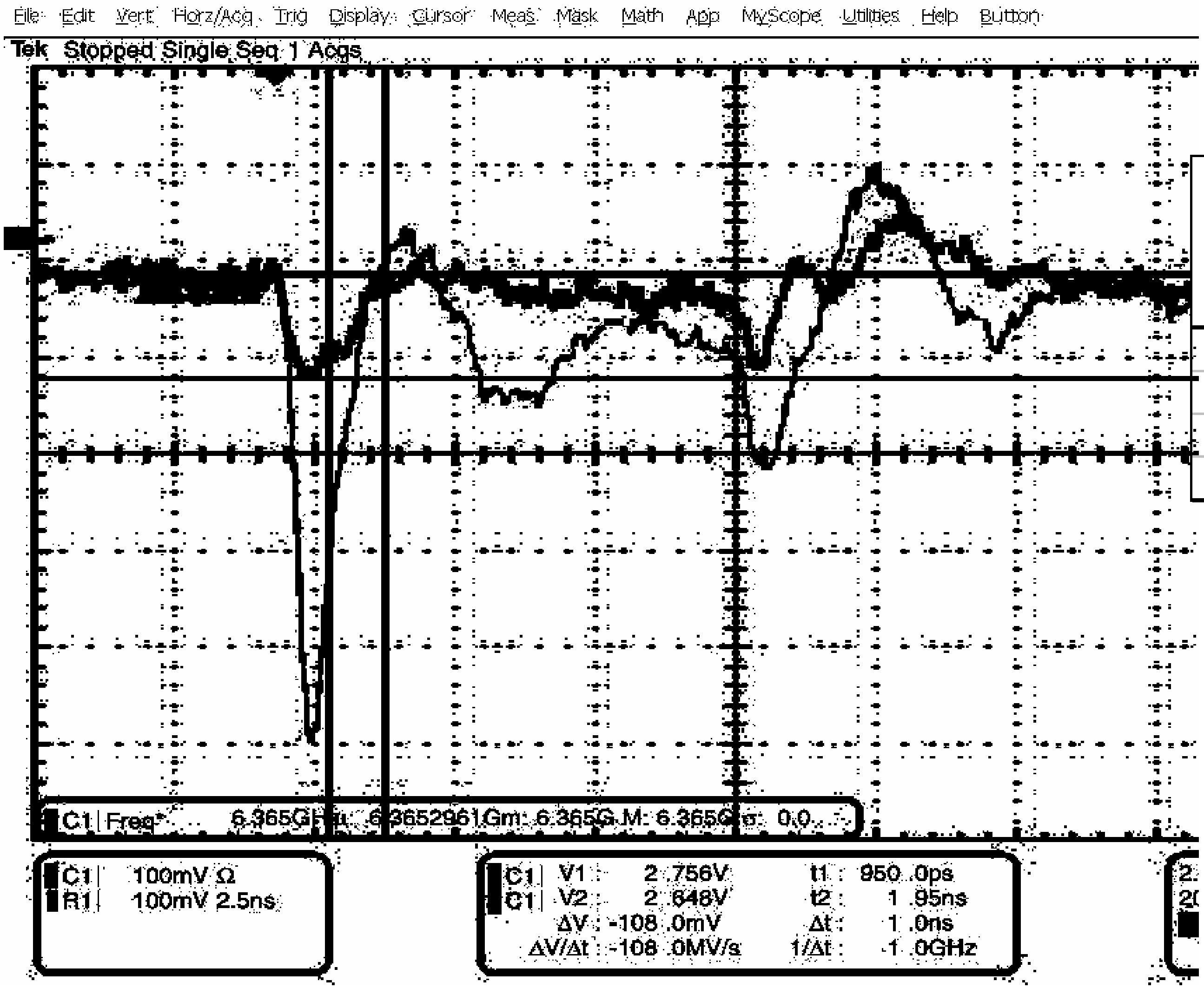
# Measured voltage across quite lines with 64 DDR2-667 IOs switching MIM vs non-MIM results



```
C1 | Freq*   6.365GHz μ: 6.3652961G m: 6.365G M: 6.365G σ: 0.0

C1 |  100mV Ω
R1 |  100mV 2.5ns

C1 | V1 :    2.756V        t1 :  950.0ps
C1 | V2 :    2.648V        t2 :    1.95ns
      ΔV : -108.0mV        Δt :    1.0ns
   ΔV/Δt : -108.0MV/s    1/Δt :   -1.0GHz
```

**DDR Driver collapse during SSN**

| Bits Switching | MIM Pk-Pk mV | non-MIM Pk-Pk mV |
|---|---|---|
| 64 | 184 | 620 |
| 32 | 144 | 536 |
| 16 | 133 | 520 |
| 8 | 71 | 414 |

**BIG DELTA between MIM part and Non-MIM part!**

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# CONCLUSION

- **From results described in this paper, we have concluded that On-die High-K MIM DECAP of significant amount is critical**
  - **to realize the resonant free input impedance of the IO-PDN, and**
  - **to mitigate the PWR-GND noise voltage generated in PKG**

- **Increased amount of Capacitance density of On-die High-K MIM capacitors as compared to Gate-Oxide DECAPS provide significant improvements in noise, speed, power, Silicon-to-design correlation, debug time and time to market!**

- **Large amount of effective capacitance (~ 20 nF) can be obtained from On-die High-K MIM DECAP with appropriate physical implementation**

- **We have shown significant reduction in rail collapse and SSN by implementing On-die High-K MIM DECAP in a 90nm SOI microprocessor**

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# Conclusion (Contd)

- Distributed circuit models for On-die High-K MIM DECAPs are discussed in detail

- We have shown that SSN reduction by the distributed model of the On-die High-K MIM DECAP is close to that of an ideal capacitor.

- It is shown that value of $R_{c4}$ ($R_{metal}$ plus PWR/GND resistance of C4's) resistance is critical for SSN reduction using On-die High-K MIM DECAP

- We have shown a Methodology to estimate critical value of
  - On-die High-K MIM DECAP for a known value of effective IO-PDN loop inductance and the switching frequency of IOs, and
  - Critical value of Rc4 resistance for known a known value of effective loop inductance of IO-PDN and DIE/MIM capacitance

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# References

[1] Om P. Mandhana and Jin Zhao, “Methodology for On-Package Decoupling Capacitor Selection with Considerations of Coupled Core and IO Power Delivery Network and Simultaneous Switching Noise Effects”, *Proceedings of Electrical Performance of Electronic Packaging,* Austin, TX, October 2005, pp 175-178

[2] Héctor Sánchez, Bill Johnstone, Doug Roberts, Om Mandhana, Brad Melnick, Muhsin Celik, Mike Baker, Jim Hayden, Min Byoung, J. Edgerton, B. White, “Increasing Microprocessor Speed by Massive Application of On-Die High-K MIM Decpoupling Capacitors”, *Solid-State Circuits, 2006, IEEE International Conference Digest of Technical Papers,* Feb. 6-9, 2006, Page(s): 2190-2199

[3] Roberts, D.; Johnstone, W.; Sanchez, H.; Mandhana, O.; Spilo, D.; Hayden, J.; Travis, E.; Melnick, B.; Celik, M.; Byoung Woon Min; Edgerton, J.; Raymond, M.; Luckowski, E.; Happ, C.; Martinez, A.; Wilson, B.; Pak Leung; Garnett, T.;Goedeke, D.; Remmel, T.; Ramakrishna, K.; White, B.E., Jr.; “Application of on-chip MIM decoupling capacitor for 90nm SOI microprocessor”, Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, 5-7 Dec. 2005 Page(s): 72-75

[4] www.sigrity.com

[5] Chi-Te Chen, Jin Zhao, Qinglun Chen, “A Simulation Study of Simultaneous Switching Noise”, Proceedings of 51st Electronic Components and Technology Conference, 29 May-1 June 2001, Pages(s)1102-1106

[6] Om P. Mandhana, “Modeling, Analysis and Design of Resonant Free Power Distribution Network for Modern Microprocessor systems”, IEEE Transactions on Advanced Packaging, vol. 27, No. 1, February 2004, pp. 107-120

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