Infineon

EMI Modeling and Simulation in the IC Design Process

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Overview

- Power integrity (PI) of ICs
- PI in the IC design flow
- NEMO: Dynamic current profiles
- EXPO: Early PI case studies
- XcitePI: Sign-off PI simulation
- Conclusion

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Importance of Power Integrity

- Power Integrity problems are caused by the switching on large clocked ICs
- Power Integrity handles basically 3 types of problems:
  - Power bounce affects the functionality of the IC circuits by
    - Causing circuit failures
    - Reducing the speed of circuits
    - Leading eventually to latch-up of CMOS circuits
  - Conducted emission leaves the chip through the package and disturbs the switching of the circuits of other PCB components
  - Radiated emission is caused by effective antennas in IC package or PCB which are excited by high frequencies conducted from the chip
- EMI issues are Power Integrity issues
- A detailled understanding of the local power integrity is very important
- Simulation tools are mandatory to understand and predict the power integrity of large VLSIs

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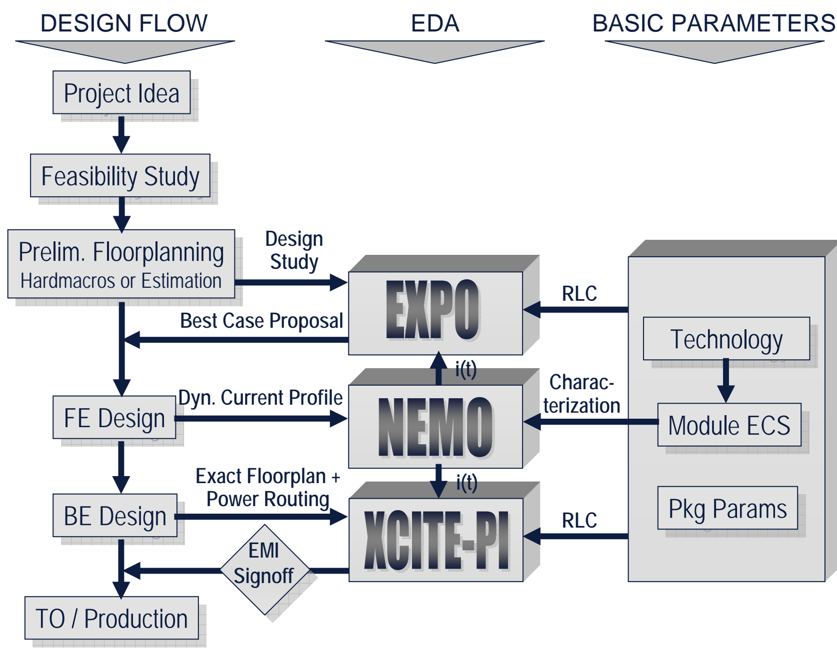
EMI Simulation in IC Design Flow



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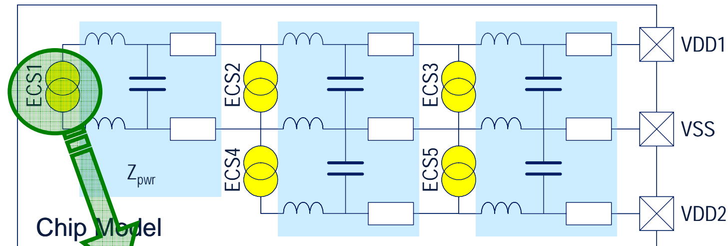
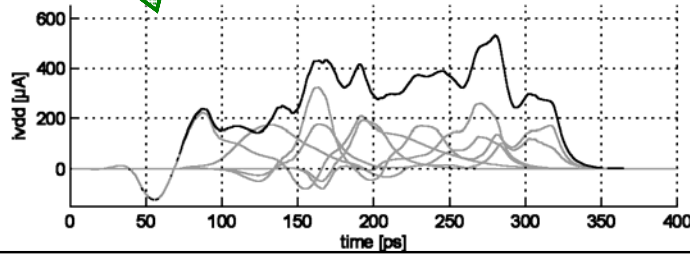
NEMO: Dynamic Current Profiles of Digital Function Modules

- Goal: create a „simple“ chip model
- Netlist-based dynamic current sources
- Details in next presentation





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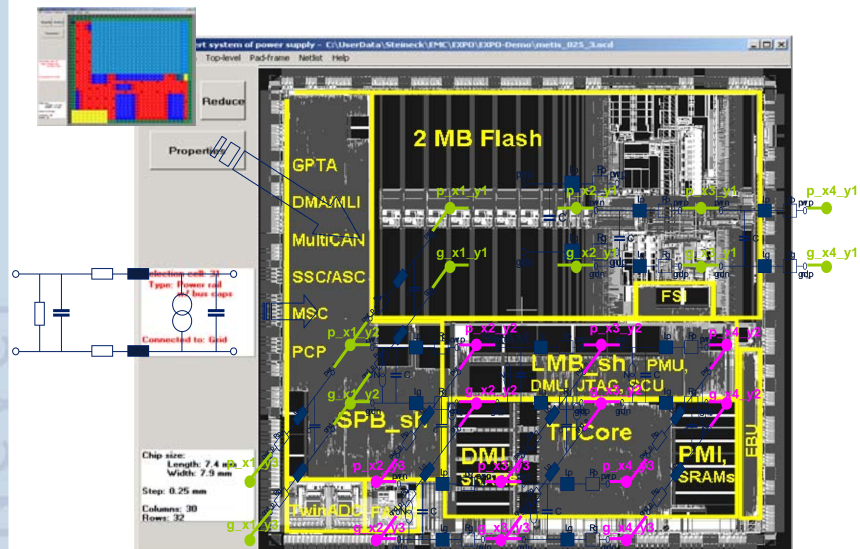
EXPO: 32-Bit Microcontroller On-Chip Layout Entry



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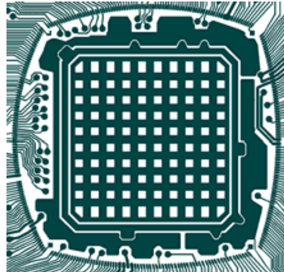
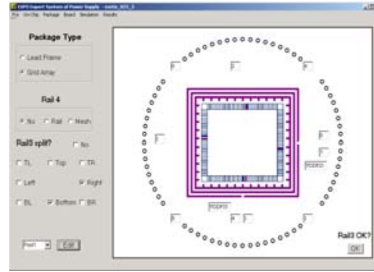
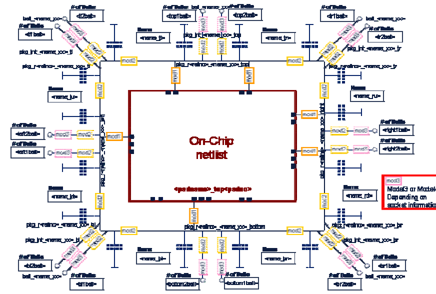
EXPO: 32-Bit Microcontroller Package Design Entry







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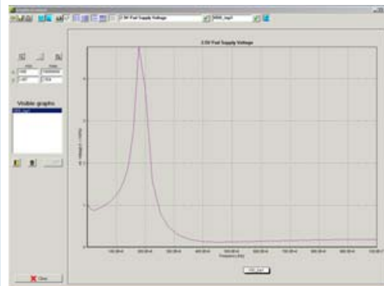
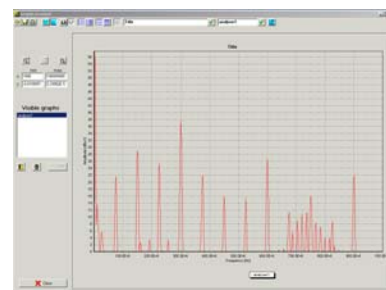
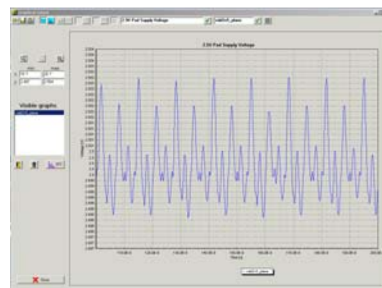
EXPO: Output Visualisation



AC Analysis



FFT Spectrum



Transient

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EXPO: Measurement ⇔ simulation correlation

Simulation
Measurement

Conducted Emission
Core Noise VDDC

Conducted Emission
Core Noise Xtalk
VDDC to VDDE

Radiated Emission
Core Noise

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XcitePI: 32-Bit Microcontroller BGA-416 Design

SPEED2000 Generator - [3D View]

Y
X

top
layer

bottom
layer

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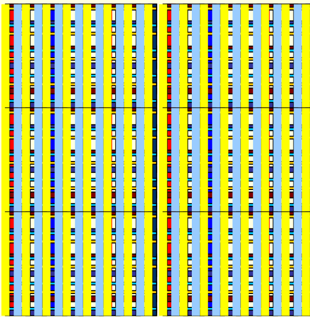
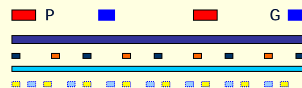
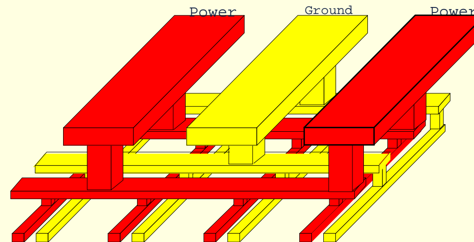
XcitePI: Physical IC Power Grid







In general : An IC-power grid can have up to 10 metal layers, with hundreds to thousands of power grid lines on each metal layer, resulting in tens of millions of metal sections and vias.

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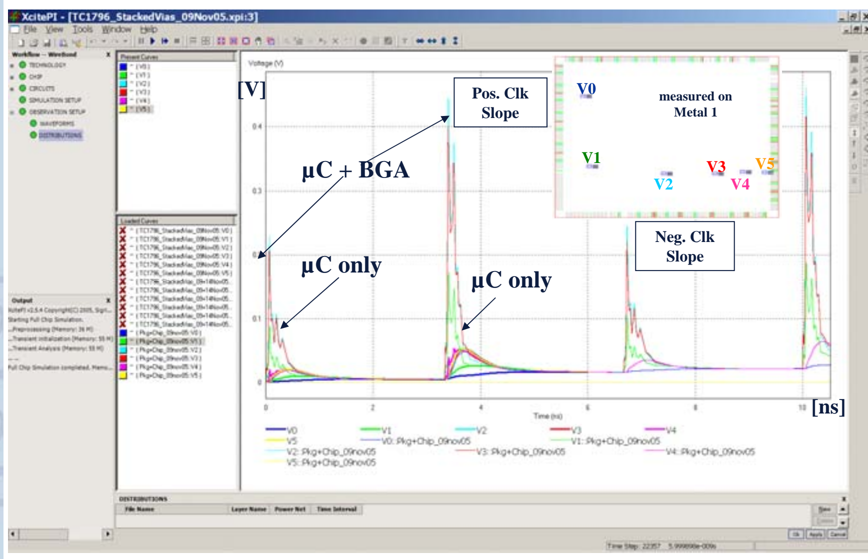
XcitePI: Power Noise Models

- Model 1: VDD-GND differential voltage on chip without package
- Model 2: VDD-GND differential voltage on chip with package



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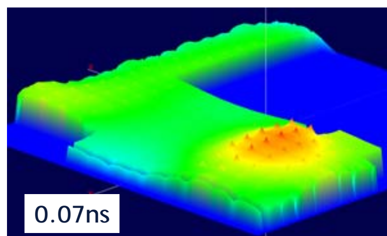
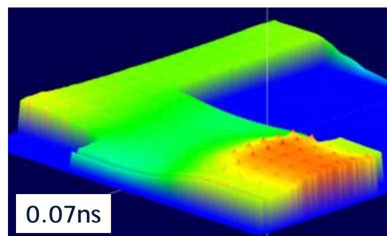
XcitePI: Power Noise Distribution

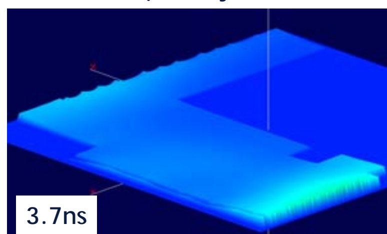
- Model 1: Power noise distribution over the µC without package
- Model 2: Power noise distribution over the µC with package

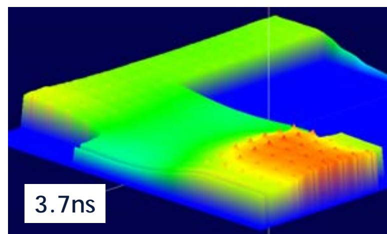




µC only

µC + BGA





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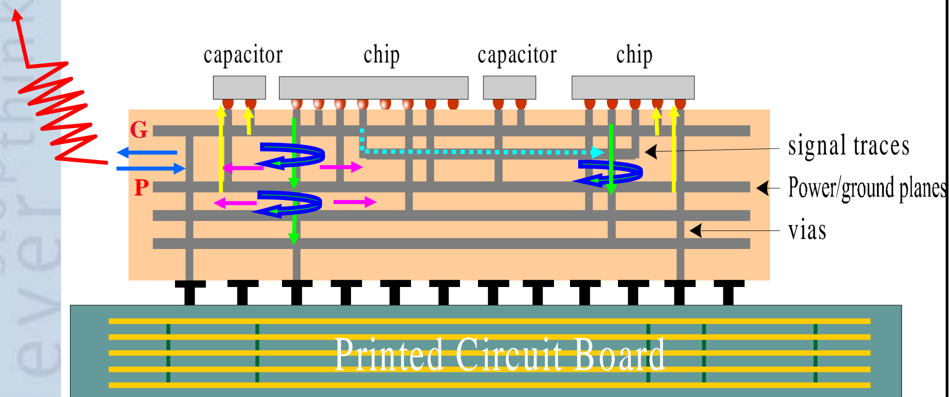
XcitePI: Power Noise Propagation

- The electromagnetic interactions take place inside the planar packaging structures



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XcitePI: Software Algorithm

- A fast fully distributed parasitic extraction of the complete power grid is implemented, which:
  - includes all capacitive and inductive coupling effects
  - on and between layers and between all conductors
- XcitePI incorporates:
  - simultaneous transient analysis of the IC power grid
  - distributed wave propagation effects of the package
- Fast electromagnetic simulation engine with a co-simulation approach for simultaneous:
  - transient Analysis of the IC power grid
  - dynamic simulation of the electromagnetic fields in package planes.

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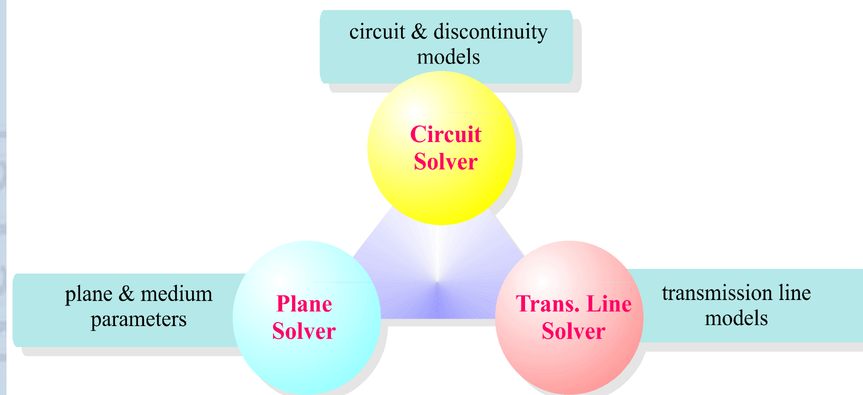
XcitePI: Software Algorithm

- In order to get one final Spice simulation run of the Spice-based analysis:
  - the individual Spice runs of the electrical IC and package structures are merged to one entity within a full-wave 3D solution
- Simulations of complex designs stay in the “minutes” to “hours” range



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Conclusion

- Power integrity (power bounce, conducted & radiated EMI) has become an IC quality criterion
- PI models and simulations are currently implemented into Infineon‘s VLSI-IC design process
- 3 tools have already been successfully tested for their benefit
  - Dynamic current profiles of chip modules are provided by NEMO
  - Early chip/package design case studies are performed with EXPO
  - Netlist-based PI sign-off is performed with XcitePI
- This extended design flow will lead to first-time-right PI quality

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