

Power Integrity Analysis of a Microcontroller (μC) plus its Chip Package (BGA)

Dr. Ekkehard Miersch¹, Thomas Steinecke², Mehmet Goekcen²

¹ EFM Consulting, Schoenaich, Germany

² Infineon Technologies AG, Munich, Germany

Abstract — The power integrity (PI) of the system chip (IC) plus chip package (CP) of a 32-bit microcontroller (μC) has been successfully analysed by co-simulation of the μC plus its BGA. Goal was to examine the limits of the combined power distribution system as a function of the switching activities on the μC . The power noise on the IC is a function of the positioning of the circuit domains, i.e. the logic functions like CPU, cache, on-chip memory etc., the decoupling on the IC (non-switching circuits plus on-chip decoupling), the on-chip leakage currents and the power system impedance distribution on the CP.

The other and most important parameter with regard to system PI is the timing of the circuit domains, which are supplied by their corresponding power domains. The power domains are defined by the local power distribution nets in form of local power grids or traces.

Beside the evaluation of the initial IC+CP system design concept including place+route case studies, the analysis is needed to explore the extendibility of the IC+CP design concept to higher frequencies w/o e.g. having to change the cost/performance CP concept.

This paper describes the electrical power modeling of a 30-million transistor 32-bit automotive microcontroller plus its BGA which allows to generalize the validity of EMI measurements through static I/O pins with the help of dynamic current simulation results, applied to various IC power domains, including also the CP power domains.

1. INTRODUCTION

Electromagnetic emission caused by switching activity of large clocked ICs like microcontrollers is an important quality criterion which may lead to customer rejection of an IC and missed design-wins. Thus it is essential to provide modeling and simulation tools which allow to predict the EMI behaviour of complex ICs before costly masks are generated and silicon is fabricated. The modeling and simulation approach described in this paper is intended to be established as EMI sign-off process for automotive microcontrollers at Infineon Technologies AG. In cooperation with the tool vendor Sigrity, the 32-bit microcontroller TC1796 was modeled, and noise distribution on chip and through the package has been simulated. This IC is complex enough to really investigate the noise propagation paths and even self-disturbance of the chip.

Once switching noise is generated at certain locations (circuit domains) on an IC, the noise often propagates more easily to other locations (circuit domains) of the chip through the package power and ground structures rather than directly through the chip power grid itself. This is particularly true for flip-chip packages, but also for wire-bonded chips, see Fig.1.

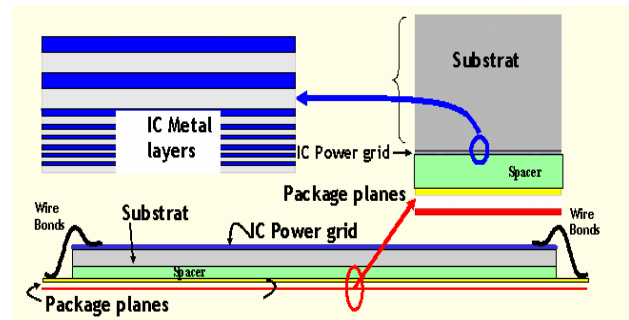


Fig. 1. Concept of co-simulation of wire-bonded ICs plus chip packages

In the case of the Infineon 32-bit microcontroller TC1796, the behaviour of the IC plus its chip package is analyzed to understand the different ways of noise distribution. Fig. 2 shows the complexity of this product. The TC1796 consists of approx. 30 million transistors and is mounted in a P-BGA 416 package. The μC contains ca. 10 power supply domains, of which the main supplies are connected to rings on the package substrate. The whole chip/package system is therefore very complex.

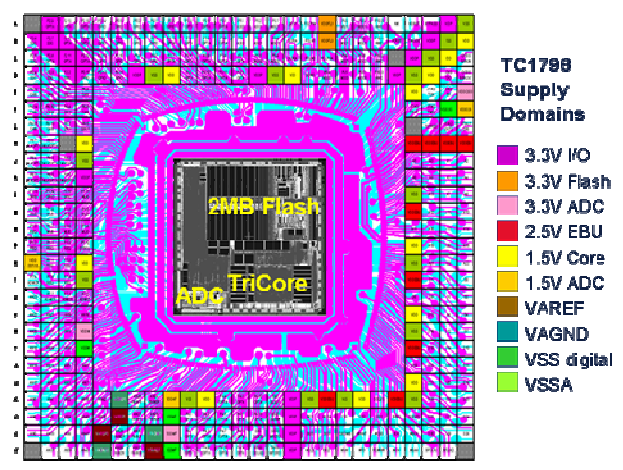


Fig. 2. TC1796 chip-package configuration

The goal is to gain a reliable model for dynamic current flow through the μC wire bonds/balls. The results have to reflect chip design changes (module placement, power routing) and package design changes (BGA substrate, integrated passives).

An alternate approach for the RLC parasitic extraction of the on-chip power supply system [1] was developed in the Medea+/BMBF funding project MESDIE, Fkz 01 M 3061 H [2].

2. CHIP AND PACKAGE MODELING

The switching activities on the μC need to be modeled with the help of high-quality on-chip current sources, which are distributed all over the silicon die as a function of the individual circuit domains. These current sources are connected by the on-chip power supply network, realized by a combination of grid and ring structure. The power network also has to contain the distributed on-chip capacitors and leakage currents. This system is modeled by co-design [3], [7] in a retroactive way, such that current paths through the package are re-entered into the silicon.

Results of this co-simulation are dynamic currents or voltages at various points of interest, e.g. power supply package balls. The dynamic currents and voltages can afterwards be re-used by PCB simulations considering noise decoupling circuits.

Lumped RLC or simplified S-parameter models would fail to consider off-chip package effects, as they are unable to take into account the distributed interaction between IC power grid and chip package, and are thereby unable to determine the true transient noise distribution and behavior in the power delivery system.

Consequently accurate modeling of the noise behaviour of high-speed ICs therefore necessitates the modeling of distributed electromagnetic wave propagation effects in the package planes and the distributed interactions between IC power grid and package structures, as done in Speed2000 [7],[5] + Co-Simulator [7] + XcitePI [6].

This way it is possible to evaluate different decoupling schemes, to simulate the impacts of various distributions and characteristics of the given source excitations. It is also possible to assess the effects of chip packages and one can perform what-if comparisons to optimize electrical performance, power grid physical parameters etc.

3. ELECTRICAL DESCRIPTION OF μC AND BGA

Major goal is a high-quality correlation between simulation results and EMI measurements in the time domain. Once the good quality of the simulation model has been demonstrated, models for new chips and their packages are trusted to deliver realistic simulation results already during the IC design phase without having physical measurement values.

In the case of the TC1796 the 32-bit μC is wire-bonded to a two-layer BGA. BGA and the wire-bonds are shown in Fig. 3.

The power distribution system of the μC is distributed over the 7 metal layers of the CMOS chip plus the power distribution system of the BGA. The on-chip power distribution consists of ring buses, regular power grids of core logic and on-chip memory and the more or less

regular power nets grids in the analog circuit part of the μC .

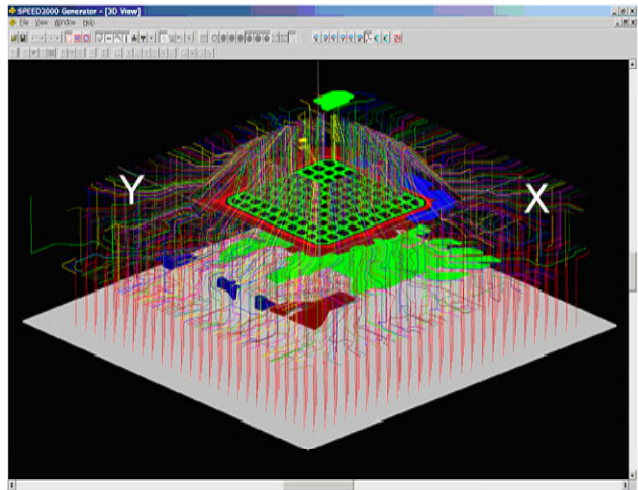


Fig. 3. 416 wire-bonds connect the 32 bit μC with its two-layer BGA.

The power net distribution system of the two-layer BGA connects the μC power net distribution system with corresponding PCB power nets, which have to supply the chip with power within the corresponding total design.

All static and dynamic electrical characteristics of the materials, needed to form the IC and the BGA, were considered in the XcitePI and SP2k simulations. The full wave solver algorithms of XcitePI and SP2k cover automatically the coupling of all vias and the inter-plane coupling of all involved power patches and power planes. The power trace coupling on chip is covered automatically; the power trace coupling on the BGA with SP2k can also be automated on request. The power net grid geometry of the μC is described by tables. The table data can be manually generated in XcitePI or in EXCEL¹ tables or can be read in automatically through LEF/DEF² data, defining the μC design. The EXCEL tables can be converted into .xml data. XML³ is the XcitePI input format.

The power integrity (PI) analysis for the μC is performed within XcitePI [6]. The μC has 9 VDD and 4 GND power net systems, the BGA contains 4 VDD and a common GND power net system.

The PI-analysis of the BGA, done with SPEED2000 (SP2k), covers the BGA plus the wire-bonds between the BGA and the μC . The BGA geometry can be read into SP2k through the APD⁴) format .mcm.

¹ EXCEL = Microsoft table program

² XML = open source "Extensible Markup Language".

³ LEF/DEF language: Cadence® Library Exchange Format (LEF) and Design Exchange Format (DEF) integrated circuit (IC) description languages. LEF defines the elements of an IC process technology and associated library of cell models. DEF defines the elements of an IC design relevant to physical layout, including the netlist and design constraints. LEF and DEF inputs are in ASCII form.

⁴ APD = Cadence "Advanced Package Designer" program, generates layout data in .mcm format.

As only the μC + BGA without corresponding PCB were simulated, it is assumed that all BGA power solder balls see the idealized supply voltages of the corresponding voltage regulator modules (VRM). Also the VRM internal resistance is so far idealized with 1mOhm.

4. POWER INTEGRITY (PI) AND ON-CHIP CIRCUIT SWITCHING

As already mentioned in the introduction, the switching activities on the μC need to be modeled with the help of high-quality on-chip current sources, which are distributed over the silicon die.

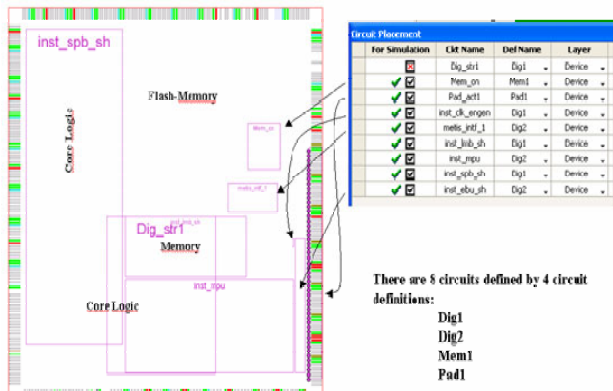


Fig. 4. Some of the device circuits on chip are shown, which are characterized by the current demand during switching, the so called “circuit signatures”.

In Fig. 4 several current sources are connected to the on-chip power supply network, realized by a combination of grid and ring structure. The power network also contains distributed on-chip capacitors.

The current sources, which are current switches, model the switching activities of the individual logic circuit domains on the μC , which is given by the architecture of the μC . The format is SPICE piece-wise linear.

The implemented example of such a modelling is shown in Fig. 4.

5. CO-SIMULATION OF CHIP AND PACKAGE

The chip and package current distribution has to be simulated as a function of given circuit domain switching activities.

Fig. 5 shows the μC embedded in its BGA. During the input procedure of the co-design analysis, the input to the chip data and the chip-package data can still be modified. The simulation and the run-time parameters are defined here exclusively. Those are e.g. the locations at which the noise voltages or the dynamic current behaviour on the local power distribution is of interest. The noise sources need to be provided by the chip designers. A way of automatic generation of dynamic current profiles for large digital function modules is described in [8].

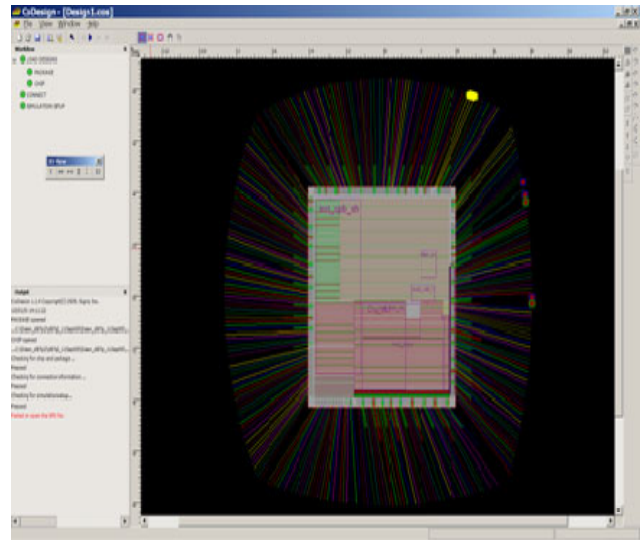


Fig. 5. CoDesign program: μC and wire-bond area of BGA are shown.

Fig. 6 is an example of a chosen set of view points for a given switching activity on the μC with and without BGA. The circuit signature repetition rate is about 6 ns. From these individual analysis results it can be concluded that the power distribution shows considerable variations over time and that these variations are larger with BGA than without BGA. As minimum it can be concluded that PI simulations of an IC alone do not deliver a complete picture of the power distribution variations on the IC under real world application conditions. Combined with measurements, the shown simulation techniques allow a better insight into the existing power distribution implementation and its characteristics.

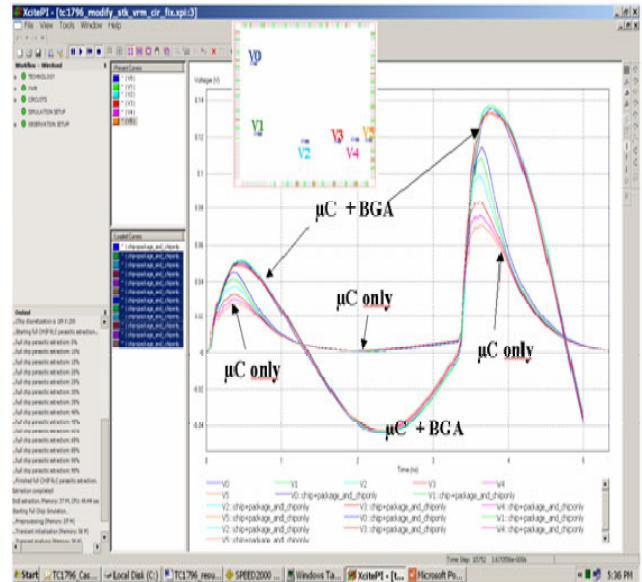


Fig. 6. Power potential distribution over the μC as function of the location and time for the μC only and the μC + BGA.

As can be also seen from Fig. 7, the power potential variations are considerably higher for μC + BGA.

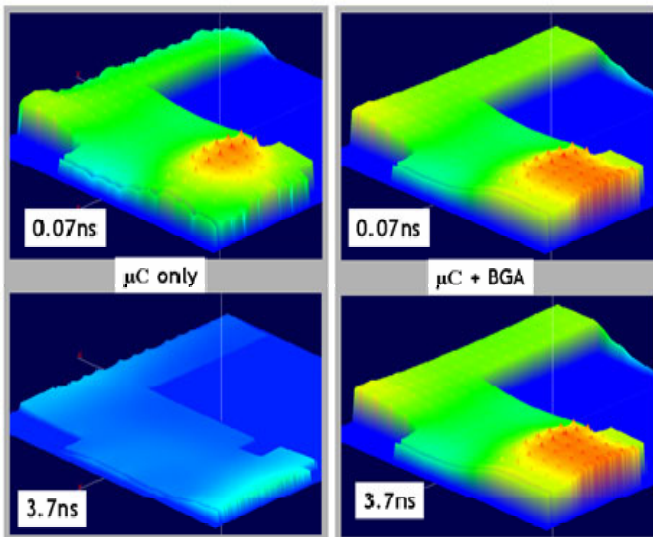


Fig. 7. Comparison of power potential variations as function of time and location for the $\mu\text{C} + \text{BGA}$ and the μC w/o BGA. It can be seen that the power potential variations of $\mu\text{C} + \text{BGA}$ are considerable larger than those of the μC alone.

6. CONCLUSIONS

It has been successfully shown for the first time that it is possible to determine the power integrity of the entity “wirebonded IC plus its chip package”. CoDesign can analyse the power integrity of IC flip-chip packages as well as wire-bonded IC+CP units. This functionality is necessary to perform a design-based reliable sign-off analysis for complex digital and mixed-signal ICs with respect to electromagnetic emission.

7. ACKNOWLEDGEMENTS

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