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Joint Study of Simultaneous Switching Noise and IO Return Current for CMOS FPGA Package

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Abstract
Simultaneously switching noise (SSN) has been studied mainly from power distribution network (PDN) perspective. Signal transmission line effects associated with IO networks are often excluded from SSN study. However, signal traces use part of PDN as reference plane for return current path. The IO noise due to return current can have direct impact to the power network integrity, especially for field programmable gate array (FPGA) chips containing massive number of IOs. This paper will present a joint study of return current effect and SSN with focus on ways to minimize the impact through chip and package co-design.

Author Biography

Dr. Hong Shi is a Member of Technical Staff in the Packaging Technology Group of Altera Corporation. His current responsibilities include developing strategy for high density and high-performance FPGA packaging, simulating system level electrical performance and developing chip-package-board interconnect co-design capability. Before joining Altera, Hong was principal engineer and project leader for Agilent's first 40Gbps digital communications analyzer module. Hong has published over 30 technical papers and has twice received the Agilent "Spark of Insight" award for his contribution to the company. Hong obtained his PhD in microwave optoelectronics field from CREOL College of Optics at University of Central Florida.

Introduction

Advances in complementary metal-oxide-semiconductor (CMOS) technology result in rapid increases in circuit density, faster device switching speed, and higher input and output (I/O) densities. These trends lead to circuit designs with high simultaneous switching activities at high clock frequency. The result is an increase in simultaneous switching noise (SSN), which is a combination of delta-I noise in power distribution network (PDN), return current sharing common path, and reflected and coupled noise in IO networks. In addition to increased noise generation, signal level and supply voltage continue to decrease. If uncontrolled, SSN can cause logic circuits to falsely switch state or cause an increase in circuit delay.

Field-programmable-gate-array (FPGA) devices offer large number of I/Os as a competitive feature. Designing a FPGA package that generate very low noise on the power and ground structure, in the presence of a larger number of simultaneously switching I/Os is becoming ever challenging for high-performance CMOS FPGA to ensure optimized system performance and cost. To fulfill this goal, in-depth understanding of mechanisms contributing to power ground noise is imperative.

This paper presents a study to the causes of SSN in FPGA package by means of system simulations. Measures that potentially mitigate the noises are discussed. The outline of discussion is as follows:

- In the first part of paper, a package model including PDN and I/O is extracted by use of commercial available field solver tools.
- System simulation that includes CMOS drivers, I/O traces, and PDN is performed. Simulated SSN noise is correlated to lab measurement to establish confidence to the validity of package model.
- In the second part of the paper, the aforementioned package PDN model is used as a vehicle to carry out further studies on potential effectiveness of on-package and on-die decoupling capacitance to SSN reduction.
- The paper is concluded with useful package design strategies that promise better power and signal integrity.

It should be noted that this paper considers SSN on the package level with the assumption of idealized PCB board, because high density FPGA packages post the most challenges in the entire application system design.

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Part I

SSN in Package

Two major mechanisms, PDN network inductance and I/O-return path loop inductance, contributes to SSN generation. As illustrated in Figure 1, simplified PDN net is represented by Lpwr, Lgnd, and Cpkg. The signal I/O trace consists of characteristic inductance Lsig and capacitance Csig. There exist inductive and capacitive coupling of different level between each nets.

As commonly acknowledged, inductance is associated loop structure that current flows. As a result, SSN is best described inside current flow loops that couple to each other inside a high-density package.

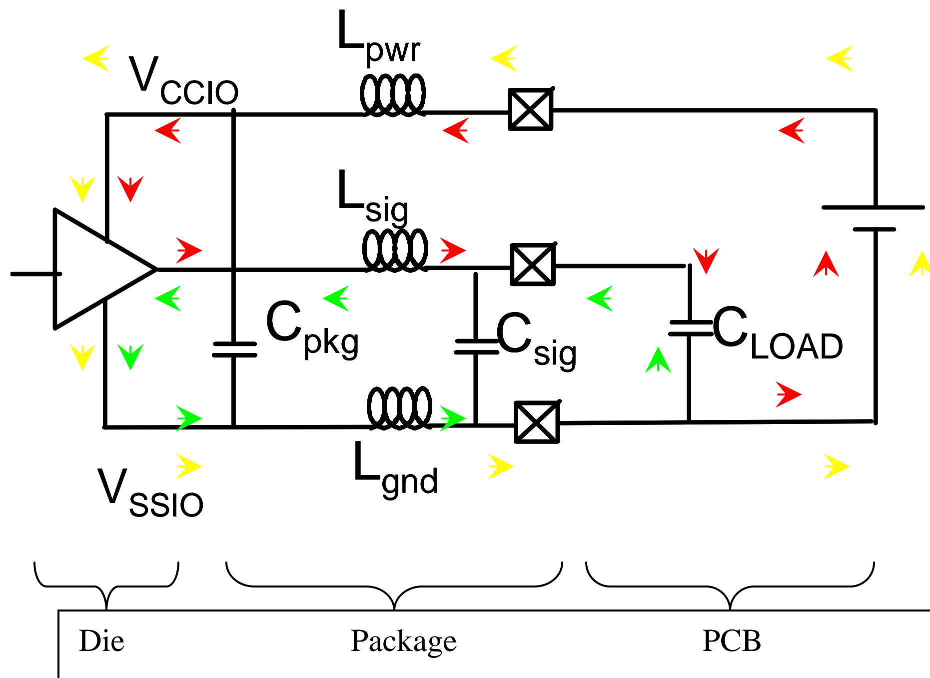


Figure 1: Simultaneously switching noise in FPGA package

When signals switch from low state to high state, pull-up device turns on and pull-down device turns off. Current starts to source from VCCIO. The red current loop is formed to supply charges from power supply to the die. Due to the inductance associated with power rail, Lpwr, charges can not reach device instantaneously owing to current chock. A voltage drop occurs at VCCIO governed by the relationship of V=Lpwr*di/dt. When signal switch from high to low, pull-up device turns off and pull-down device turns on. Current on I/O sinks into VSSIO and form green loop. The same Lgnd*di/dt rule applies

and causes ground potential increase, or ground bounce. Both voltage and ground potential variations are often referred as switching noise.

It is worthy noting that CMOS device brings in use of power and ground net at different time events. In an ideal situation, the upper device is on at the moment signal rise above threshold voltage. At the same instance lower device is shut off. In reality, there is a short period of time that both devices remain on in the transition region. During the period, a low impedance path is formed directly between VCCIO to VSSIO. As a result, a surge current, often referred as crossbar current, passes both devices and flows through the loop in yellow color. The crossbar current generates voltage droop and ground bounce directly from power and ground loop at every edge that input signal transitions, independent of I/O nets.

The magnitude of inductances in each loop is related to it loop structure that encircles magnetic fields created by current flowing on the loop. Large loop will generate high loop inductance so loop structure must be careful designed. Power and ground should be made as close to each other as possible to minimize loop inductance. As for I/O-ground loop, I/O traces are usually designed with 50 ohm characteristic impedance by balancing inductance and I/O to ground capacitance (Sqrt(L/C)). Thus I/O trace can not be put arbitrarily close to ground. However, any increase of the loop, such as ground cut, will not only causes impedance discontinuity but also increase of loop inductance, which leads SSN noise increase.

A measurement example of ground bounce is shown in Figure 2. Red trace is one of the switching I/Os and the purple trace is representation of VSSIO.

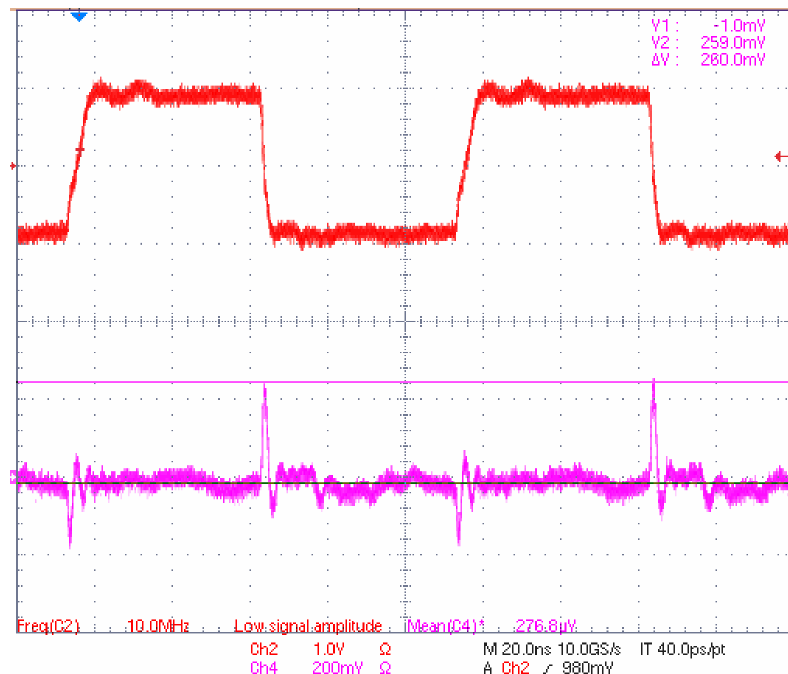


Figure 2: Real world example of SSN (ground bounce in this case)

On the VSSIO trace, one can clearly identify the ground bounce lining up with falling edge (high to low transition) of the signal.

To summarize this section, mechanisms contributing to switching noises on power ground network are briefly introduced. A package design that promise low SSN noise is preferred to have low inductance power and ground plane, impedance well controlled and sufficiently isolated I/O nets, and localized charge pump to supply current surge. Owing to design constrains, there are trade-offs in implementations. The following sections will denote to understandings of design trade-offs with using SSN values as performance figure of merit.

Package Model and SSN Correlation

In this section, a FPGA package model is built and connected to multiple I/O buffers that are simultaneously switching. Since PDN and I/O return effects interacts in SSN generation, a good way to study is to include both in the package model creation. SSN results are then simulated and compared to measurement data collected from a similar hardware bench setup. The purpose is to justify the validity of package PDN model for design feature trade-off studies in the later sections.

Simulation setup is shown in Figure 3. Extracted package model consists of 40 I/O nets and all the power and ground nets. All VCCIO bumps are lumped together as one power port, assuming switching current is uniformly distributed in each VCCIO bump branch. All VCCIO balls are lumped as one port on the far side of the package. Similarly, all VSSIO bumps and balls are lumped, respectively. Reference ground is tied to VSSIO ball port.

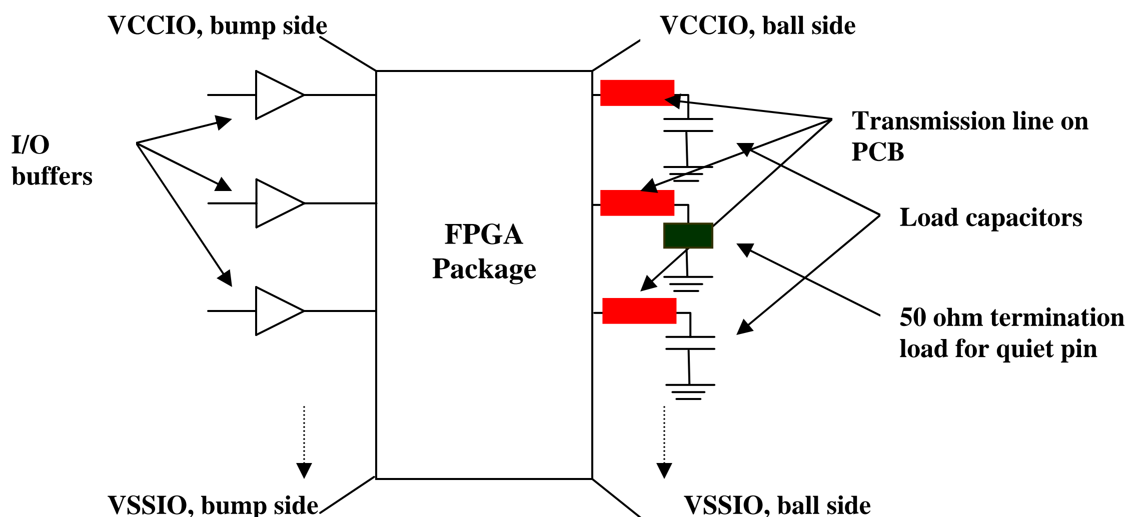


Figure 3: SSN simulation setup. Both PDN and I/O nets are considered

Buffers are tied to I/O ports on the bump side of the package models. On the ball side a short transmission lines of 3 in is connected, and tied to 10 pf load capacitors. The power and ground of the drivers are tied to the bump side VCCIO and VSSIO respectively. A various number of drivers, 10, 20 and 40 are switched simultaneously in a repetitive pattern. The quiet pin that is driven logic low is observed for ground bounce.

Following are the plots for the 10, 20, and 40 drivers switching in the simulation environment.

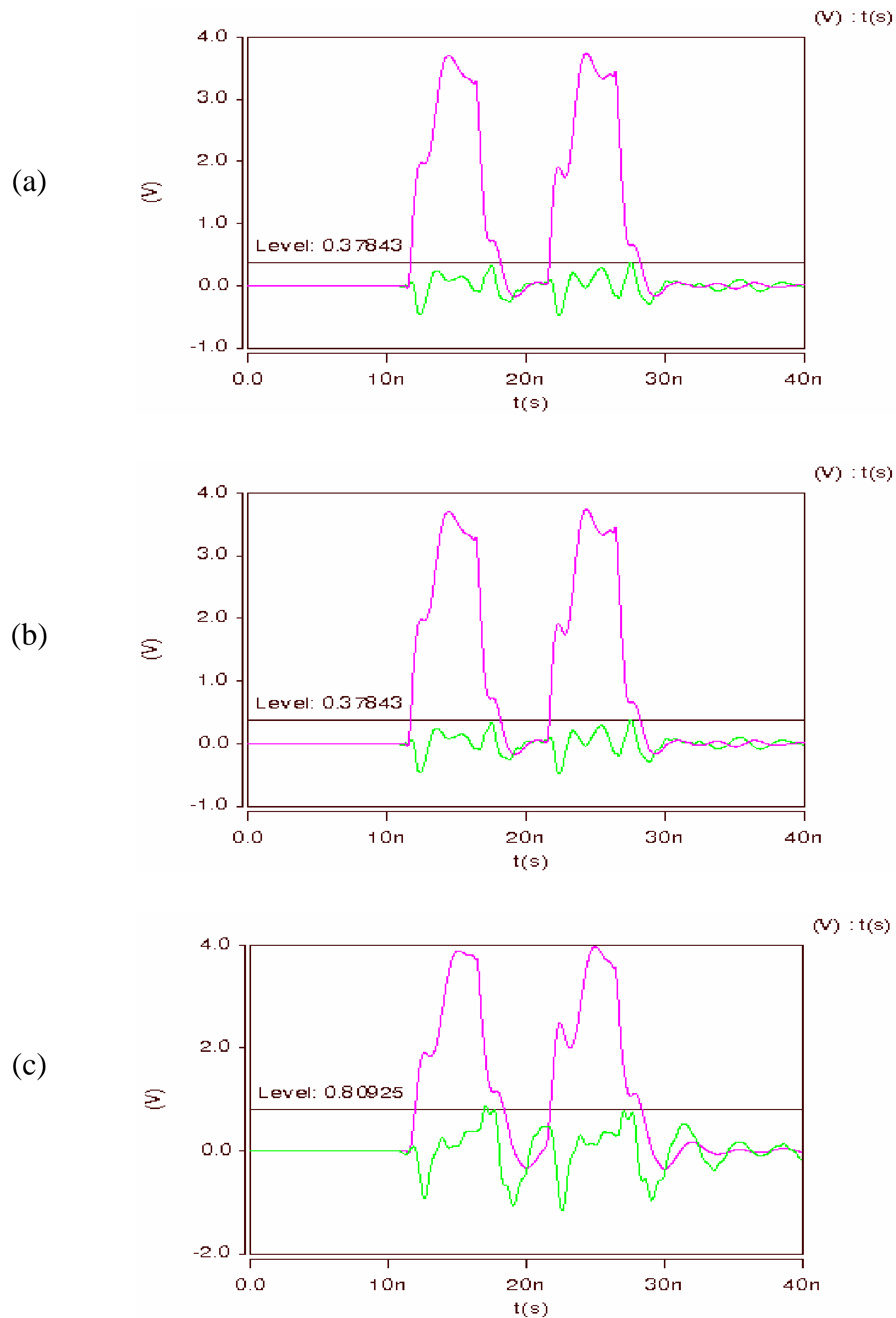


Figure 4: Simulated SSN on ground and switching I/O at load

The comparison to measurement is listed in the following table.

# of I/Os	10	20	40
Ground bounce Simulated (mV)	378	434	809
Ground bounce Measured (mV)	390	470	740

A good correlation is reached between simulation and measurement. From above discussion, the package model is believed to be accurate to a satisfactory degree. Thus it will be used in the following package design feature simulations.

Part II

In the second part, decoupling features are investigated through SSN simulations. Mitigation measures are compared to each other in terms of noise reduction effectiveness. In order to simplify the simulation efforts yet without sacrificing the accuracy, power and ground networks are transformed into a single net by reducing the matrix order of aforementioned PDN. In light of this modification, SSN will expressed in the format of power-ground noise instead of separate voltage droop or ground bounce.

On-Package Decoupling

As described in the SSN introduction section, lack of electrical charges close to buffers to supply fast I/O switching current is the dominate cause to SSN generation. Because of excessive inductance residing on the power ground networks, current can not flow instantaneously from power supply on the PCB through package to the die. Most initial charges needed to facilitate switching current come from parasitic capacitance of the package. In most package designs, parasitic capacitance is not large enough to store enough charges. Consequently, external on-package chip capacitors are often recommended. Nowadays, buffers are often designed with built-in on-die capacitor structures on their internal power buses. The end result of such efforts is the establishment of local charge storage for fast current backup. Also, adding decoupling capacitors can be regarded as forming a smaller current loop local to buffers that minimize the loop inductance in switching.

Firstly, let us examine the use of on-package decoupling capacitor. Multiple vendors supply inter-digital capacitors or LICA type capacitors with capacitance ranging from 100’s nF to a few uF. The salient feature of such chip capacitors is the very low ESL, easily on the order of 10s picohenry. The small ESL makes the chip capacitor self-resonance pushed to beyond the signal spectrum and makes themselves valid candidate in

on-package decoupling. However, the implementation of capacitors on the package can make a difference to the final results.

A typical package substrate is made of a core layer and many much thinner layers built up on each side of the core. Core layer thickness usually dominates the total thickness of package. As a result, core layer carries significant large inductance if paths of VCCIO and VSSIO through the core are not always close coupled. It is the core layer that makes difference to the implementation of on-package capacitors.

Figure 5 shows a frequency domain package PDN impedance profile looking into from the bump side with ball side connected to a DC supply. Capacitor models are added to the package PDN model. As explained at the beginning, this study focuses on package so that the board PDN features is not included in the impedance profile plot. The absence of board effects can be justified by acknowledging PCB structure affects only the low frequency impedance.

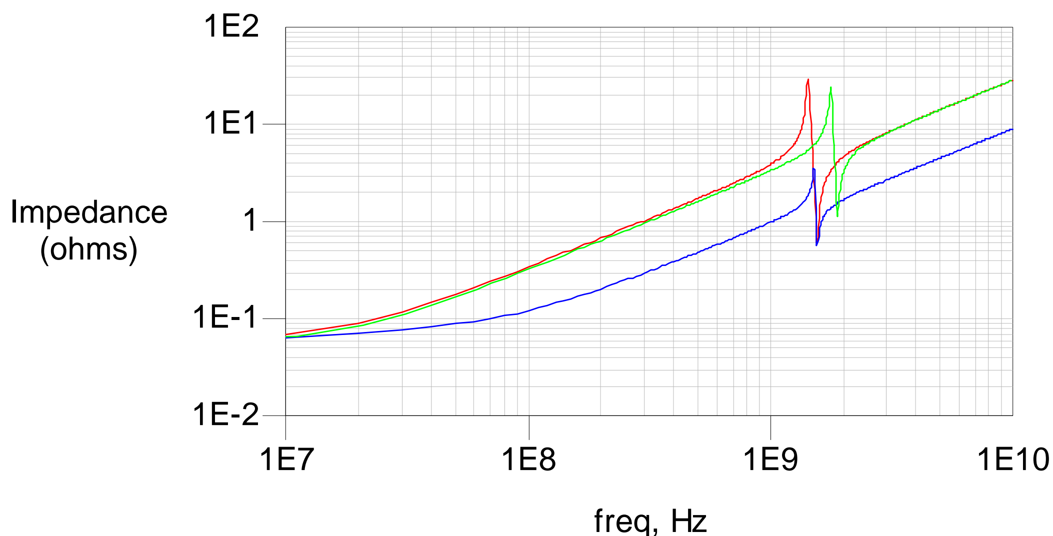


Figure 5: Frequency domain PDN profile with different on-package decoupling capacitors implemented

The capacitor is an IDC 1.5uF chip capacitor with 60 mohm ESR and 50 pH ESL. The red trace is the package without any on-package capacitor. Also shown in the figure are impedance profiles for packages with on-package capacitor connected to its top layer (blue) and bottom layer (green), respectively. From the plot, it is apparent that adding capacitor on power-ground layer below core has little effect in reducing impedance. However, capacitors added on power-ground planes above core reduce package PDN impedance by 2-3 times over most of the frequency range.

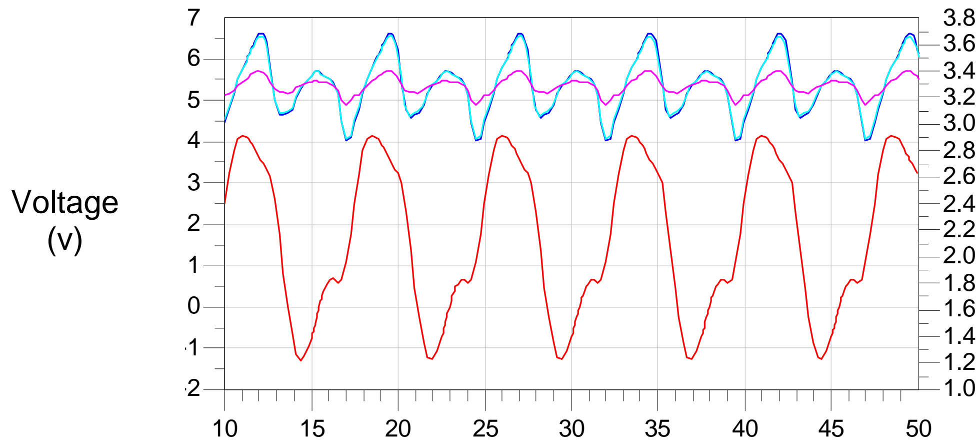


Figure 6: Switching I/O and relative power-ground noise generated in PDNs with different on-package decoupling capacitors implemented

The effectiveness of each on-package capacitor implementation can be best viewed by relative power-ground noise generated when current flow through each PDN configuration, as shown in Figure 6.

In the picture the lower trace is voltage waveform of one of the switching I/Os at load. On the top of plot, there are three traces, original package without capacitor is in blue color, capacitor on bottom power-ground layer is in cyan, and capacitor on top power-ground layer is in magenta. Peak to peak noise is suppressed by roughly a factor of three if capacitors implemented on power-ground plane above the package core.

It should be mentioned that location of capacitor on top layer is not necessarily required to be close to the die, as long as the impedance between die bump to the cap pad is keep low. This is achievable by using power ground planes and well designed escape area next to bumps.

On-Die Decoupling

In on-die decoupling cases, values of on-die capacitor are usually limited because of complexity and required real estate in capacitor implementation. This is especially true for a FPGA device that is designed with maximum flexibility in mind as compared to most application dedicated ASIC device.

In Figure 7, overall impedance profile is shown for a package PDN with on-die capacitor incorporated. The on-die capacitor values range from no capacitance to 4000pF in a step of 500pF, from left to right.

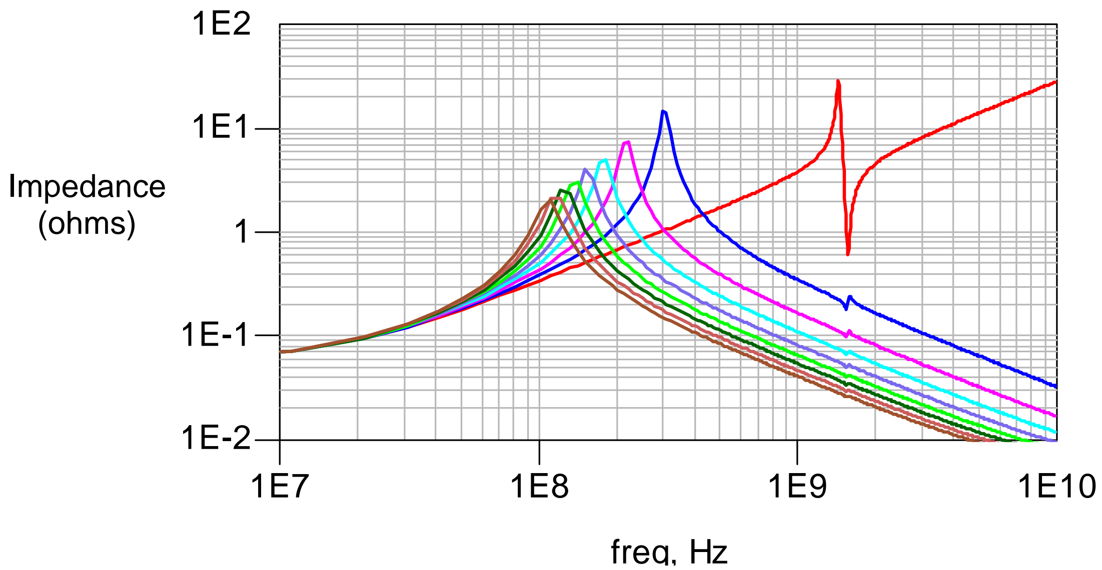


Figure 7: Frequency domain PDN profile with different on-die decoupling capacitors implemented

Resonance is caused by on-die decap and package parasitic inductance. Note that resonance peak value drop steadily with increase of capacitance values. The salient feature using on-die capacitors is that impedance resonance at high frequencies is greatly suppressed.

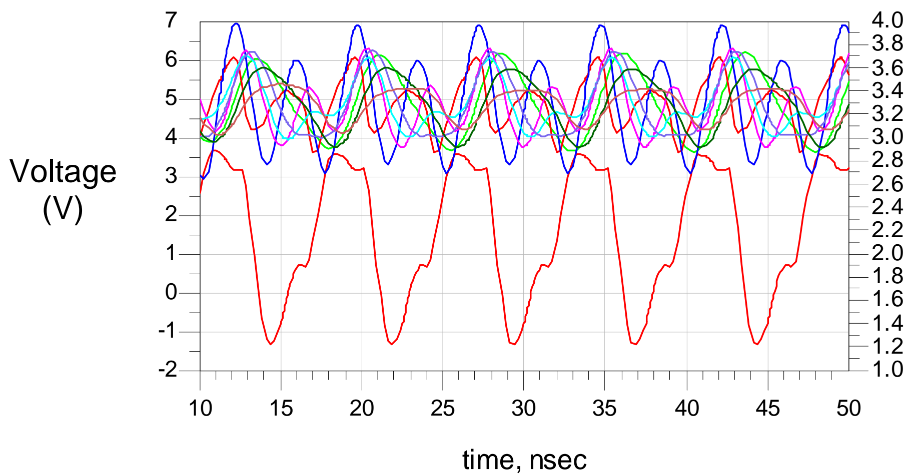


Figure 8: Switching I/O and relative power-ground noise generated in PDNs with different on-die decoupling capacitors implemented

How the combined PDN affect SSN generation. Figure 8 illustrates SSN reduction caused by different on-die capacitance. A tabulated peak to peak noise values is shown in Table 1.

Table 1

Decap Value (pF)	Resonant Frequency (MHz)	Resonant Magnitude (ohms)	Power Rail Noise (volt, p-p)
No cap	1430	29.2	0.85
500	300	14.5	1.26
1000	221	7.5	0.83
1500	181	5.1	0.69
2000	151	4	0.72
2500	141	3.1	0.85
3000	121	2.5	0.66
3500	111	2.1	0.5
4000	101	1.6	0.35

By plotting noise value versus decoupling capacitor, an interesting feature is revealed shown in Figure 9.

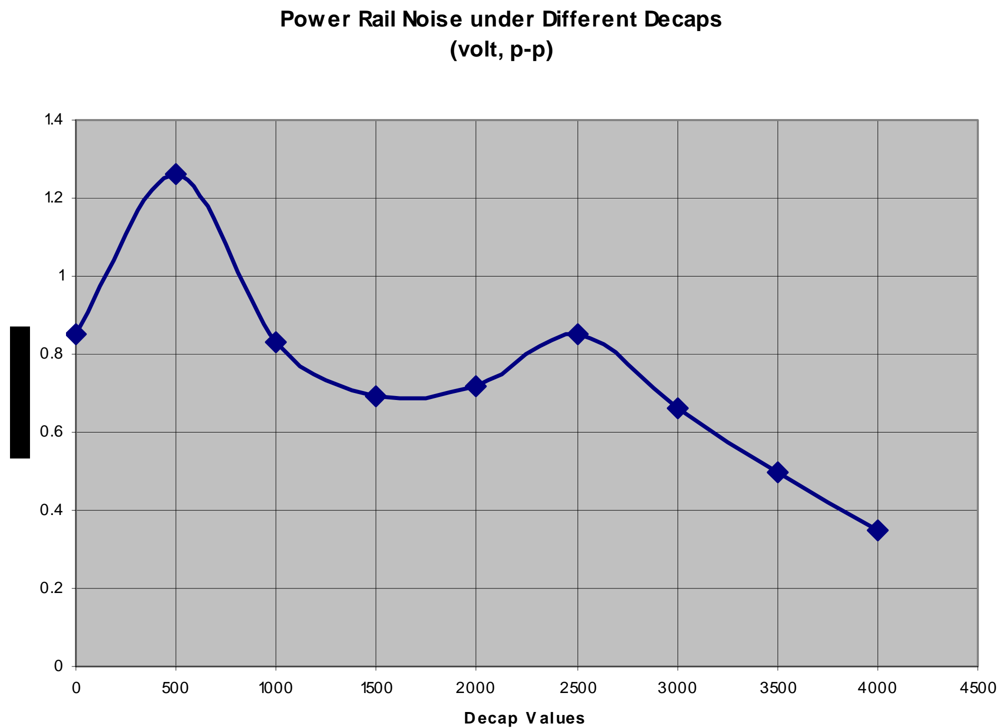
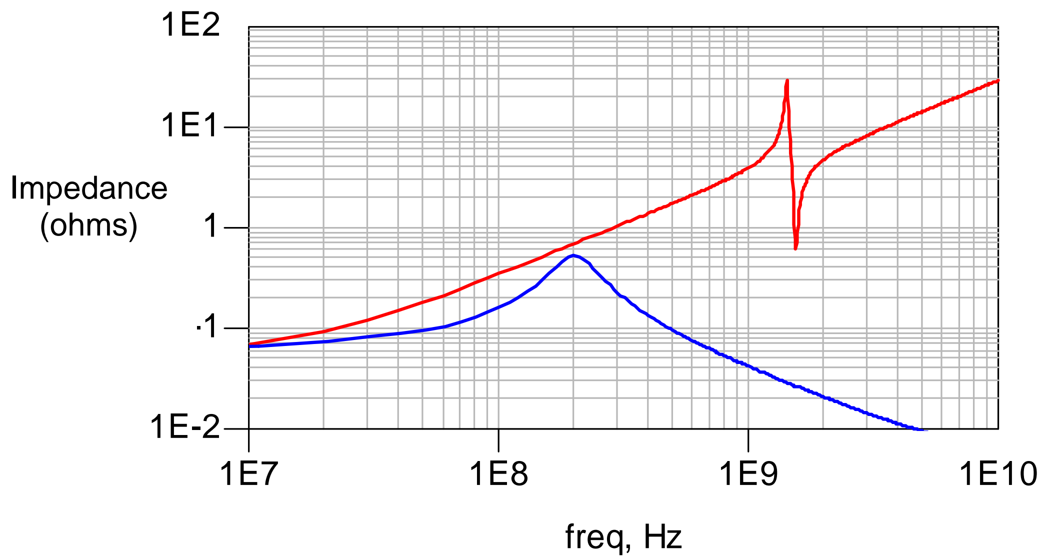


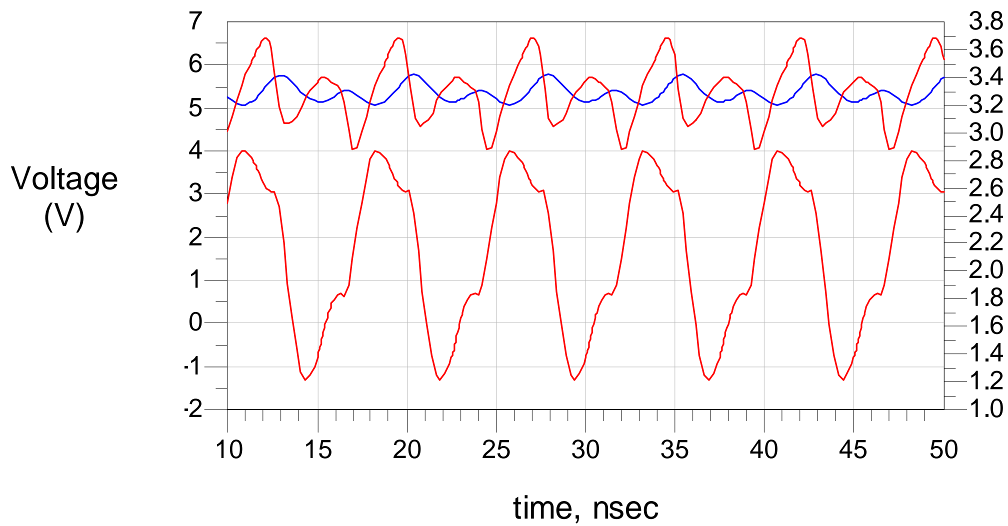
Figure 9: Value of on-die decoupling capacitor on noise reductions

From the trend of peak to peak noise values, it indicates that on-die capacitance should be closely monitored because certain value causes enhancement of noise. For example, use of 2500pF causes noise increase owing to that the corresponding impedance resonance coincides with one of switching current frequency components.

To achieve the best result, both on-package and on-die capacitors should be used with appropriate value and implementation. Use of 4000pF on-die capacitance together with on-package capacitor on top layer of package yield low impedance over entire frequency range, as shown in Figure 10a. The effectiveness of such measure is demonstrated in Figure 10b



(a)



(b)

Figure 10: (a) Frequency domain PDN profile. (b) Switching I/O and relative power-ground noise generated in optimized PDN

Noise Prediction from Stimulus Spectrum

Two observations are made on previous plots. The first observation is that largest noise voltage droop tends to occur along rising edge of the signal in using on-package capacitor, while in on-die capacitor application, droops are lined up with logic high portion of each bit and noise repetitive rate equates to signal frequency (ex. noise waveform in 4000pF case). They can be explained with switching current included into PDN impedance analysis.

Switching current either sources from or sinks to package PDN. The interaction of excitation source with PDN impedance resonance governs many SSN phenomena. By transforming switching current from time domain to frequency domain, a noise spectrum exciting package PDN network is obtained.

In Figure 11, current spectrum is given for I/O buffers employed in this SSN study, which is converted from time domain waveform by Fourier transform. The first spectral line on left is the fundamental frequency, or the data rate of signal. In this case, it is 133MHz. Up to 20 harmonic are included in the spectrum to illustrate spectral energy contributions of each high frequency component that constitutes the fast rising edge of switching current.

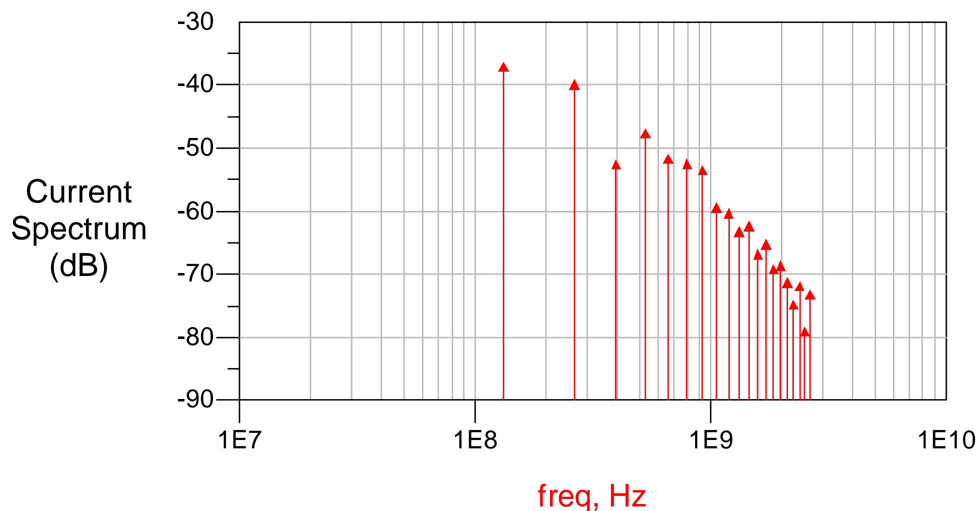
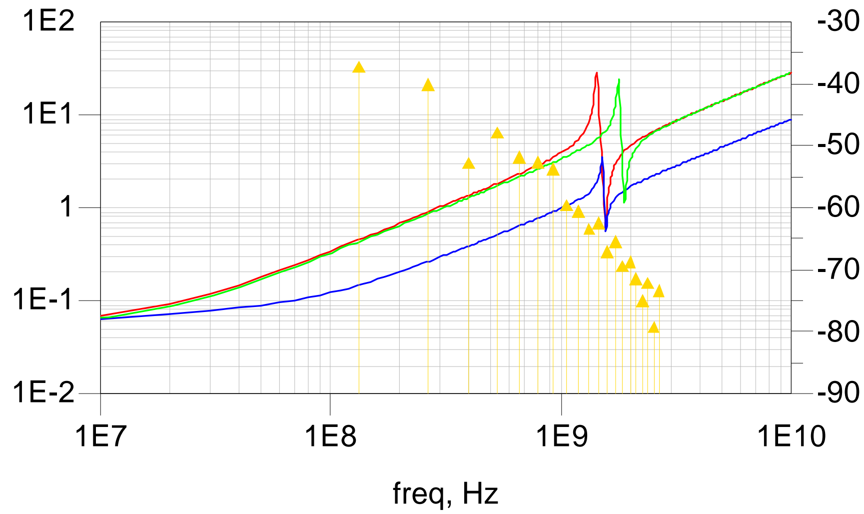
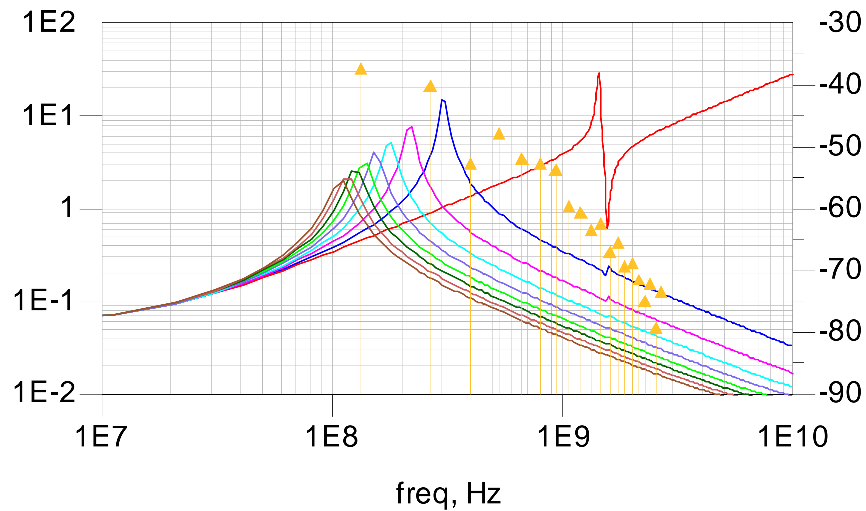


Figure 11: Switching current spectrum signature

If the excitation spectrum is overlaid on package PDN profile, the coincidence of PDN impedance resonance and signal frequency component will tell what to expect for the noise generation. This is done in Figure 12, where the PDN profiles are for on-package capacitor (a) and on-die capacitor (b), respectively.



(a)



(b)

Figure 12: Current spectrum overlaid on PDN impedance profiles with on-package (a) and on-die (b) decoupling capacitors implemented.

It can be seen that most of low harmonics that carry dominant power experience low impedance of PDN. As a result, less noise is generated at these frequencies. On the other hand, frequency location of the strongest impedance peak is lined up with high frequency components of signal. These high frequency components, residing and in phase at transition edge of signal, experience peak impedance and thus large voltage drop. This is why the first observation.

As for the second observation, it can be explained in a similar pattern. On-die capacitor shifts the impedance resonance peak from high frequency to low frequencies that approximating to data rate. The end result is that low spectrum components of signal tends to experience large voltage droop. For example, use of 4000pF has voltage droop at the center of logic high, away from transition edge of each side.

An important observation is made on Figure 9 early on. The fundamental harmonic of signal is underneath impedance resonance peak created by 2500pF. This explains why use of large capacitor value sometimes enhances power noise. As for other combinations of resonance peak and harmonics, relative strength of each must be analyzed in order to decide suppression effectiveness.

Conclusion

A joint study of SSN and I/O return path is presented in this paper by analyzing contribution factors in FPGA package model that includes both PDN and I/O networks. The package model is verified through SSN simulation and correlation to lab bench data. By employing the package PDN model, effectiveness of on-package and on-die decoupling capacitor to noise reduction is analyzed. Explanations to noise feature is given in terms of stimulus current spectrum applying to package PDNs.

It is evident that on-package decoupling capacitor should be implemented on power ground plane above core layer of package to give the best effectiveness. Design emphases should be given to on-die decoupling capacitor values in order to prevent LC oscillation in the vicinity of die-package interface.

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