Simulation Study of Power Delivery Performance on Flip-Chip Substrate Technologies

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Abstract

The input impedance of finite utility plane structures is calculated accurately from the simulated package resonance data using a commercial signal integrity tool. The effect of the equivalent circuit parasitics of the utility planes and their contributions to power integrity are simulated on both, digital and high-speed sections for the same die and package footprint on three different package substrate technologies. In addition, the effective loop inductance and package substrate DC resistance is also calculated from the package input impedance at low frequency range. These results are used to discuss the intrinsic relationships between the physical package structure such as: stackup, utility plane shapes and via types to identify and minimize the potential sources of package utility plane noise for critical applications.

Introduction

The electrical behavior of the power delivery of a package substrate is increasingly being considered as critical in high-speed system performance as devices are becoming more sensitive to the power ground noise from the board and package. Presently, advanced package designers and signal integrity engineers have been focusing on reducing package substrate cost while still maintaining electrical performance and product reliability. In this paper, an attempt is made to understand FCBGA package resonance based on substrate technology that includes package physical design parameters such as: via structures, plane shapes, dielectric constant, stackup & manufacturing design rules from the bump to the ball. The same die and package footprint is used to perform the simulation study of package resonance on three different flipchip substrates. Both, time and frequency domain simulations are performed to determine package level utility plane responses from the die pad (top layer) to the package ball (bottom layer).

Literature survey points to several studies on package parasitic model extraction methods [10] and the degrees of accuracy required to include the effects of package in determining the overall system performance. Several papers have been published on qualitative & quantitative electrical properties of package substrates such as SSN, crosstalk, package resonance, and propagation delay & skew [2-4]. Many books on signal integrity [9, 10] have also addressed the need to quantify accurately electrical performance of package utility planes as an interface between the chip and the board. The referenced books and papers also point to the well-known fact that utility planes in the package are critical to minimize overall system level noise.

The commercial software used for simulation has two types of solvers, one based on frequency domain and the other time domain. PowerSI tool [1] is based on frequency domain electromagnetic simulator with the accuracy equivalent to full wave electromagnetic analysis. The software seamlessly integrates multiple solvers, such as transmission line solvers, full-wave field solvers, and circuit solvers for the simulations. All different solvers are connected to each other using appropriate algorithms to account for the interactions between different geometry features in situations such as a via passing through planes then branching into a trace, or a trace over a plane gap, etc. This hybrid method can provide direct results such as S, Y, and Z parameters at any locations on a package substrate design. In essence, we think this hybrid approach has sufficient and necessary field-solution-based accuracy for signal integrity and power integrity simulations of a package with much improved simulation speed over using the time domain approach. Features of the time domain simulator (SpeedXP) have already been described in the published literature [2] and are used to compute effective loop inductance and DC resistance.

As mentioned earlier, the focus of this study is to understand the relation between electrical properties of various package physical structures and their contribution to package level power/ground plane noise. Therefore on-die parasitics and on-board circuits were not taken into account in the simulations. It is our opinion that this simulation study of package level resonances in different substrate technologies is both informative and educative to understand signal integrity issues related to electronic packages designed for high performance and high frequency applications. This data also helps advanced package designers and physical designers in assessing the merits of substrate technology for package selection since the various structures and routing schemes in the package substrate design are constrained by manufacturing technology.

Simulation Methodology

A 3D full-wave electromagnetic field solution is necessary to determine accurately the equivalent circuit representation of package parasitics for fast rise time, high density and highly sensitive applications. However, it is common knowledge that full-wave 3D solutions require vast computational resources and extremely long CPU run times. Therefore, we had to choose a commercial field simulator that was based on numerical techniques equivalent to the accuracy of full-wave EM solution that requires reasonable computational resources and acceptable simulation run times.

The typical transmission path in the package substrate contains signal traces (with microstrip line, embedded microstrip line or stripline configurations), utility planes (with mesh, part solid or Swiss cheese structure) and vias (blind, buried or through hole). The 3D EM fields generated inside

the multi-layer structures of the package substrate can be solved using modified algorithms (with sufficient & necessary conditions) to full wave numerical techniques to obtain accurate full wave solutions with much improved efficiency in simulation run times. The commercial signal integrity software (PowerSI & SpeedXP) by Sigrity (used in this paper) adopts a hybrid approach in its simulation engine to handle various geometrical structures in the package in determining the equivalent full wave EM solution. Signal traces are modeled with transmission line equations (telegrapher equations) and the numerical method is equivalent to 2.5D MOM. Large conductor shapes such as power/ground planes, ground fills and power islands with mesh are analyzed using full-wave field solvers such as FD, FDTD, FEM, or BEM methods. Small geometry features such as via pad and dogleg holes are treated as lumped circuit networks. Therefore, instead of the whole structure package substrate structure, only the electrically large power/ground planes are numerically discretized. Consequently, different EM numerical techniques have been combined to achieve accurate and more efficient solutions with significantly improved simulation speed.

The native Cadence APD package design databases are converted into *.spd format compatible with Sigrity's PowerSI & SpeedXP tools. This was accomplished with the translator provided in the SpeedXP suite [ref]. A solid plane is added as the last layer to all the original design files to represent the external return in the board. The stackup dimensions, material properties and other related information are directly updated into the *.spd file in the translation process. Also any changes in the material properties and dimensions can be made within the PowerSI/SpeedXP generator module. The stackup layers of all the FCBGA substrate technologies under study are modified to include an external return path for the package in the board. It is assumed that the external plane is located at 500um from the bottom layer of the package and the dielectric constant of the medium between the package and the board is 4.2. Figs 1–3 show the 3D view of the utility plane structures for the substrate technologies named A1, A2 & A3 under study. Table 1 in the next section shows the salient features of each substrate technology. The 3D utility plane structures are the inputs to both SpeedXP and PowerSI tools.

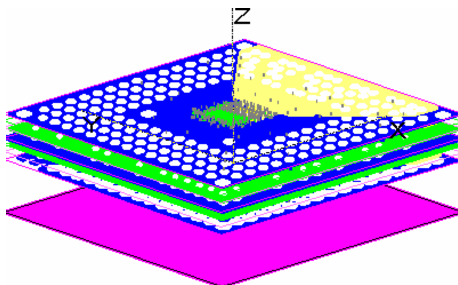

Fig 1. 3D view of the plane structures in Substrate A1

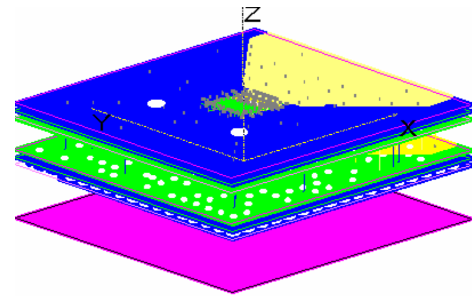

Fig 2. 3D view of the plane structures in Substrate A2

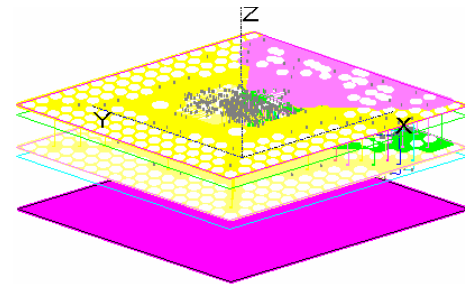

Fig 3. 3D view of the plane structures in Substrate A3

All the VSS and VDD nodes on the top layer are connected to the input port excitation. A 0.01ohm resistor connects all the VSS and VDD nodes on the bottom layer of the substrate. The built-in hybrid field solver takes into account all the electromagnetic field couplings between adjacent signal traces, vertical couplings between the vias and other plane structures. The mesh size for discretization in the simulation is set to 100 X 100. The frequency bandwidth is set to the range: 500Mhz to 4Ghz. The above mentioned connection scheme and input attributes are identically repeated for all three cases under study on both, the digital and high-speed planes individually.

Substrate Technology Features

In this section, various features of the substrate technologies with respect to differences in layer stackup to typical route connections are illustrated and emphasized to interpret the results on package resonance and finite plane inductances. The flipchip package used in this study is a 23mm square with a total ball count of 217. The distribution of the signal and utility planes is shown in Fig 4, which illustrates the package stackup layers. It is clear from the layer stackup that substrate A1 has more metal allocated to the VSS/quiet/ground plane. The other two substrates have VDD and VSS planes distributed on the same layers. The qualitative differences in the plane structures are shown in Figs 1-3, particularly the top plane. Substrate A3 has just a single layer dedicated to signal routing. However, signal traces are not included in the package resonance simulation.

Selected substrate technology attributes (mechanical & electrical properties) of the three technologies under study are tabulated in Table 1. The dielectric constant of the substrate material for A1 is the lowest and that for A2 the highest and has an effect on package capacitance. It is worth noting that the distance between the signal traces and the power planes increases from A1 to A3 (Fig 4 is not drawn to scale, see Fig 5).

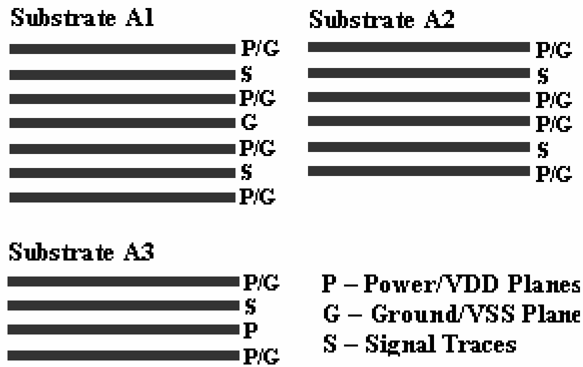

Fig 4. Layer Stackup for the Three Substrate Technologies

Both, substrates A2 & A3 have a thick dielectric core dividing the number of metal layers equally into two halves. In substrates A1 and A2 the signals are in symmetrical stripline configuration (signal traces are equally placed from the top & bottom planes). The signal configuration in substrate A3 is an asymmetrical stripline.

Table 1: Substrate Technology Attributes

Substrate Technology	A1	A2	A3
# of Layers	7	6	4
Dielectric Constant	3.3	4.7	4.2
Core Layer	Metal	Dielectric	Dielectric
Top Plane (Figs 1-3)	Meshed	Solid	Meshed
Metal Thickness	12/18um	15um	15 / 25um
Via Types	Blind &Buried	Stacked, Blind & Buried	Blind/Buried & Through
Signal Trace configuration	Symmetrical Stripline	Symmetrical Stripline	Asymmetrical Stripline
Total Substrate Thickness	0.5mm	0.64mm	0.56mm

The dielectric thickness between consecutive metal layers in A1 is much less compared to the other two substrates. Another differentiating feature in substrate A1 is the Cu core. This metal core is dedicated to ground (VSS) though all the different potential vias (as a result of via stack up limitation in this technology) going through it makes it a Swiss cheese like plane. The more flexible via (including the stacked via) configurations make the power plane connections to the bumps more attractive in the other two technologies (A2 & A3). In all three cases, the top and bottom metal layers are fully or partially dedicated to the ground/VSS plane. There are some direct bump connections to the top VSS plane. In case of the power/VDD plane, the bumps are connected to the inner planes through vias. Each substrate technology uses at a minimum of two via types for connections. The paths illustrated in Fig 5 below indicate a typical route connection to the utility (power and ground) planes. Only substrate A3 uses through vias for some connections (not shown below).

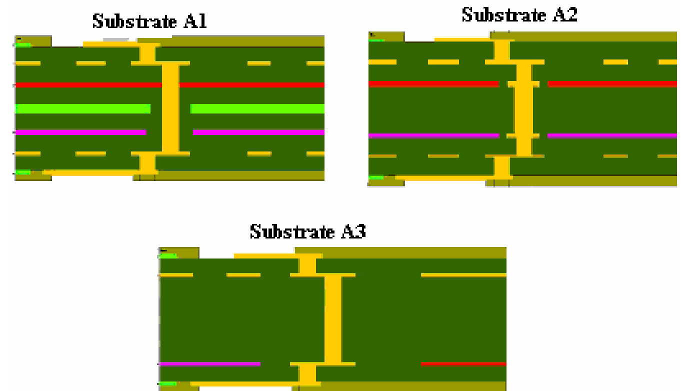

Fig 5. A typical route connection to Utility planes in each Substrate Technology

Results & Discussions

Input impedance and package resonances (Figs 6 & 7) of the complete utility plane structures are simulated for both, digital and high-speed sections for all the three different substrate technologies discussed in the above sections. The effective loop inductance for frequencies < 1Ghz and DC resistance for digital and high-speed planes are tabulated below in Table 2. Based on the computed effective loop inductance, substrates A1 and A2 have comparable noise contributions due to finite digital and high-speed plane inductances and substrate A3 is less favorable. However, substrate A3 has better DC noise in comparison to A1& A2. Therefore, the choice of package based on these two variables depends on other factors, since the application is the same.

Table 2: Effective Inductance and DC Resistance

Substrate Technology	A1	A2	A3
Effective Loop Inductance for digital plane (nH)	0.11	0.13	0.14
Effective Loop Inductance for high-speed plane (nH)	0.30	0.33	0.38
DC resistance for digital plane (mohms)	3.0	3.7	1.7
DC resistance for high-speed plane (mohms)	7.6	7.7	4.0

The results in Figs 6 & 7 show that substrate A3 has low input impedance on both the digital and high-speed planes up to 4Ghz. It also shows no resonances on the high-speed plane structure and a small resonance peak at ~3.2Ghz for the

digital plane structure. The dielectric constant of this substrate (A3) is the median value (4.2) with respect to the other two substrates. Substrate A3 consists of several through hole via type connections (not shown in Fig 5). In our analysis, we believe that this connection in substrate A3 contributes to low impedance path with no purely resistive frequencies in the bandwidth of interest (500Mhz to 4Ghz).

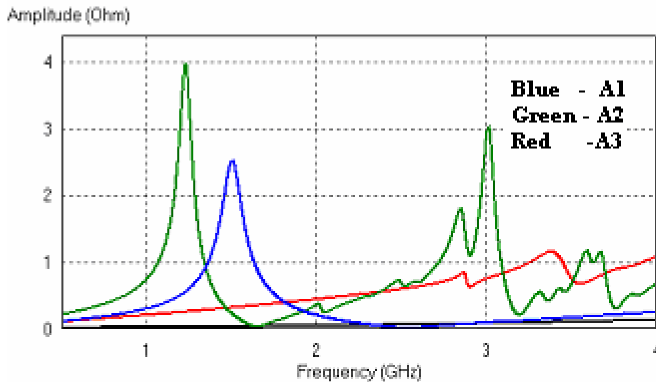

Fig 6. Input Impedance and Package Resonance for the Digital Section

Substrate A2 shows sharp resonances on both the plane structures. The prime factor for the increased number of these resonances in substrate A2 in comparison to substrate A1 is related to the path traversed from bump to ball (Fig 5). The physical length of a typical path in substrate A2 is longest (See Table 1, total substrate thickness) and consists of three different via types leading to multiple reflections at junctions due to impedance mismatches. The other feature that could possible contribute to more resonances on substrate A2 is the solid top plane. Both, A1 & A3 have meshed planes on the top layer and show better resonance behavior.

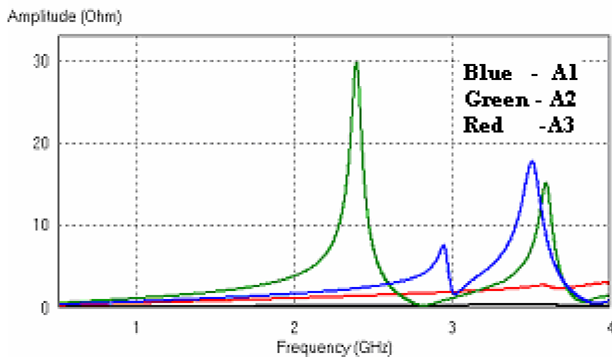

Fig 7. Input Impedance and Package Resonance for the High-Speed Section

The dielectric constant does not show a definitive trend in the package resonance behavior in this study. Substrates A1 & A2 with low and high dielectric constants respectively show many resonances. However, the number of metal layers is a factor in contributing to package resonance. Both, A1 & A2 with almost the same number of metal layers and more metal area designated to power/ground planes contributes to more resonant modes in the equivalent complex distributed plane circuit. The same package footprint on all the substrate technologies could be the factor in masking the effects of other substrate technology features such as type and thickness of the core and metal thickness.

Conclusions

In this simulation study, the package utility planes are characterized to determine the frequency bandwidth of the package footprint in different substrate technologies for the package substrate only. The package resonances are effected by on die capacitances and are not included in this paper. We presented package resonances for digital and high-speed planes as well as low frequency effective loop inductance and DC resistance for these planes.

Advanced package designers can use this data for improving utility plane routing, to get insight to the sources (substrate technology features) contributing to utility plane noise and as a guide to package selection. Chip & system level designers can use this information in estimating the application bandwidth of the package substrate technology and effect of on die decoupling capacitors. In addition, this data can be used as an alternative approach to reducing SSN levels in the package by reducing the input impedance at the resonant frequencies.

Acknowledgments

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