Power Delivery System Performance Optimization of A Printed Circuit Board with Multiple Microprocessors

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1. Introduction

The design of a noise-free power delivery system (PDS) to supply large amount of power at low voltages to multiple microprocessor systems that are operating at very fast slew rate with large dynamic load and high clock frequency is a challenging task. The printed circuit board with multiple power/ground planes are commonly used in the PDS for high performance multiple microprocessors based communication system. In general, a high-performance power delivery system consists of voltage regulator modules (VRM), multi-layer printed circuit board (PCB) with necessary decoupling capacitors (DECAPS) placed on board, microprocessor packages with or without on package DECAPS mounted, the microprocessors with on-die interconnects and the die capacitance. High-speed digital devices, such as the microprocessors that are operating at low power supply voltages and high clock frequency with fast switching currents will induce mid and high frequency noise [1] into the system due to the power ground input impedance associated with the power delivery loop through the package and the board. For a poorly designed PDS, the power ground noise voltages generated in the PDS due to microprocessor IC circuits switching will exceed the maximum allowed noise voltage margins. As a result, this will eventually reduce the maximum operating frequency of the high-speed system. At the same time, as the signal transmission paths share the same PDS environment, the power ground noise will also be coupled into signals transmitted inside the PCB and package. Therefore, it is imperative to accurately model and efficiently simulate the PDS for designing the resonance free PDS with flat or close to flat power ground input impedance over a sufficiently wide frequency range. As DECAPS are commonly used on PCBs and packages to eliminate the impedance resonant peaks and lower power and ground input impedance, to efficiently select the optimum number and types of DECAPS is a critical issue in the noise free PDS design with reduced manufacturing cost and fast design cycle.

This paper presents a simple and efficient simulation and analysis methodology for designing a noise free PDS from VRMs to on-die circuits of multiple microprocessors on a multi-layer PCB. First, by using an available frequency domain full wave electromagnetic field solver, for example [2], network representations of the PCB and the packages are generated. The frequency domain network characterization through the full wave electromagnetic field solver takes into account the electromagnetic field properties and the interactions, such as the coupling, between different components inside the PCB and the packages. These network models are then assembled together for evaluating the power ground input impedance at different microprocessor locations on the board. The combined power delivery model is also used to evaluate the effectiveness of different DECAPS placements on the PCB. Different VRM models, package models, or the on-die interconnect models can also be substituted easily in the composed power delivery model for fast and accurate "what-if" analysis. Therefore, the methodology described in this paper allows fast and accurate modeling and design for optimizing the performance of a PDS. While the analysis methodology described in this study is similar to [3]-[4], it has the advantage of combining the detailed modeling and accuracy of a full wave electromagnetic field solver with integrated capability of SPICE electrical simulation.

Section 2 focuses on power delivery system modeling. A real PCB is used as an example to illustrate the modeling procedure of the network representation. Different package models can be generated by the same procedure. A method of synthesizing a behavioral model of VRM from the measured or simulated input impedance characteristics data supplied by VRM vendors is also presented. DECAPS are modeled simply based on the specifications from vendors. Section 3 mainly focuses on the input impedance analysis. Two approaches are used for the power ground input impedance computation: by using ABCD-matrix cascading and by using Z-matrix connection. The two approaches are described briefly in section 3.1 and section 3.2 respectively. Section 4 presents simulation and analysis results. Different DECAP placements are tested and the power ground input impedance at different places, such as, on PCB at multiple microprocessor locations, before or after the package model, and at the die side looking into the package terminals, are compared. Transfer impedances are also calculated so that the noise coupled between different microprocessors is also studied. Time domain simulation results are also presented to...
provide further visual information about the performance of
the PDS.

2. Power Delivery System Modeling

Figure 1 shows a generalized power delivery system commonly used in a high-speed digital system. It contains VRM, multi-layer PCB, packages, on-die interconnections, and a number of decoupling capacitors mounted on board or on package.

Figure 1. A generalized PCB power delivery system.

Figure 2 illustrates a block diagram of a generalized PDS model. The multi-layer PCB is a critical part of the PDS system for the noise free power delivered to the IC-circuits of microprocessors. A multi-port network generated by an available full wave electromagnetic field solver or through lab measurements usually can represent it. The VRM can be represented by a simple, one-port lumped circuit model which is especially sufficient for the PDS design for the mid and high frequency range. In later part of this section, a method of synthesizing a VRM model from its frequency response characteristics will be described. The DECAPS are modeled traditionally as a one-port series RLC network with specifications provided by vendors. A more accurate DECAP model can be generated through lab measurement. Two-port networks represent the microprocessor package and the on-die interconnection respectively. Both the package and the on-die interconnection models can also be generated by a full wave electromagnetic field solver or through lab measurement.

For the purpose of demonstrating the PDS design and optimization methodology for reducing core power/ground noise, a ten-layer printed circuit board with four microprocessors mounted on bottom and two VRMs mounted on top of the PCB is used as an example in this paper. The stackup information of the 12-inch by 12-inch, 10-layer system board with 6 signal layers, two power planes and two ground planes is shown in Figure 3. Figure 4 shows the two similar power islands on layer 9 of the system board for power supply from one VRM to a pair of microprocessors. Figure 4 also illustrates the locations of four wire bonded TBGA packaged microprocessors mounted on the bottom and the locations of two VRMs mounted on the top of the board.

Figure 3. System board stackup

Figure 4. Power plane shape on layer 9 of the system board

Figure 5 shows the details of the PDS model feeding power to the pair of microprocessors through a power island on layer 9 of the board. This model is used for one simulation analysis study based on the methodology presented in this paper. The DIE-model for the microprocessor core in Fig. 5 is represented by a grid resistance and a current source with the chip capacitance across it. The current source in the die-model represents the dynamic load variation in the microprocessor core circuitry. A simple RL circuit represents the package and the on-die interconnection of the microprocessor. A full wave electromagnetic field solver is used for the computation of the multi-port network parameters to model the PCB. The series connection of $C_b$, $R_b$, and $L_b$ represents the lumped circuit model for the on board DECAPS at the output of the VRM.
A simple approximated lumped model of VRM, which is sufficient in the initial design phase of the PDS, is also shown in Figure 5 [5]. The lumped model consists of an ideal voltage source and four passive elements. The values of these passive elements can be found from the frequency domain output impedance characteristics of the VRM, generally provided by the vendors. As shown in Fig. 6, the output impedance magnitude curve of a typical VRM in the low frequency range can be considered as the impedance of the inductance through which the current ramps up in the VRM, such as a buck regulator. Similarly, the impedance of the filter capacitor and its ESR at the output terminals of the VRM dominates in the frequency range beyond the response time of the feedback loop. Therefore, the value of the inductance \( L_r \) and capacitance \( C_r \) can be obtained from the inductive portion in the low frequency range and capacitive portion in the frequency range beyond the resonance peak of the impedance magnitude characteristics of the VRM. By reading the resonant frequency \( f_o \) from the impedance magnitude plot, value of resistance \( R_r \) can be found from \( Q = \frac{R_r}{2\pi f_o L_r} \). Typically the value of \( Q \) for a parallel R-L-C circuit can be assumed as 0.707. The output impedance at frequency \( f >> f_o \), the crossover frequency of the feedback loop, can be assumed as the parallel combination of \( R_r \) and the ESR, \( R_d \) of the capacitor \( C_d \). Therefore, knowing the value of \( R_r, R_d \) can be found from a point in the flat portion of the impedance magnitude plot, in the high frequency range above \( f_o \).

### 3. Impedance Analysis Methodology

A good power delivery system should provide low enough input impedance to the IC devices of the microprocessor. Two approaches are used to compute the input impedances in the PDS of a PCB system. One approach is based upon using the cascaded ABCD-matrices of the components in the PDS system and the other approach is using the combination of the Z-matrices of the PDS components. In the ABCD-matrix cascading approach, the multi-layer printed circuit board, together with a certain number of decoupling capacitors and the VRMs mounted on board, is modeled as a two-port network. For each port, a package model, which is also a two-port network, is cascaded. Next, beyond the package model, an on-die interconnection considered as a two-port network is also cascaded on. The cascaded configuration of the PDS is shown in Figure 7.

![Figure 7. ABCD-matrix cascading approach](image)

A second approach for the input impedance analysis, based on the Z-matrix representation of the PDS components, is proposed to efficiently perform the "what-if" analysis for different types of packages, DECAPS, and VRMs mounted on the PCB. In this approach, the printed circuit board is modeled as a multi-port network. Some of the ports are connected with DECAP model or a VRM model. The remaining ports are connected with a two-port package network system and beyond that, an on-die interconnect two-port network is cascaded. Figure 8 shows the configuration.

![Figure 8. Z-matrix connection approach](image)

The different ABCD-matrices shown in Figure 7 or the impedance matrices shown in Figure 8 can be easily
assembled together as a hybrid power delivery model by matrix manipulation. Then, the power and ground input impedance at the package or die of a microprocessor can be obtained from the resultant ABCD or Z matrix of the hybrid system. This hybrid modeling methodology takes into account the interaction of the electromagnetic field between different components of the PDS, without increasing the overall complexity of the power delivery model. By using these hybrid modeling approaches, following “what-if” analysis are efficiently performed:

(i) Self power and ground input impedance of the PCB (with and without DECAPS) looking into either at the microprocessor locations with and without microprocessor package, as well as, with and without on-die interconnections.

(ii) Transfer power/ground impedance of the PCB (with and without DECAPS) between any two microprocessor locations, from the microprocessor package, or from the die side.

Two computation approaches of self-input impedances and transfer-impedances for different configurations of the PCB including the microprocessor on-die interconnections, packages and DECAPS are described next.

### 3.1 Impedance Analysis Using ABCD-matrix

The computation of self-input and transfer impedances using ABCD-matrix approach is described in this section for a PDS with two microprocessors mounted on the PCB, as shown in Figure 5. Assuming that a Z-matrix parameter ($Z_{11}$, $Z_{12}$, $Z_{21}$, and $Z_{22}$) is obtained from the frequency domain computation of a printed circuit board by using a full wave electromagnetic field solver. The corresponding ABCD-matrix parameter can be computed as

$$A_{pcb} = \frac{Z_{11}}{Z_{21}}, \quad B_{pcb} = \frac{Z}{Z_{21}}, \quad C_{pcb} = \frac{1}{Z_{21}}, \quad D_{pcb} = \frac{Z_{22}}{Z_{21}}$$

where, $Z = Z_{11}Z_{22} - Z_{12}Z_{21}$.

Considering identical microprocessors, the ABCD-matrix parameters for the microprocessor package and the core/die can be computed from their lumped circuits shown in Figure 5 as

$$A_{pkg1} = A_{pkg2} = 1, \quad B_{pkg1} = B_{pkg2} = R_{pkg} + R_{grid} + sL_{pkg}, \quad C_{pkg1} = C_{pkg2} = 0, \quad D_{pkg1} = D_{pkg2} = 1$$

$$A_{die1} = A_{die2} = 1, \quad B_{die1} = B_{die2} = 0, \quad C_{die1} = C_{die2} = sC_{chip}, \quad D_{die1} = D_{die2} = 1$$

Assuming the ABCD matrices for the PCB, package and die stages of Figure 7 as $[T_{pcb}]$, $[T_{pkg1}]$, $[T_{die1}]$, $[T_{pkg2}]$ and $[T_{die2}]$; the ABCD matrix of combining the muP1-PKG stage and PCB can be found as

$$[T_{die1(pkg1_pcb(pkg2_pcb)}] = [T_{die1}] [T_{pkg1}] [T_{pcb}] [T_{pkg2}]$$

Finally, the muP1-DIE, muP1-PKG, PCB, muP2-PKG and muP2-DIE stages can be combined as

$$[T_{die1(pkg1_pcb(pkg2_die2)}] = [T_{die1}] [T_{pkg1}] [T_{die2}] [T_{pkg2}]$$

Notice that the order of multiplication of the matrices must be the same as the order in which the two-port networks shown in Figure 7 are cascaded.

The self-impedance of the PCB looking from the location of the two microprocessors is given by

$$Z_{pcb_{-}muP1} = \frac{A_{muP}}{C_{pcb}}, \quad Z_{pcb_{-}muP2} = \frac{D_{muP}}{C_{pcb}}$$

The transfer impedances looking from the location of the microprocessor 1 and 2 can be found as

$$Z_{pcb_{-}muP1_{-}muP2} = \frac{A_{muP}D_{muP} - B_{muP}C_{muP}}{C_{muP}}$$

Assuming $A_{pkg1_{-}pkg2}$, $B_{pkg1_{-}pkg2}$, $C_{pkg1_{-}pkg2}$, and $D_{pkg1_{-}pkg2}$ as the elements of the $[T_{pkg1_{-}pkg2}]$ matrix, impedance characteristics at the muP1-PKG and muP2-PKG respectively, can be obtained as

$$Z_{pkg1} = \frac{A_{pkg1_{-}pkg2}}{C_{pkg1_{-}pkg2}}$$

and

$$Z_{pkg2} = \frac{D_{pkg1_{-}pkg2}}{C_{pkg1_{-}pkg2}}$$

Considering $A_{die1_{-}pkg2_{-}die2}$, $B_{die1_{-}pkg2_{-}die2}$, $C_{die1_{-}pkg2_{-}die2}$, and $D_{die1_{-}pkg2_{-}die2}$ as the elements of the $[T_{die1_{-}pkg2_{-}die2}]$ matrix, impedance characteristics at the muP1-DIE and muP2-DIE respectively, can be obtained as

$$Z_{die1} = \frac{A_{die1_{-}pkg2_{-}die2}}{C_{die1_{-}pkg2_{-}die2}}$$

and

$$Z_{die2} = \frac{D_{die1_{-}pkg2_{-}die2}}{C_{die1_{-}pkg2_{-}die2}}$$

### 3.2 Impedance Analysis Using Z-matrix

The computation of the self-input and transfer impedances using Z-matrix approach is described in this section for an n-port PDS as shown in Figure 8. Assuming that $[Z]_{n*n}$ is the impedance matrix obtained from the full wave electromagnetic field solver, with $np$ as the number of microprocessor ports, and $nt$, as the number of termination ports, such as DECAPS and VRMs. Notice that $n$, $np$ and $nt$ satisfy $nt + np = n$. The impedance matrix $[Z]_{nxn}$ can be grouped as

$$[Z_{11}]_{nxn} [Z_{12}]_{nxn} [Z_{21}]_{nxn} [Z_{22}]_{nxn}$$

where $n = 1$ for 2 microprocessors.
Considering the termination conditions of the DECAPS and VRMs mounted on the PCB, the impedance matrix corresponding to microprocessor ports only, can be calculated as

$$Z_{\text{micro}}^{-1} = Z_{11} - Z_{12}(Z_{22} + Z_t)^{-1} Z_{21}$$

(15)

where $Z_t$ is the termination matrix.

Next, considering that each microprocessor port is connected with a 2-port network, such as a package as shown in Figure 8, which can be described as

$$
\begin{bmatrix}
\tilde{I}_1 \\
\tilde{V}_{2,k}
\end{bmatrix} =
\begin{bmatrix}
\tilde{z}_{11} & \tilde{z}_{12} \\
\tilde{z}_{21} & \tilde{z}_{22}
\end{bmatrix}
\begin{bmatrix}
\tilde{I}_k \\
\tilde{V}_{1,k}
\end{bmatrix}
(k = 1..np)
$$

(16)

The final impedance of the PDS, consisting of the multilayer printed circuit board model, with models of different DECAPS, VRMs, and packages, can be calculated as

$$Z = \tilde{z}_{11} - \tilde{z}_{12}(\tilde{z}_{22} + \tilde{z})^{-1} \tilde{z}_{21}$$

(17)

where $\tilde{z}_{11}$, $\tilde{z}_{12}$, $\tilde{z}_{21}$, and $\tilde{z}_{22}$ are matrix composed by the matrix entries from equation (16).

One can see that this approach is more generalized than the first ABCD-matrix approach. In ABCD-matrix approach, the DECAP models and the VRM models are included in the PCB model before the PCB model extracted. In the Z-matrix approach, the DECAP models and the VRM models are separated from the PCB model. The DECAP and VRM terminations are connected to the PCB model afterwards. Therefore, the second approach provides more flexibility in the impedance analysis.

4. Simulation and Analysis Results

The PDS modeling, simulation and analysis methodology described in sections 2 and 3 has been used to evaluate the impedance characteristics for a number of configurations of the system board whose physical characteristics are shown in Figure 3 and 4. These configurations are different in the number, the size and the locations of DECAPS placed around the microprocessors on the board in order to realize the overall power and ground input impedance close to a specified target impedance over a wide frequency range.

After the impedance matrix with and without DECAPS around each microprocessors is obtained from the frequency domain simulation of the system board by using a full wave electromagnetic field solver, the DECAPs are selected to reduce the resonant peaks of the input impedance. Some of the DECAPS are placed at the specified locations on top layer of the system board as close as possible to the microprocessors. Additional DECAPS are placed on the bottom layer of the system board to lower the impedance close to the specified target impedance over a wide frequency range for reducing the power ground noise. The simulation of the system board by using the full wave electromagnetic field solver were repeated to obtain the Z-matrix at the microprocessor locations with different number and values of DECAPS on top and bottom layer of the board. Then, different self-input impedance and transfer-impedance at different locations are computed by applying the ABCD-matrix approach. The lumped circuit parameters for the computation of impedances are: $C_{\text{chip}} = 50 \text{ nF}$ and $R_{\text{grid}} = 34 \text{ m}\Omega$, $L_{\text{pkg}} = 1 \text{ nH}$ and $R_{\text{pkg}} = 30 \text{ m}\Omega$.

The self-input impedance of the PCB at the microprocessor locations with no DECAPS (the red line) and with five 10 nF DECAPS mounted on top layer of the PCB (the blue line) are shown in Figure 9. The impedance magnitude in red line in Figure 9 shows resonant peaks at 60 MHz, 363 MHz and 554 MHz. In order to reduce the resonant peak at 60 MHz, five DECAPS, each of 10 nF with equivalent series resistance (ESR) of 0.23 $\Omega$ and equivalent series inductance (ESL) of 0.6 nH are placed close to each of the microprocessors on the top layer of the board. The self-input impedance with these five DECAPS around each microprocessors on the top layer, the blue line, is also shown in Figure 9. Notice in Figure 9, that adding five DECAPS at each microprocessor locations on the top layer reduces the impedance peak at 60 MHz with new impedance peaks introduced at 310 MHz and 400 MHz. Also, the resonant peaks in the frequency range from 554 MHz on ward are shifted to higher frequencies with reduced magnitude.

Figure 9. Self-input impedance at the PCB with no DECAPS and five DECAPS on the top of the board

Figure 10. Transfer-impedance at the PCB with no DECAPS and five DECAPS on the top layer of the board
The transfer-impedance of the PCB at the microprocessor locations with no DECAPS (the red line) and with five 10 nF DECAPS mounted on top layer of the PCB (the blue line) are shown in Figure 10. One can see by adding five DECAPS the 60 MHz resonant peak has been eliminated. Below 300 MHz, there are no transfer-impedance resonant peaks.

The self-input impedance observed at the package side and at the die side of the microprocessors, with no DECAPS and with five 10 nF DECAPS mounted on top layer of the PCB are shown in Figure 11 and Figure 12 respectively.

- **Figure 11.** Self-input impedances at package with no DECAPS and five DECAPS mounted on the top of the board
- **Figure 12.** Self-input impedances at die side of the core area with no DECAPS and five DECAPS mounted on board

One can see that there are no resonant peaks beyond 200 MHz in the self-input impedance looking at the die side of the microprocessor core power supply. This is because of the fact that on-die capacitor provides an effective high frequency return path to the IC-circuitry of the microprocessor.

Although the input impedance observed at the die side has no resonant peaks beyond 400 MHz, the self-input and transfer-impedance observed at package and on the PCB still contains resonant peaks around several hundred MHz.

Because the signal transmission system will share the same PCB environment, more DECAPS are added on the system board to reduce impedance peak magnitudes at 310 MHz and 400 MHz. A 270 pF DECAP with ESR of 1.49 Ω, ESL of 0.6 nH and with self-resonant frequency at 395 MHz is selected to reduce the resonant peaks at 310 MHz and 400 MHz.

The magnitude of the self-input impedances at the two microprocessor locations on the board, with four, eight, and sixteen 270 pF DECAPS mounted on the bottom layer of the board, in addition to the original five 10 nF DECAPS mounted on the top layer are shown in Figure 13.

- **Figure 13.** Self-input impedance at the PCB with five DECAPS on the top layer and four, eight or sixteen DECAPS on the bottom layer of the board

Notice that 4 DECAPS, each of 270 pF on the bottom layer of the system board significantly reduces the impedance peaks at 310 MHz and 400 MHz. The impedance peak at 154 MHz introduced due to the addition of 270 pF DECAPS can be reduced by using a 1 nF capacitor with ESR of 0.69 Ω, ESL of 0.9 nH and self-resonant frequency at 167.8 MHz.

Figure 14 shows the self-input impedances with five 10 nF DECAPS on the top layer, plus four 270 pF DECAPS and two or four 1 nF DECAPS on the bottom layer of the board.

- **Figure 14.** Self-input impedance at the PCB with five DECAPS on the top layer and four, six or eight DECAPS on the bottom layer of the board

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Figure 15 shows the self-input and transfer-impedances at the microprocessor locations on the PCB with five 10 nF DECAPS on the top layer plus four 270 pF and two or four 1 nF DECAPS on the bottom layer of the board. The self-input impedance resonant peaks below 800 MHz are reduced significantly due to additional DECAPS on the bottom layer of the board.

Figure 15. (a) Self-input and (b) Transfer impedances at the PCB with five DECAPS on the top layer and four, six or eight DECAPS on the bottom layer of the board

The self-input impedances at the package and at the die side of the microprocessors with five DECAPS on the top layer and four, six or eight DECAPS on the bottom layer are shown in Figure 16.

Figure 16. Self-input impedances at (a) the package and (b) the die side of the microprocessors with five DECAPS on the top layer and four, six or eight DECAPS on the bottom layer

5. Time Domain Simulation Results

The time domain simulation of the PDS model shown in Figure 5 is performed using the SPICE integrated capability of a time domain full wave field solver [6]. The PDS model was simulated considering the on-die capacitance, $C_{\text{chip}}$ of 40 nF, the on-die interconnect resistance of 30 m$\Omega$, the package resistance $R_{\text{pkg}}$ of 25 m$\Omega$, and the package inductance of 1 nH. The current source waveform of 300 MHz for the time domain simulation with rise and fall time of 0.1 ns is shown in Figure 17.

Figure 17. Time domain current source waveform

For the core current shown in Figure 17, the time domain simulation results for the voltages at the PCB, package and die with five DECAPS of 10 nF each on the top layer, plus four DECAPS of 270 pF each and two DECAPS of 1 nF each on the bottom layer of the board is shown in Figure 18. Notice that the voltage deviation at the PCB is 3.7% of the 2 V whereas the voltage deviation at the die is 5.2%.

Considering a 0.9 amp current source of 300 MHz with rise time of 3.3 ns and fall time of 0.33 ns, as shown in Figure 19, the transient voltage at the PCB and at the die are obtained, as shown in Figure 20. The transient voltages with no DECAPS on the board and with five DECAPS of 10 nF each on the top layer, plus four DECAPS of 270 pF each and two DECAPS of 1 nF each on the bottom layer of the board show the effect of decoupling capacitors in reducing the voltage droop.

Figure 18. Core noise in the PDS of Fig. 5

Figure 19. Time domain current source waveform
6. Discussions and Conclusions

Based on a network representation of different components used in a PDS, an efficient simulation and analysis methodology for optimizing the PDS performance of a system board mounted with multiple microprocessors has been presented in this paper. The method provides a capability of fast, accurate modeling of the physical structure and efficient computational algorithm for performance optimization of a PDS. Two matrix computation schemes are used for the input and transfer impedance analysis of the PDS. Simulation results are presented for different configurations of the PCB that are efficiently obtained by using one of the analysis method described in this paper.

Further work will be focused on accurately predict the selection of DECAPS and the locations on a PCB.

7. References