

Transient Current Extraction from Time Domain Voltage Measurement

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Abstract

An easy method to extract the current signature of a core power supply is suggested and used to obtain the transient current during HRESET of a microprocessor system.

Introduction

Noise mitigation is an increasingly difficult problem as device circuitry becomes more dense and power demand increases. A simultaneous switching event in the core logic can cause a large transient current demand in modern microprocessors. This current will cause large voltage deviations even when flowing through a small impedance. The noise voltage can cause functional failures, decreased performance, and EMI related issues in a system. To properly design a power delivery system (PDS) including board and package effects this worst case current demand, the current signature, must be known to accurately calculate the target impedance of the system.

To meet the current demand while providing a stable voltage it is critical to design a low impedance PDS across a wide frequency range. Many papers describe how to design such a low impedance PDS [1]. To calculate the target impedance the current signature and the acceptable voltage fluctuation, typically 5%, must be known. The current signature is often difficult to obtain. It cannot be directly measured because high-performance PDS contain boards and packages with multiple power and ground planes, numerous decoupling capacitors of various values, and hundreds of connections at the interfaces between die and package as well as between package and board. Measuring the current at any given point may not be representative of the current signature.

An alternative to measuring the current directly is to measure the impedance of the PDS and the voltage at the interface of interest and then calculate the current signature [2-4]. The method used in [2] relies on a lumped element circuit to represent the distributed effects of the board and package PDS, the lumped model is derived from parameter extraction procedure using resonance measurements with a network analyzer. With modern electromagnetic simulation tools such as SPEED2000 the impedance measurement of the PDS can be eliminated, replaced by a simple time domain simulation. Also the complex distributed effects of today's PDS's can be considered without having to reduce to a lumped model.

This paper will discuss a method for easy extraction of the current signature for an integrated circuit (IC) device. The method will be introduced and applied to a PowerPC based microprocessor to extract the current signature during an HRESET event.

Methodology

Figure 1 is a block diagram of the PDS for a device. Currents I_c and I_{pkg} are critical parameters for package/board designers to determine whether the power supply system meets performance requirements. The difficulty of a direct measurement of I_c and I_{pkg} lies in the fact that these currents are distributed. I_{pkg} , for example, goes through all the power and ground solder balls of the package. Indirect measurements [2-4] involve measuring voltage and impedance in an appropriate frequency range.

Our current signature extraction method is a hybrid of measurement and simulation. With our method, voltages V_c , V_{pkg} , and/or V_{brd} are measured using an oscilloscope, but the impedance of the power supply system (package and board) is simulated using software tools such as Speed2000 from Sigrity. Speed2000 is a tool that provides fast and accurate full-wave electrical analysis of IC packages and printed circuit boards. The advantages of this method are: 1) it's easy to implement; 2) it doesn't assume any lumped circuits for the power distribution system; 3) it accurately considers the distributed effects.

Currents I_c or I_{pkg} can be extracted using this method. To extract I_{pkg} , voltages V_{pkg} and V_{brd} are measured simultaneously with two channels of an oscilloscope, and they are used as voltage sources to stimulate the printed circuit board with all the decoupling capacitors in Speed2000. I_{pkg} in time domain is the simulated current going out of the voltage source at the solder balls. Measuring V_c at the die pads (wire bonding pads or flip chip bump pads) is needed to extract I_c . For die-up wire bonding devices, measuring V_c is very easy, but for die-down flip chip devices, a designated voltage sensing pair routed to board is a good way for such measurement.

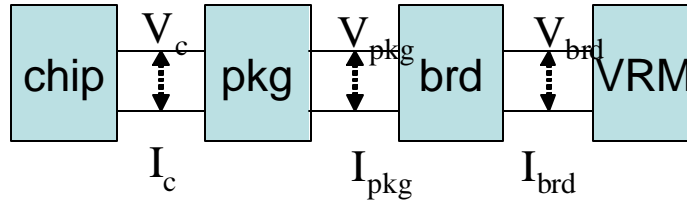


Figure 1. Block diagram of a power delivery system (PDS).

Application

This method was used to extract the current signature of a PowerPC based microprocessor system. The microprocessor runs at 1.4GHz and is housed in an eight layer ceramic ball grid array package. The package has 24 decoupling capacitors, of which 18 are for core power supply decoupling. To verify that Speed2000 could accurately simulate the impedance of such multi-layer structures, the impedance of the package was measured using a network analyzer and also simulated with Speed2000. The results are shown in Figure 2. Very good agreement was displayed up to GHz frequency range.

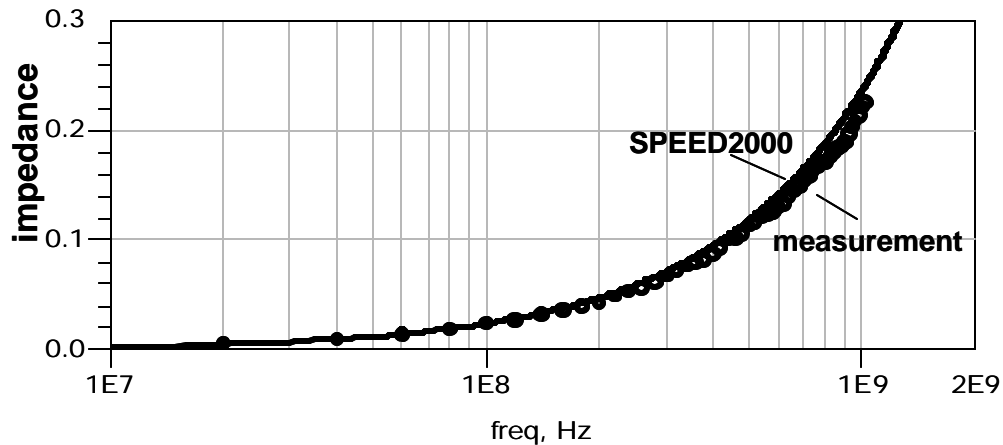


Figure 2. Measured and simulated power supply impedance of the microprocessor package. Impedance is in Ohm.

The package is soldered to a multi-layer board with many decoupling capacitors, and its core power is supplied by a voltage regulator, as shown in Figure 3. In this application, core supply current I_{pkg} at the interface between the package and the board was extracted, and the examined event was HRESET deassertion.

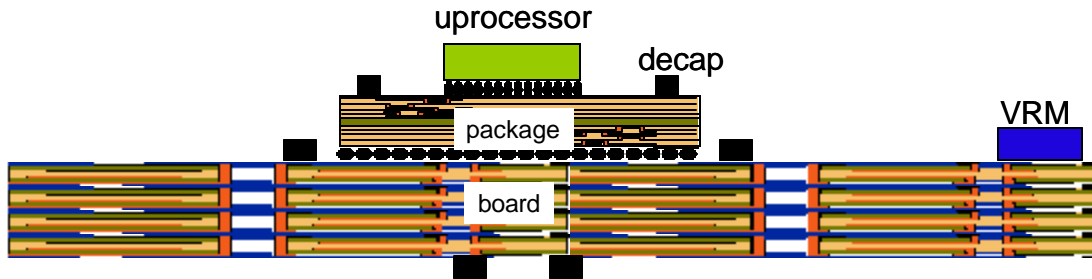


Figure 3. Schematic of the PDS for the PowerPC based microprocessor system.

An Agilent Infiniium 54850 oscilloscope and high impedance probes were used to measure voltages. Since VDD and GND pins were located in the center of the ball array, the voltage V_{pkg} could not be measured at the solder balls. V_{pkg} was instead measured at two locations, one directly underneath the package on the bottom side of the board and the other at a decoupling capacitor site on the package. The two voltages were found to be equal during HRESET, and one was used for V_{pkg} . V_{brd} was measured at the voltage regulator. An HRESET event consists of two steps (Figure 4): assertion and deassertion. When HRESET is asserted, the microprocessor stops functioning and supply current goes to zero, this zero current point was used to calibrate the DC level of the simulated results. A deassertion occurs $\sim 200\text{ms}$ later in this device, this long time assures that all decoupling capacitors are charged to their DC voltage, which will be the initial states of the capacitors in later Speed2000 simulations. V_{pkg} and V_{brd} were measured while deasserting HRESET. Details of V_{pkg} are shown in Figure 5.

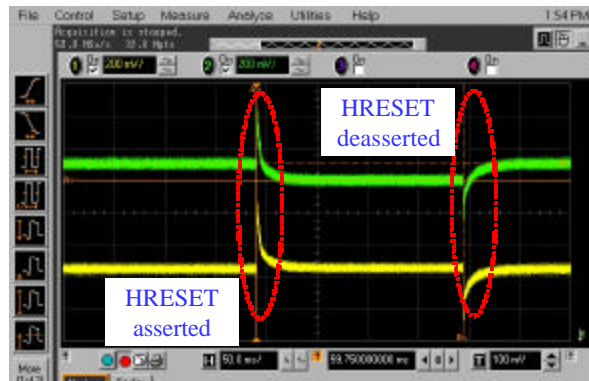


Figure 4. Measured voltage while HREST. Two V_{pkg} are equal as discussed in the text.

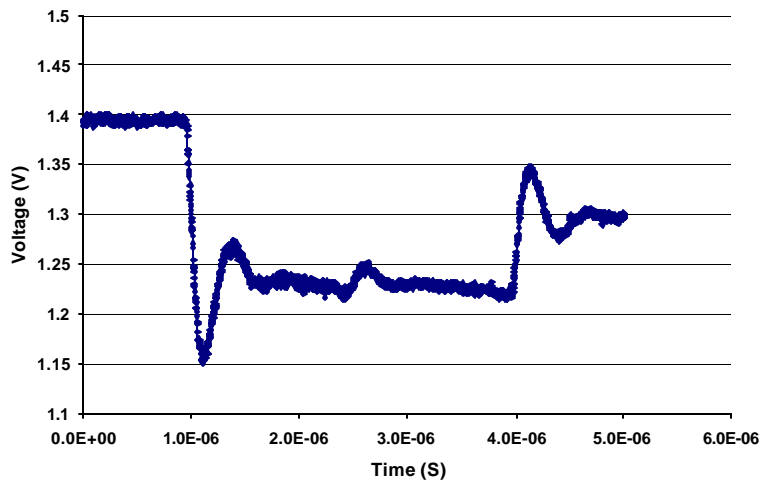


Figure 5. Measured V_{pkg} while HRESET is being deasserted.

The board and all the decoupling capacitors with proper ESL/ESR values were imported to Speed2000 and the measured voltages were then used as the stimuli at the respective locations. Initial DC analysis was enabled to obtain the correct initial states of decoupling capacitors. The simulated time-varying current through the source at the package pins, the current signature, is plotted in Figure 6. At first the current rises sharply with a maximum transient current rate of ~ 0.12 A/ns. It reaches and stays at a maximum current of ~ 19 A for $1.5\mu\text{s}$ and then decreases. The high current demand occurs during built-in self test (BIST).

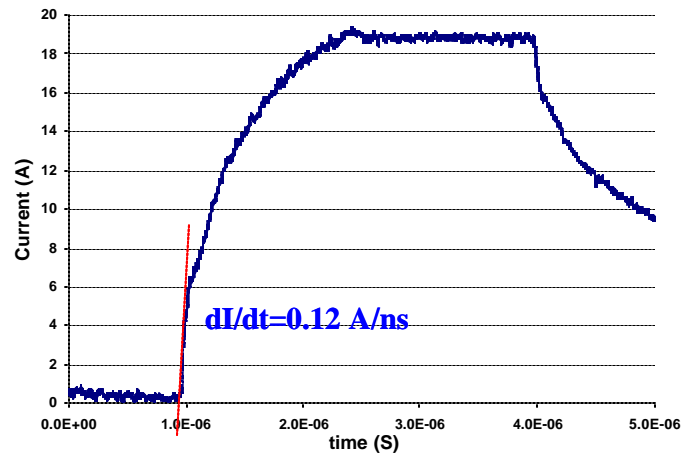


Figure 6. Simulated transient core power supply current at solder balls while HRESET is being deasserted.

Summary

A hybrid method involving voltage measurement and Speed2000 simulation is suggested to extract current signature of power supply. This method is very easy to implement and accurately considers distributed effect of the power supply system. It's used to extract the current signature of a PowerPC based microprocessor system during HRESET and reasonable results were demonstrated.

Reference:

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- [2] Z. Chen, B. Young, and N. Pham, "Norton Equivalent Modeling Of Microprocessor Core Noise From Measurements," in *Proc. EPEP 1998*
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