



Power Delivery System Performance Optimization of a Printed Circuit Board with Multiple Microprocessors

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PURPOSE:

- Describe **PDS** (**P**ower **D**elivery **S**ystem) Modeling and Simulation Methodology for
Reduced Core Noise, Using a
System Board with Multiple Microprocessors
- Describe an algorithm developed for **Input Impedance Computation** at different Microprocessor locations on the System board
- **Recommend** – An Efficient Design Methodology for Improving the performance of the PDS of a **Microprocessor System**

PDS Design is Critical, as

Fast transient current of large magnitude due to **Switching Core logic circuits at High Frequency** with **Fast slew rate** and **at Reduced Voltage**

→ Transient voltage drop across the PDS-Impedance

(PDS-impedance → Loop inductance and Resistance associated with Power and GND path)

→ Less voltage available to the Microprocessor Core

→ Reduces the Maximum Operating frequency of the Microprocessor

CORE-PDS

(Power/Current distribution path to deliver power to Core/Die)

consists of

⇒ VRMs,

PWR-GND planes of PCB and Packages

Via-BGA distribution, and

On-Die Interconnects

- Impedance of the **CORE-PDS** increases with frequency
- **PDS-impedance** should appear as a **low impedance path from source to load over a wide frequency range (dc to several clock cycle)**
- **Ideally, PDS-Impedance should be = Target Impedance**

• Target impedance:
$$Z_{\text{target}} = \frac{xV_{\text{dd}}^2}{P_{\text{av}}} = \frac{xV_{\text{dd}}}{I_{\text{av}}}$$

⇒ A figure of merit, used to realize PDN-impedance over a wide frequency range

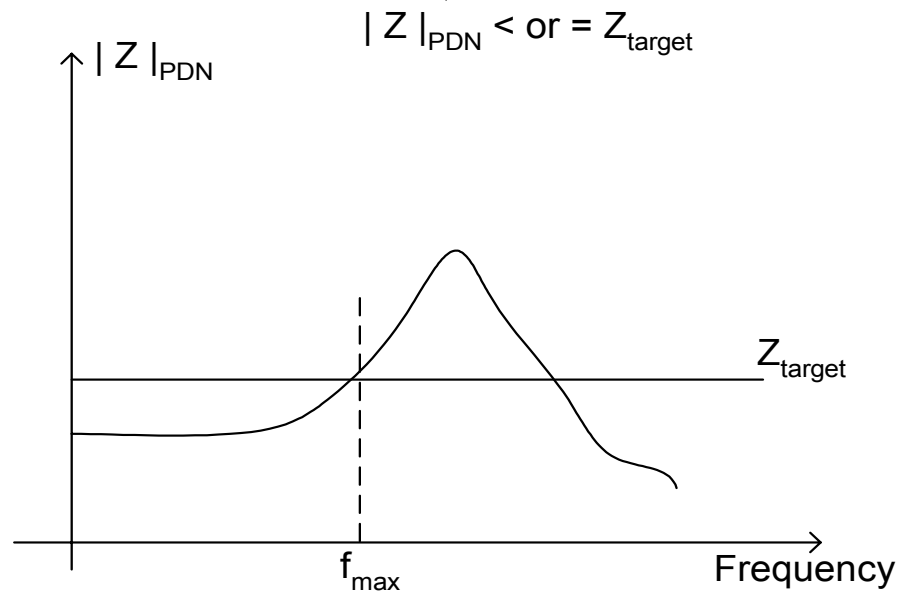
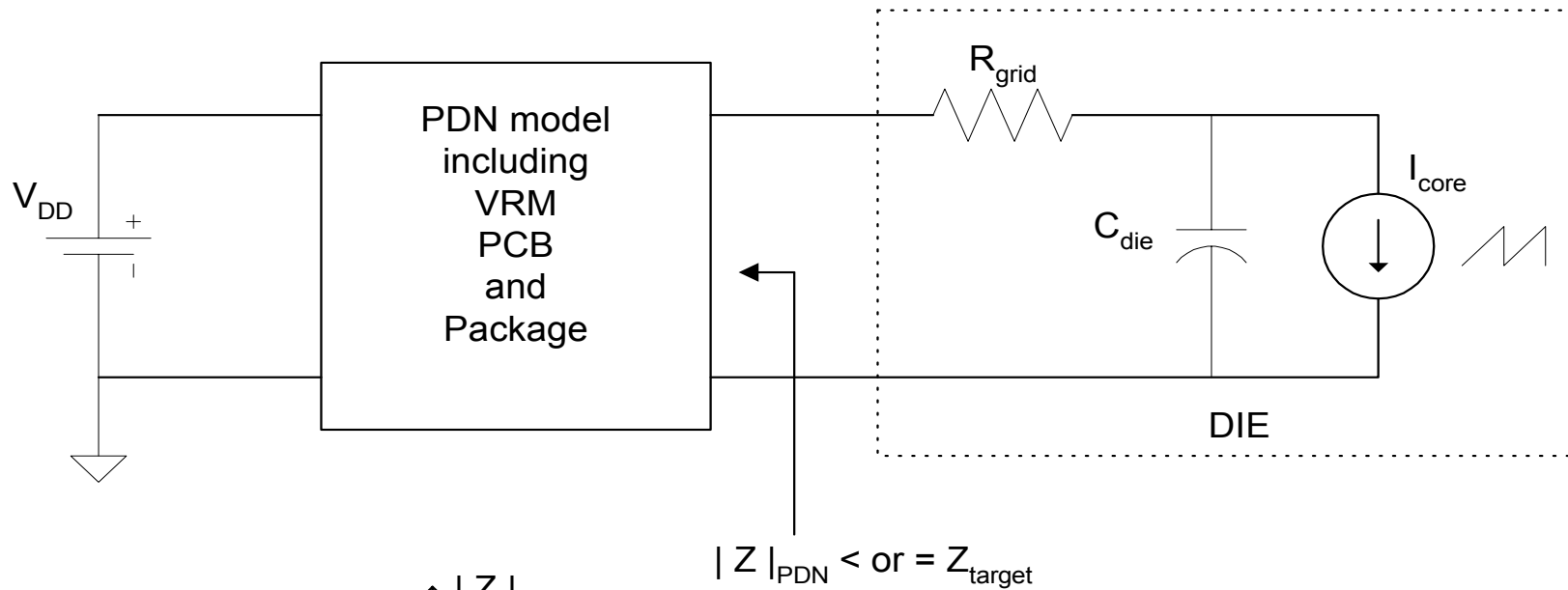
V_{dd} ⇒ Nominal/Operating voltage

x ⇒ % Ripple

xV_{dd} ⇒ Allowed ripple voltage (5 - 10% of V_{dd})

P_{av} ⇒ Average power associated with the device

I_{av} ⇒ Average current associated with the device



Adding

A number of higher-valued DECPAS for low-impedance in the low frequency range + A number of lower-valued DECAPS for low impedance in the high frequency range

==> An optimal way to realize the

PDS-impedance = Target Impedance

However,

Resonance conditions in the System can exist such that the DECAPS can worsen the PDN-impedance for some frequencies

Next,

Modeling,

Simulation

and

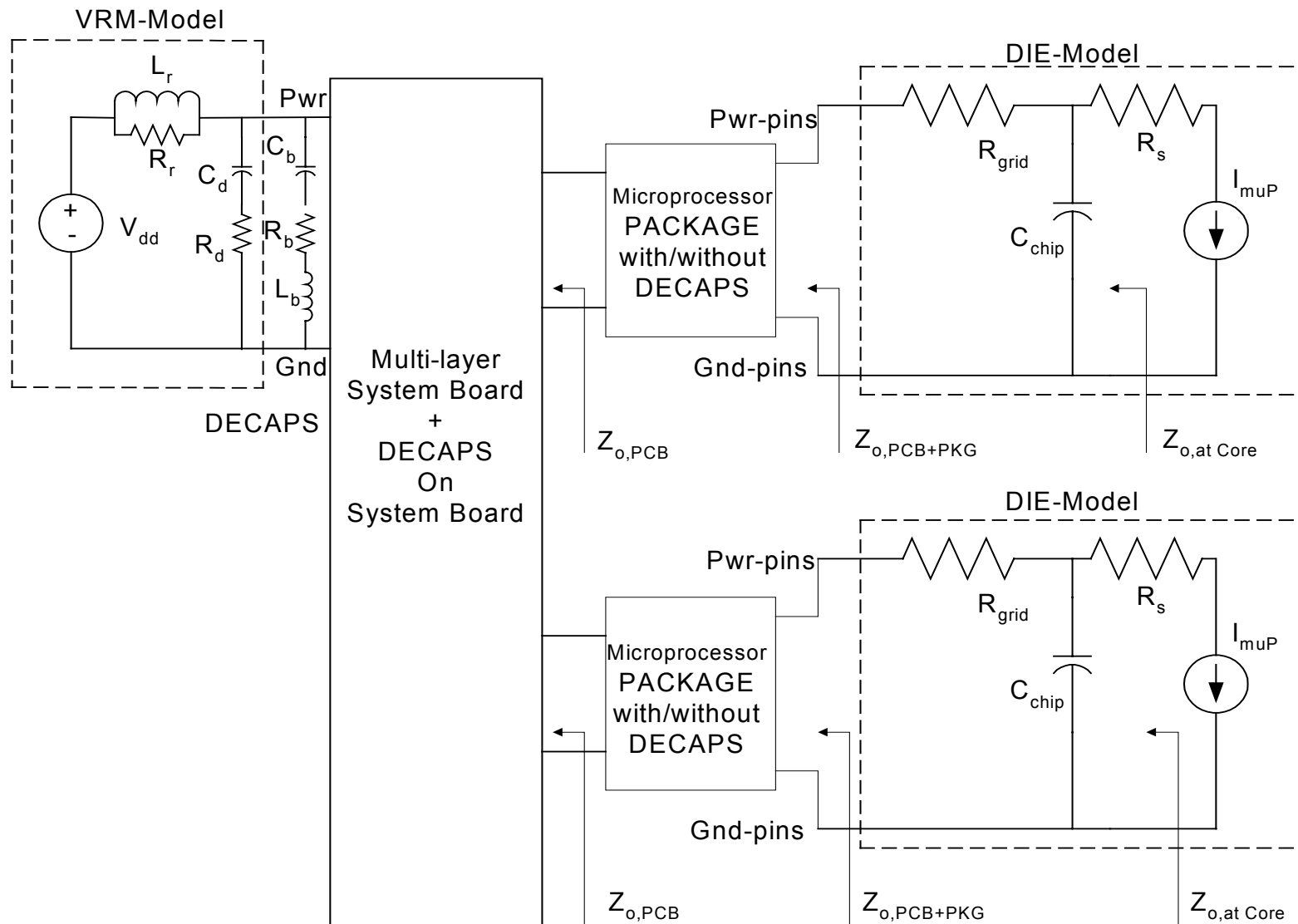
Analysis

For

**Core Noise Performance Optimization of a Printed
Circuit Board (PCB) with Multiple Microprocessors**

(as an example)

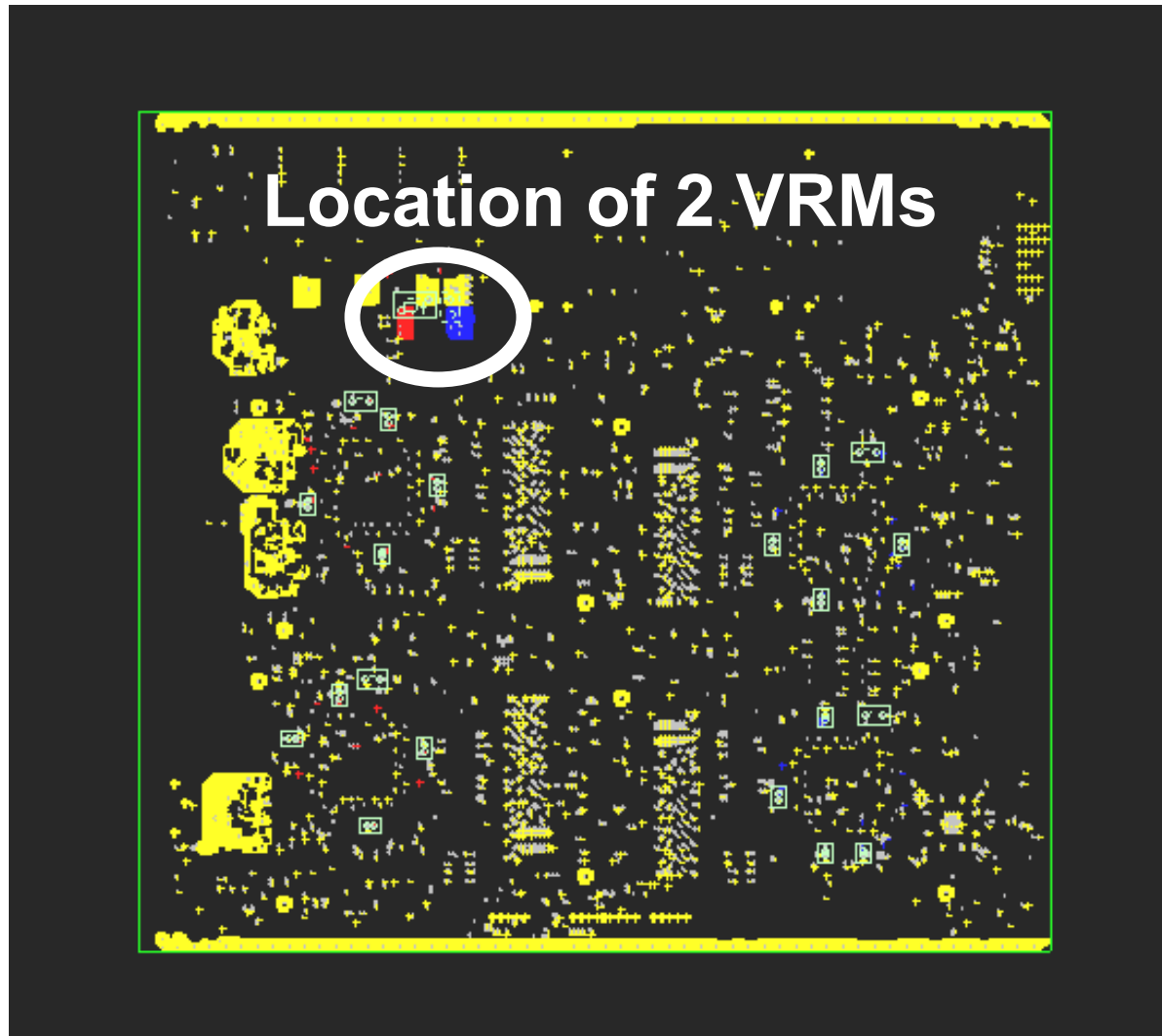
Complete PDS Model of a System Board with 2 Microprocessors



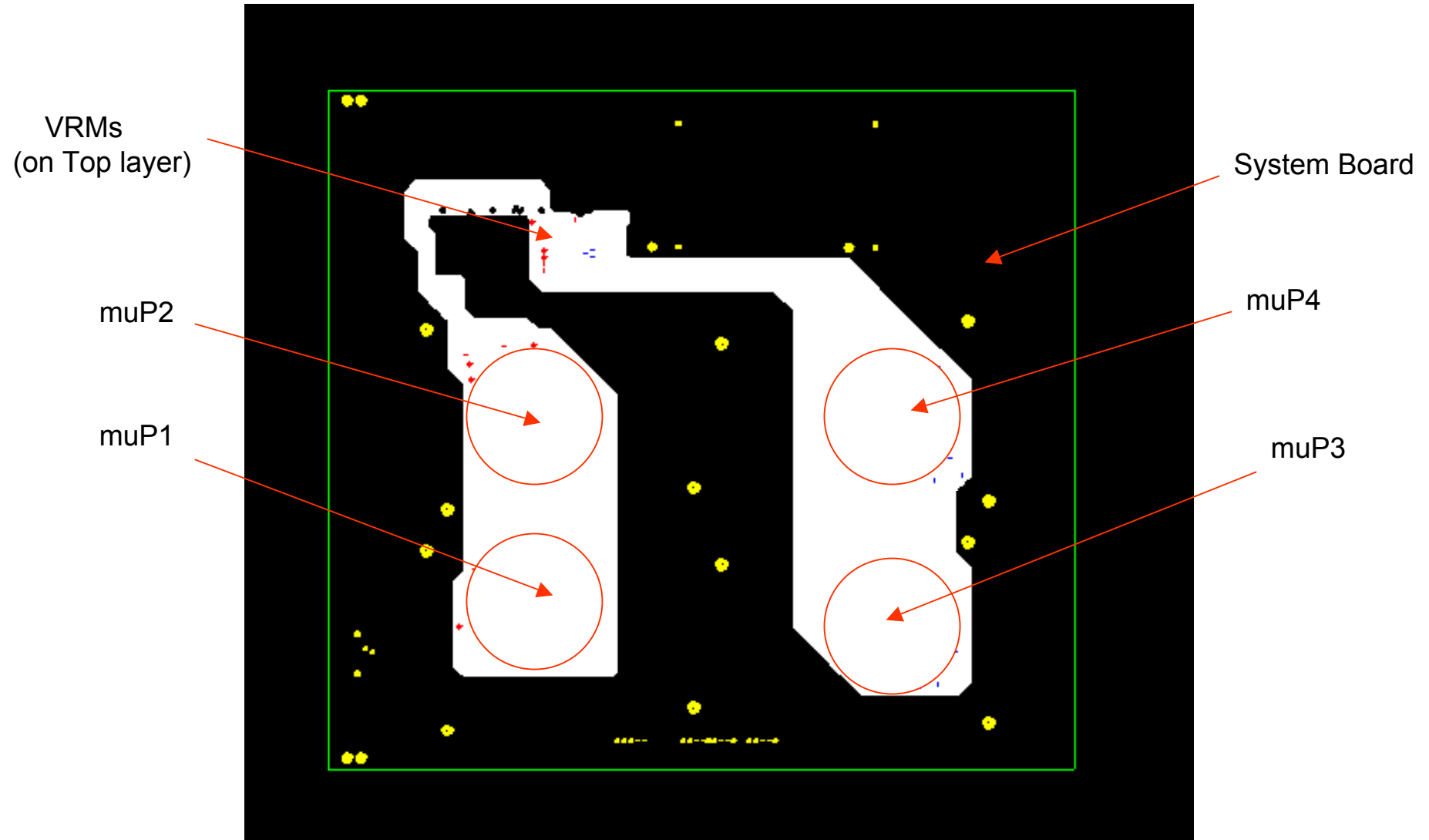
System Board with Multiple Microprocessors:

- **10-Layer PCB**, with
- **6 Signal layers**
- **4 layers for Power Distribution**
- **4 Microprocessors** on the Bottom layer
- **2 VRMs** on the Top layer of the board
- **1 VRM feeds power to 2 Microprocessors**
- **1 Power Plane (V_{dd})**, separated to 2 different areas:
(**$V0_1$ and $V0_2$** , each for core power to **2 Microprocessors**)

Top Layer of the System Board



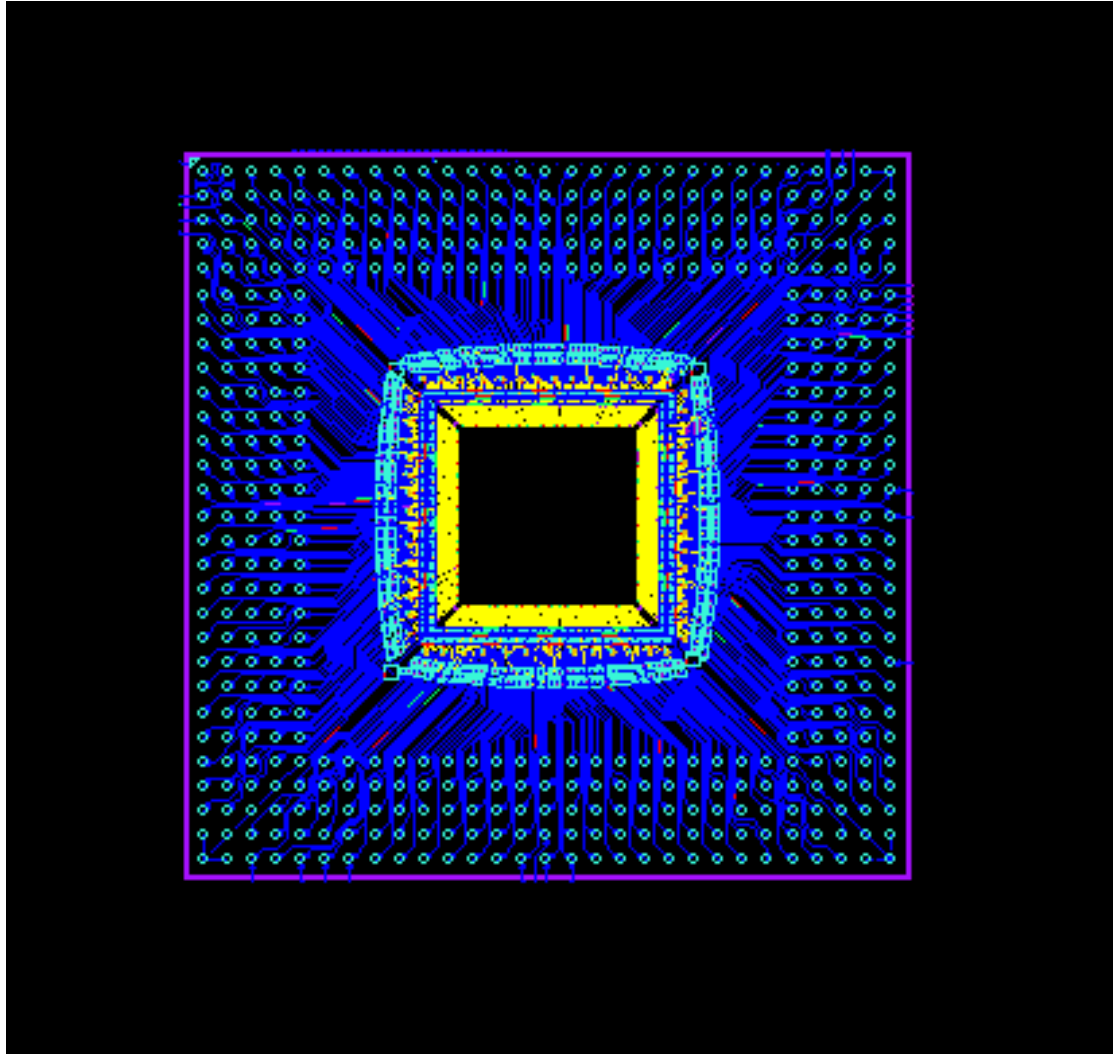
Power Plane of System Board to feed Power to 4 Microprocessors



System Board Stackup

Layer #	Layer Name
(1)	-----Sig_1
(2)	-----Pwr_1/Gnd
(3)	-----Sig_3
(4)	-----Sig_4
(5)	-----Pwr_3
(6)	-----Pwr_4/Gnd
(7)	-----Sig_5
(8)	-----Sig_6
(9)	-----Pwr_2 (V0_1 and V0_2)
(9)	-----Sig_2

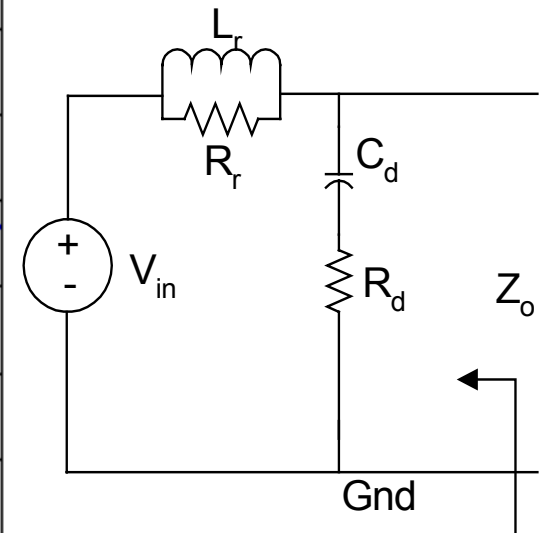
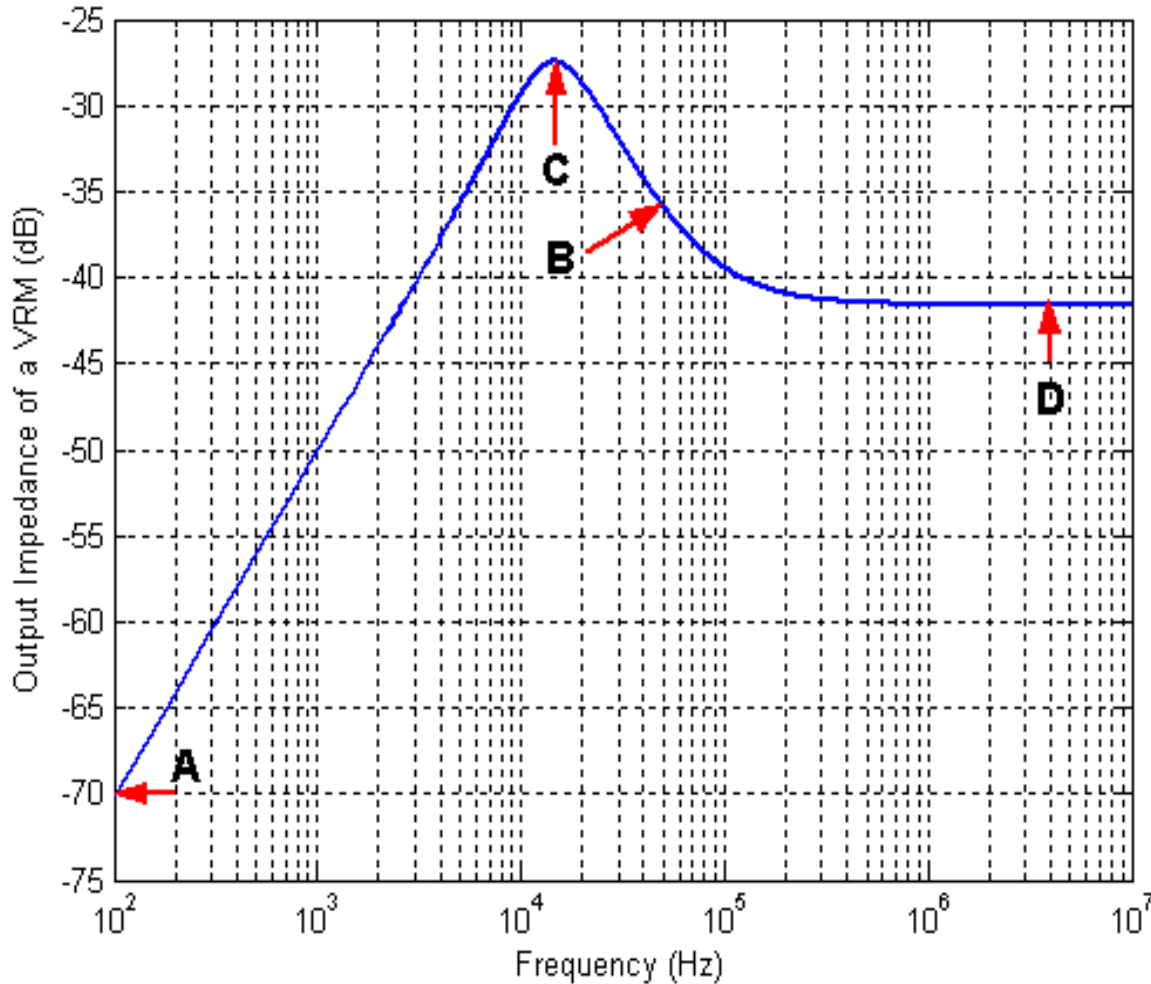
Microprocessor-Package: 480-pin TBGA



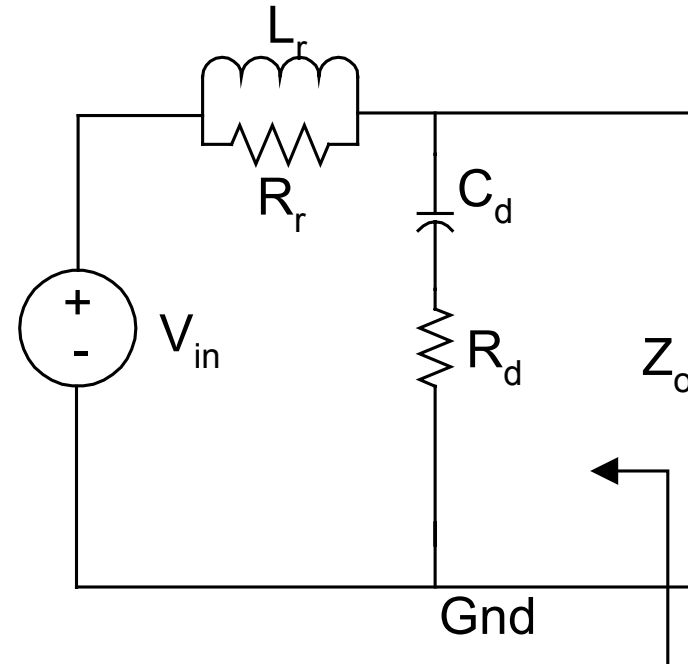
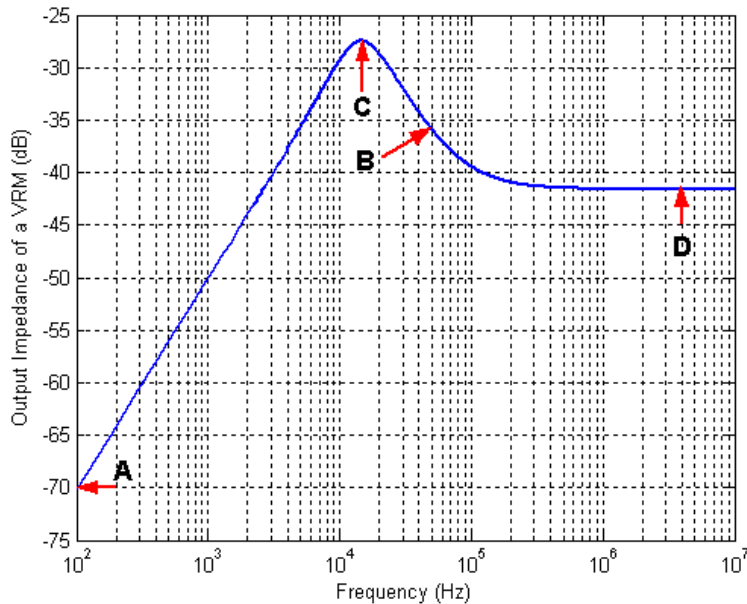
Components Modeled:

- **Voltage Regulator Module (VRM)**
- **Decoupling Capacitors (DECAPS)**
- **System Board (PCB)**
- **Microprocessor – Package (PKG), and**
- **Microprocessor – Die/Core**

VRM-Model Using its Impedance magnitude characteristics



VRM Model



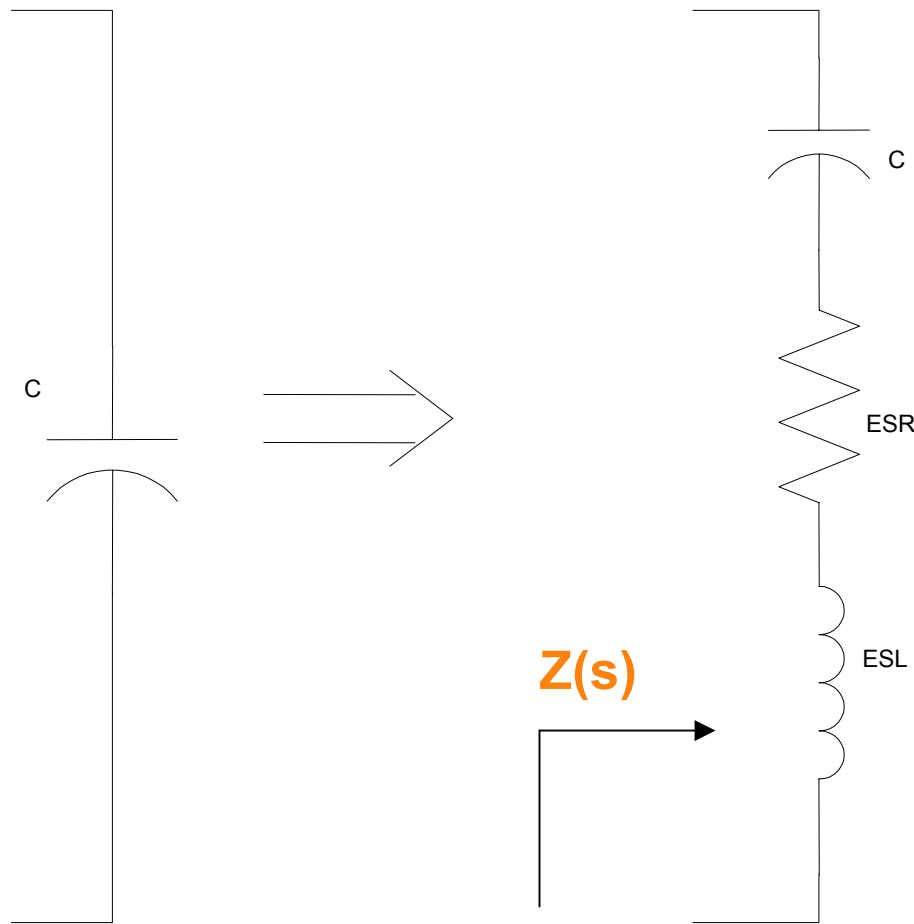
$$L_r = \frac{\text{Impedance at A, } Z_A}{2\pi f_A}$$

$$R_r = 2\pi f_0 L_r Q (= 0.707)$$

$$C_d = \frac{1}{2\pi f_B (\text{Impedance at B, } Z_B)}$$

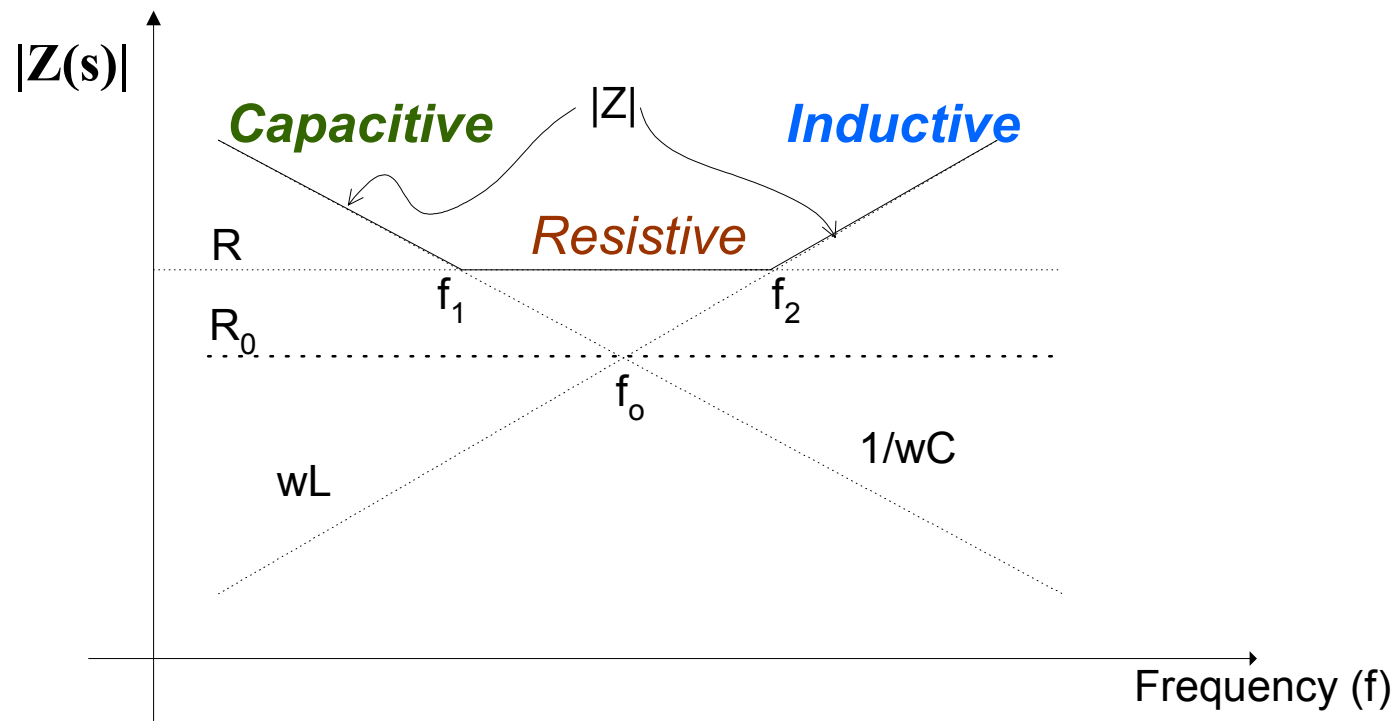
Impedance at D, $Z_D \Rightarrow R_d$

Decoupling Capacitor Model :



$$Z(s) = R + sL + \frac{1}{sC}$$

where $R \implies ESR$, and $L \implies ESL$



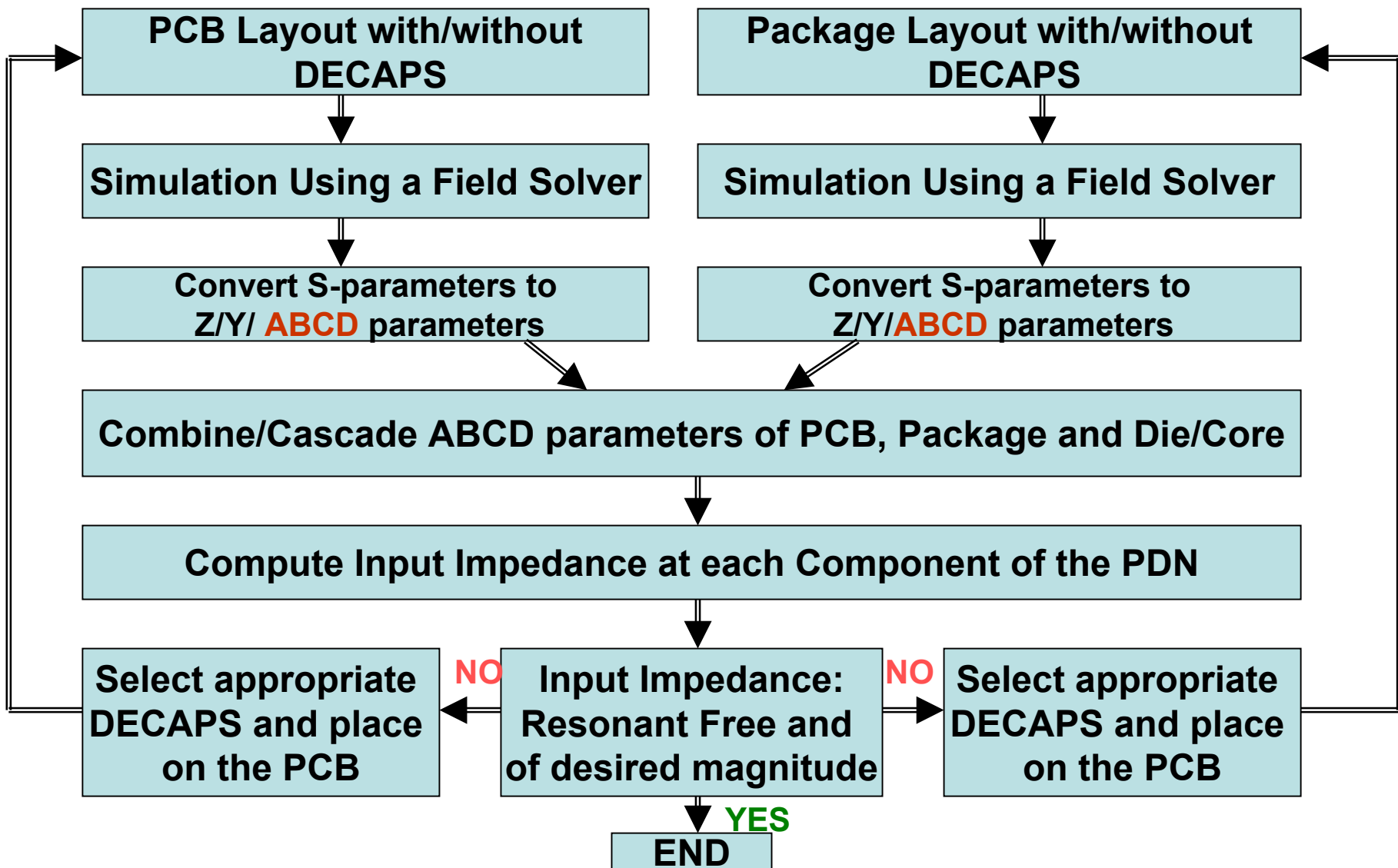
Corner Frequencies:

$$\omega_1 = 2\pi f_1 = \frac{1}{RC}, \quad \omega_2 = 2\pi f_2 = \frac{R}{L}$$

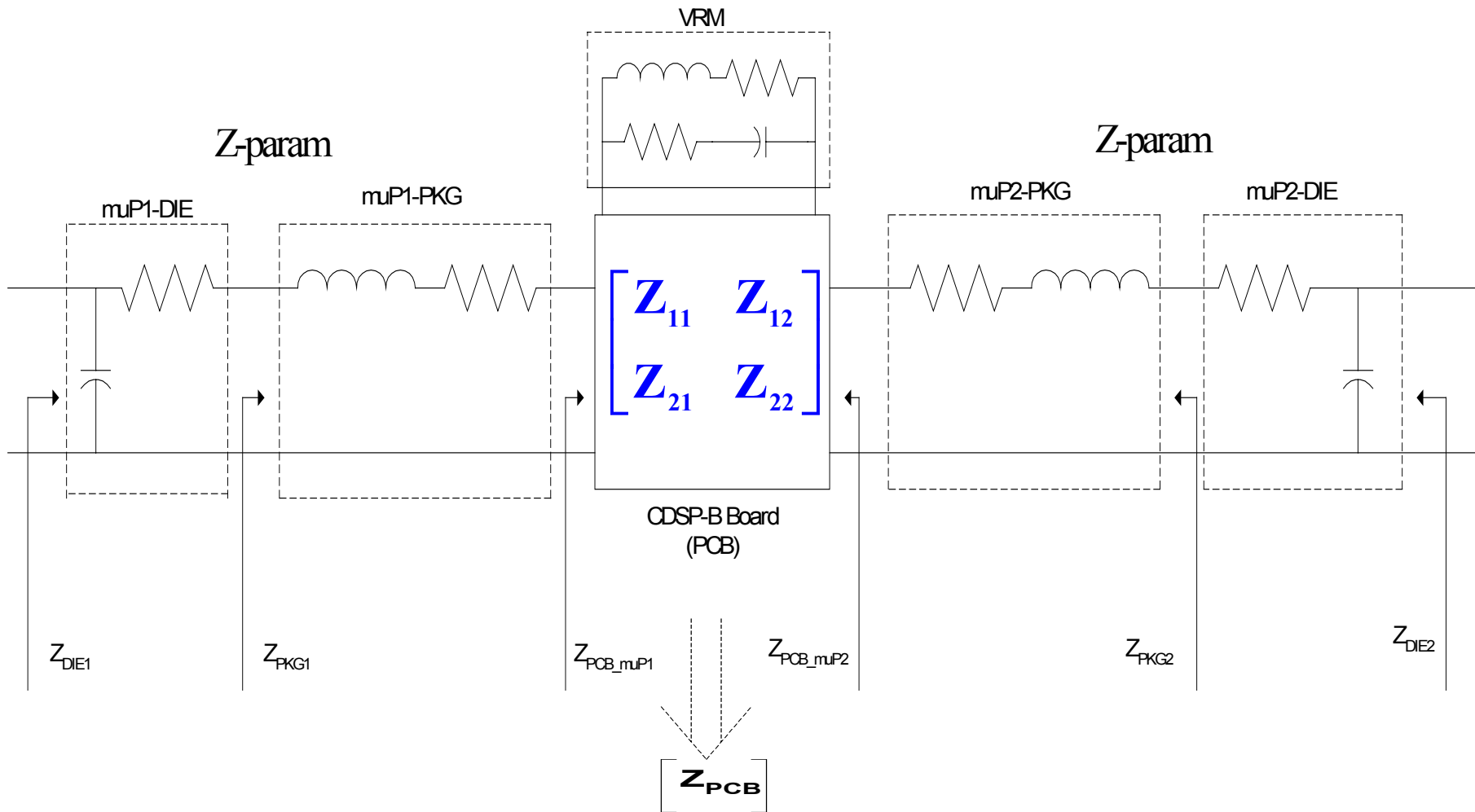
Resonant Frequency: $R \downarrow \Rightarrow \omega_1$ and ω_2 move closer:

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0 \quad \Rightarrow \quad \omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}}$$

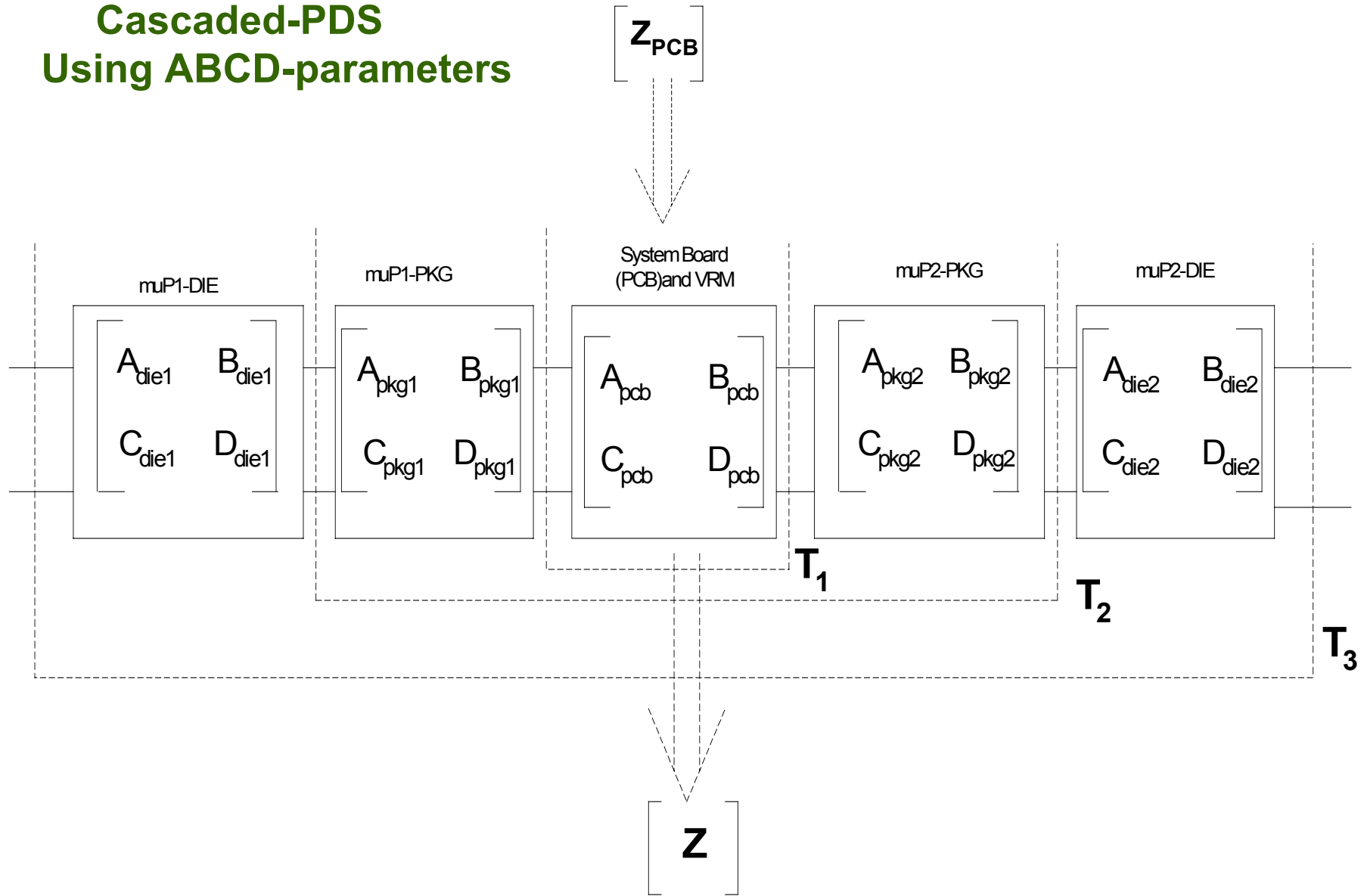
PDN Modeling, Simulation, Analysis and Design Methodology



Complete PDS Model (Hybrid) of System Board with 2 Microprocessors for Frequency-domain Simulation-Analysis



Cascaded-PDS Using ABCD-parameters



Convert Z-parameters of PCB to ABCD-parameters:

$$A_{pcb} = \frac{Z_{11}}{Z_{21}}, \quad B_{pcb} = \frac{Z}{Z_{21}},$$

$$C_{pcb} = \frac{1}{Z_{21}}, \quad D_{pcb} = \frac{Z_{22}}{Z_{21}}$$

where $Z = Z_{11}Z_{22} - Z_{12}Z_{21}$

Z_{11} ==> Input impedance of PCB, looking from the location of **Microprocessor1** with location of **Microprocessor2** as open

Z_{21} ==> Transfer impedance of PCB looking from location of **Microprocessor2** with **Microprocessor1** location open

ABCD-parameters of Package and Die/Core

For Package:

$$A_{\text{pkg1}} = A_{\text{pkg2}} = 1,$$

$$B_{\text{pkg1}} = B_{\text{pkg2}} = R_{\text{pkg}} + sL_{\text{pkg}} + R_{\text{grid}},$$

$$C_{\text{pkg1}} = C_{\text{pkg2}} = 0, \text{ and}$$

$$D_{\text{pkg1}} = D_{\text{pkg2}} = 1$$

For Die/Core:

$$A_{\text{die1}} = A_{\text{die2}} = 1,$$

$$B_{\text{die1}} = B_{\text{die2}} = 0,$$

$$C_{\text{die1}} = C_{\text{die2}} = sC_{\text{chip}}, \text{ and}$$

$$D_{\text{die1}} = D_{\text{die2}} = 1$$

Define

$$T_{pcb} = \begin{bmatrix} A_{pcb} & B_{pcb} \\ C_{pcb} & D_{pcb} \end{bmatrix}$$

$$T_{pkg1} = \begin{bmatrix} A_{pkg1} & B_{pkg1} \\ C_{pkg1} & D_{pkg1} \end{bmatrix}, \quad T_{pkg2} = \begin{bmatrix} A_{pkg2} & B_{pkg2} \\ C_{pkg2} & D_{pkg2} \end{bmatrix},$$

$$T_{die1} = \begin{bmatrix} A_{die1} & B_{die1} \\ C_{die1} & D_{die1} \end{bmatrix}, \quad T_{die2} = \begin{bmatrix} A_{die2} & B_{die2} \\ C_{die2} & D_{die2} \end{bmatrix},$$

For the cascaded PKG1, PCB and PKG2:

$$\begin{aligned} [T_{\text{pkg1_pcb_pkg2}}] &= [T_{\text{pkg1}}][T_{\text{pcb}}][T_{\text{pkg2}}] \\ &= \begin{bmatrix} A_{\text{pkg1_pcb_pkg2}} & B_{\text{pkg1_pcb_pkg2}} \\ C_{\text{pkg1_pcb_pkg2}} & D_{\text{pkg1_pcb_pkg2}} \end{bmatrix} \end{aligned}$$

For the Cascaded DIE1, PKG1, PCB, PKG2 and DIE2:

$$\begin{aligned} [T_{\text{die1_pkg1_pcb_pkg2_die2}}] &= [T_{\text{die1}}][T_{\text{pkg1}}][T_{\text{pcb}}][T_{\text{pkg2}}][T_{\text{die2}}] \\ &= \begin{bmatrix} A_{\text{die1_pkg1_pcb_pkg2_die2}} & B_{\text{die1_pkg1_pcb_pkg2_die2}} \\ C_{\text{die1_pkg1_pcb_pkg2_die2}} & D_{\text{die1_pkg1_pcb_pkg2_die2}} \end{bmatrix} \end{aligned}$$

Self-Impedance of the PCB looking from:

Microprocessor1: $Z_{pcb_muP1} = \frac{A_{pcb}}{C_{pcb}},$

Microprocessor2: $Z_{pcb_muP2} = \frac{D_{pcb}}{C_{pcb}}$

Transfer impedance looking from:

Microprocessor1: $Z_{pcb_muP1_muP2} = \frac{A_{pcb}D_{pcb} - B_{pcb}C_{pcb}}{C_{pcb}},$

Microprocessor2: $Z_{pcb_muP2_muP1} = \frac{1}{C_{pcb}}$

Composite Impedance looking from:

Package1: $Z_{\text{pkg1}} = \frac{A_{\text{pkg1_pcb_pkg2}}}{C_{\text{pkg1_pcb_pkg2}}},$

Package2: $Z_{\text{pkg2}} = \frac{D_{\text{pkg1_pcb_pkg2}}}{C_{\text{pkg1_pcb_pkg2}}}$

Die1: $Z_{\text{die1}} = \frac{A_{\text{die1_pkg1_pcb_pkg2_die2}}}{C_{\text{die1_pkg1_pcb_pkg2_die2}}}$

Die2: $Z_{\text{die2}} = \frac{D_{\text{die1_pkg1_pcb_pkg2_die2}}}{C_{\text{die1_pkg1_pcb_pkg2_die2}}}$

Simulation of the System Board Using Field Solver:

==>

Output: Z-Parameters for the System Board (PCB)

- Next, Effective Output Impedance:

Z_{Pkg} , for (PCB+Package), and

Z_{die} , for (PCB+Package + Die Capacitance)

- Computed by cascading the **Two-Port Network Model** of PCB, Package and DIE – represented by **ABCD-parameters**

Output Impedances with

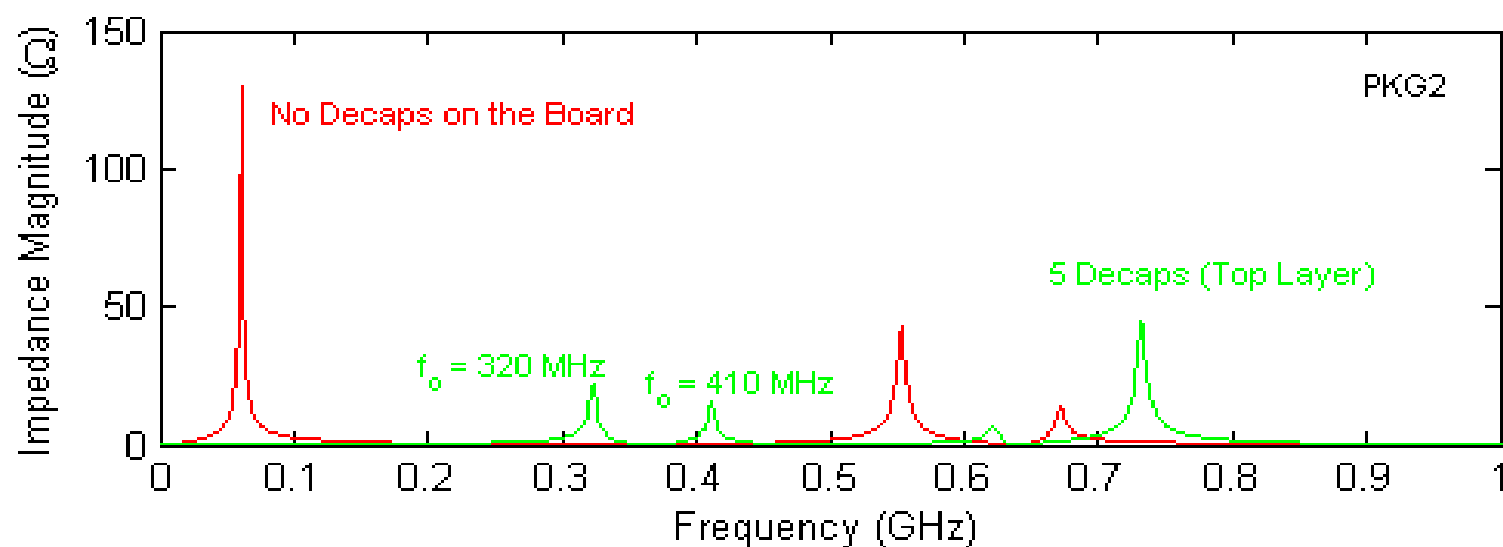
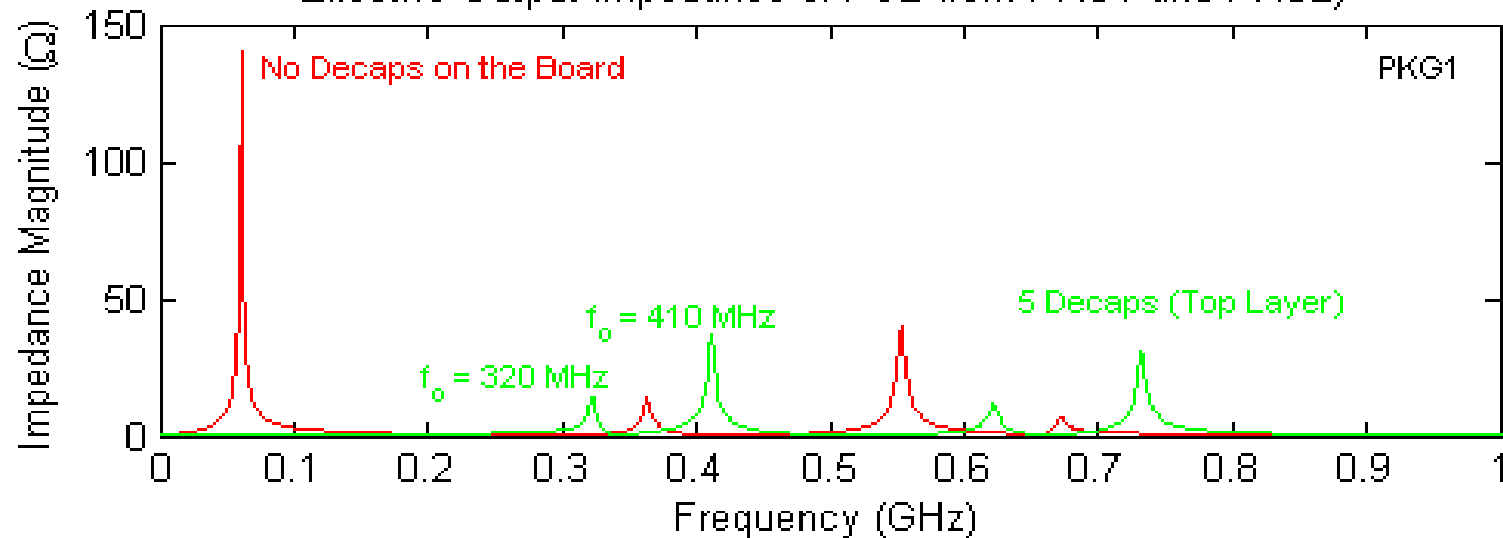
- No Decaps, and
- **5 DECAPS** around MuP1 and MuP2 On the Top Layer

5 DECAPS on the Top-layer:

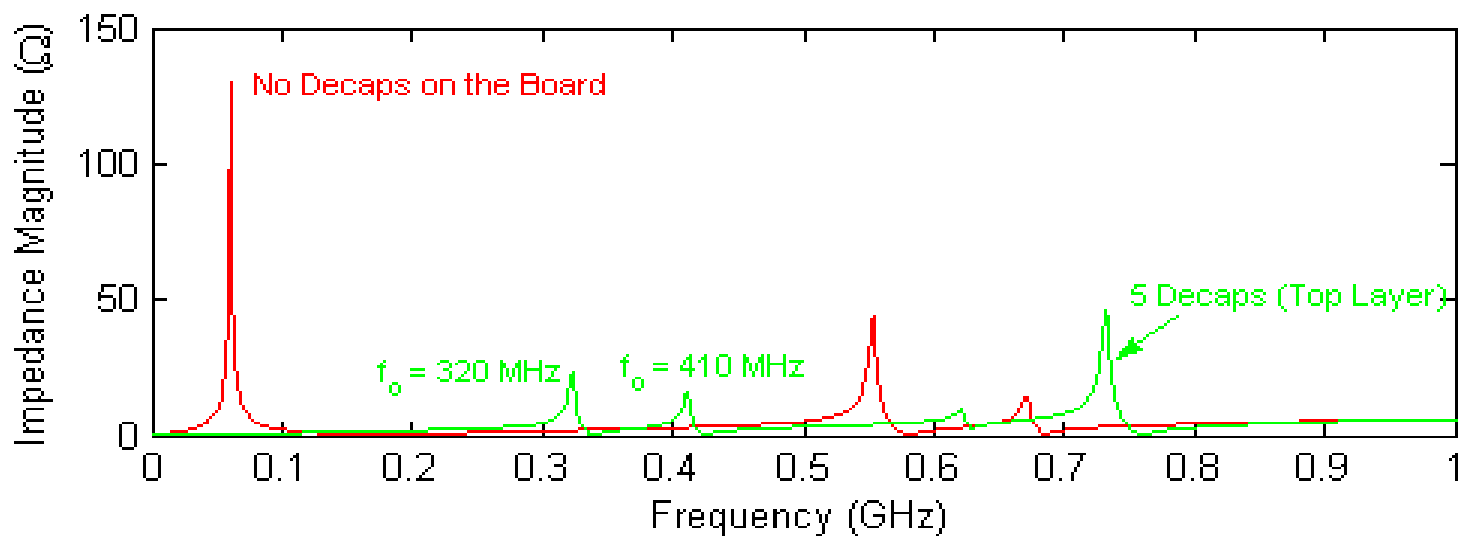
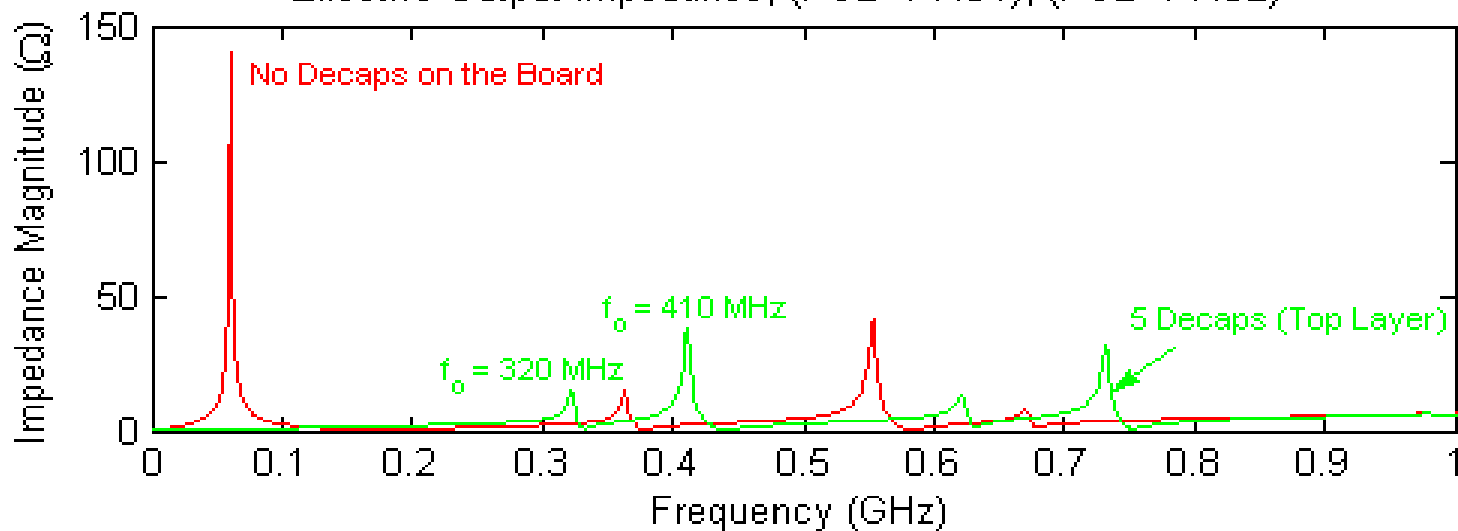
4 DECAPS : $C = 100 \text{ nF}$, $ESR = 10.2 \text{ m}\Omega$, $ESL = 195 \text{ pH}$

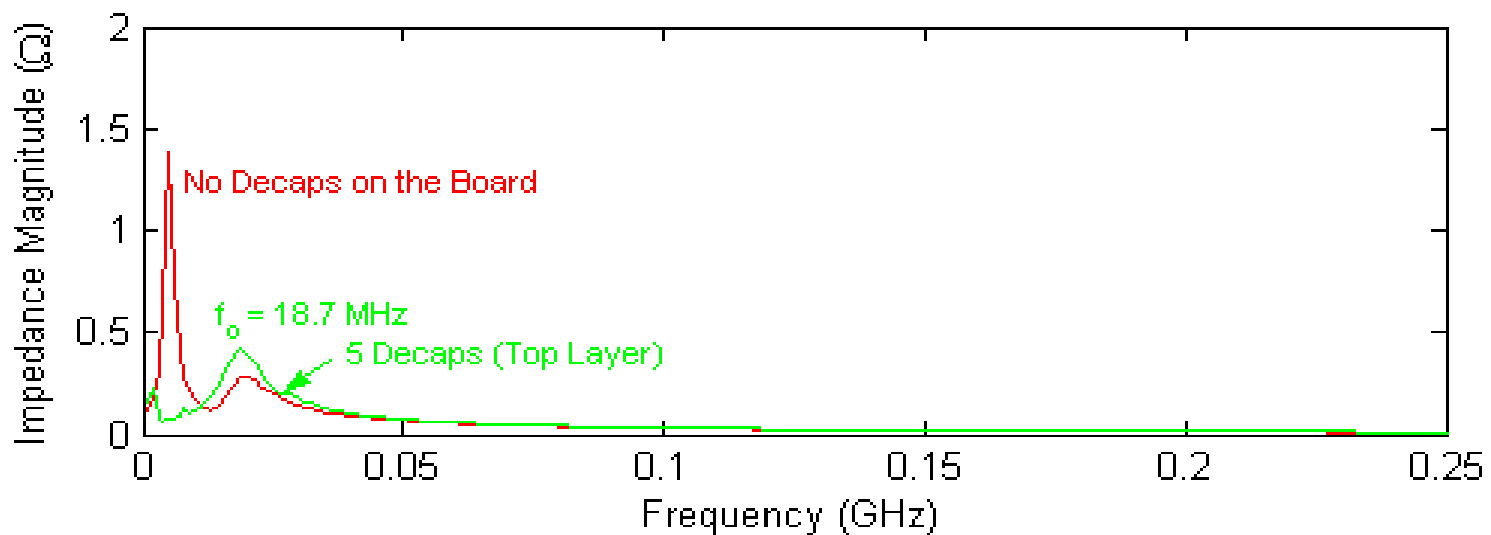
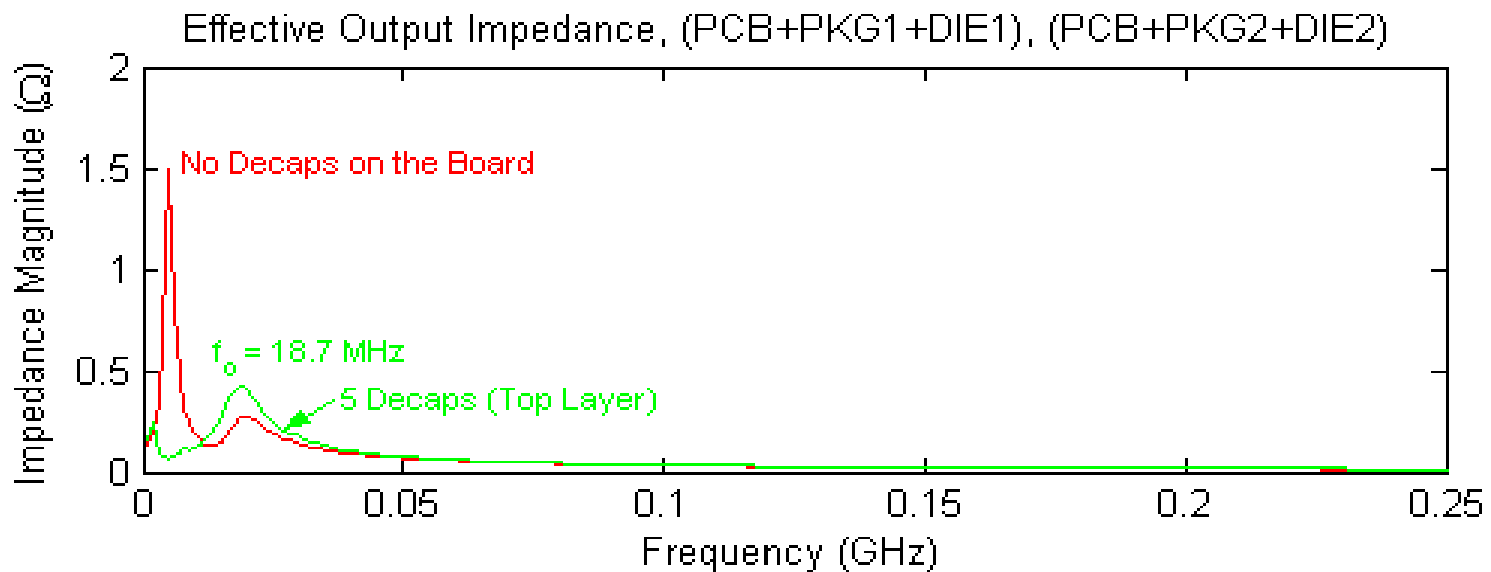
1 DECAP: $C = 10 \text{ nF}$, $ESR = 50 \text{ m}\Omega$, $ESL = 200 \text{ pH}$

Effective Output Impedance of PCB from PKG1 and PKG2)



Effective Output Impedance, (PCB+PKG1), (PCB+PKG2)





5 Decaps on the Top-Layer:

- removes 60 MHz resonance peak,
- introduces 310 MHz and 400 MHz resonance peaks

Selected Caps to be placed on the Bottom Layer:

AVX's (0508) caps of 270 pF:

$C = 270 \text{ pF}$, $ESR = 1.49 \text{ Ohm}$, $ESL = 0.6 \text{ nH}$, $f_r = 395.51 \text{ MHz}$,

To reduce resonance peaks on the System board, upto 400 MHz

Output Impedances with (5 + 16) DECAPS around MuP1 and MuP2

5 Decaps on the Top-Layer:

4 DECAPS : $C = 100 \text{ nF}$, $ESR = 10.2 \text{ m}\Omega$, $ESL = 195 \text{ pH}$

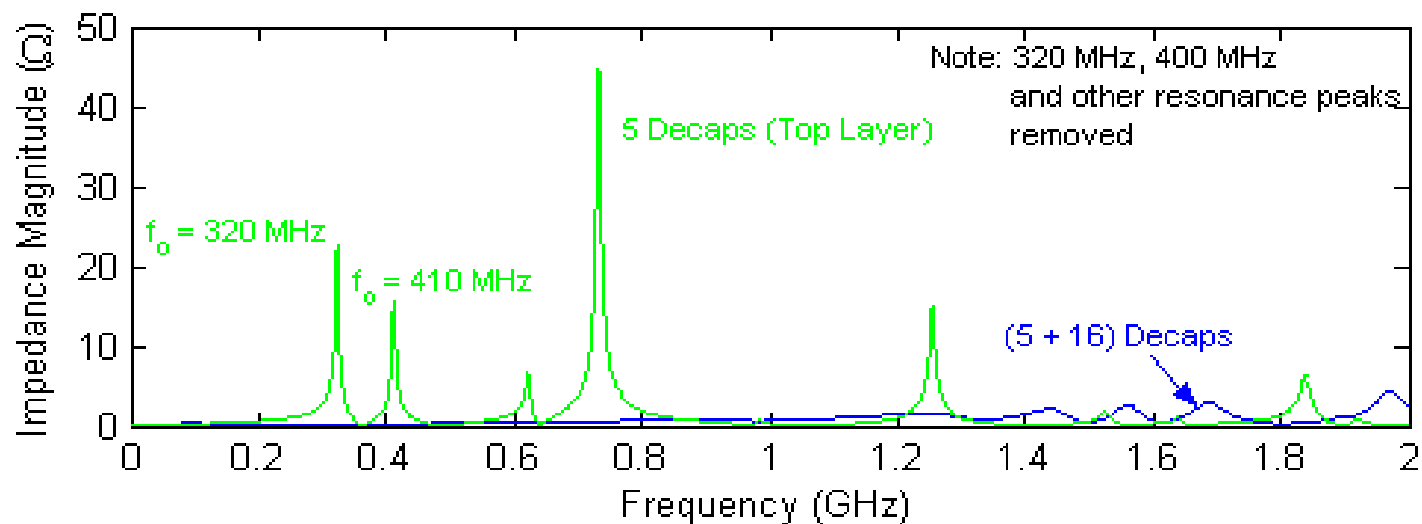
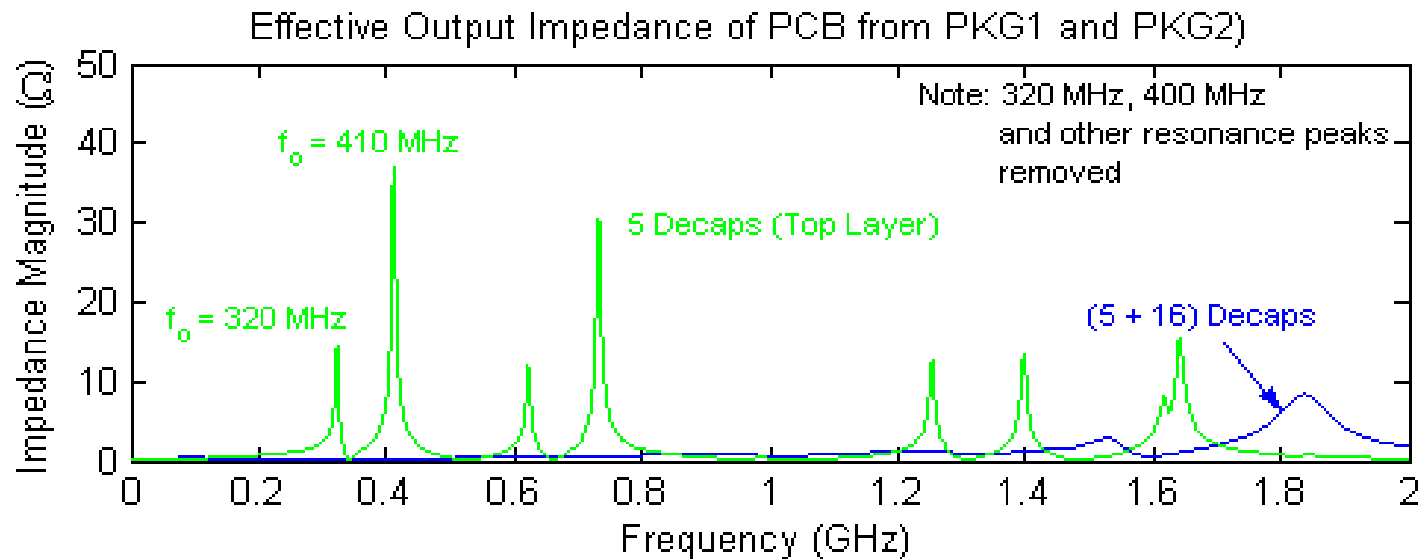
1 DECAP: $C = 10 \text{ nF}$, $ESR = 50 \text{ m}\Omega$, $ESL = 200 \text{ pH}$

Plus

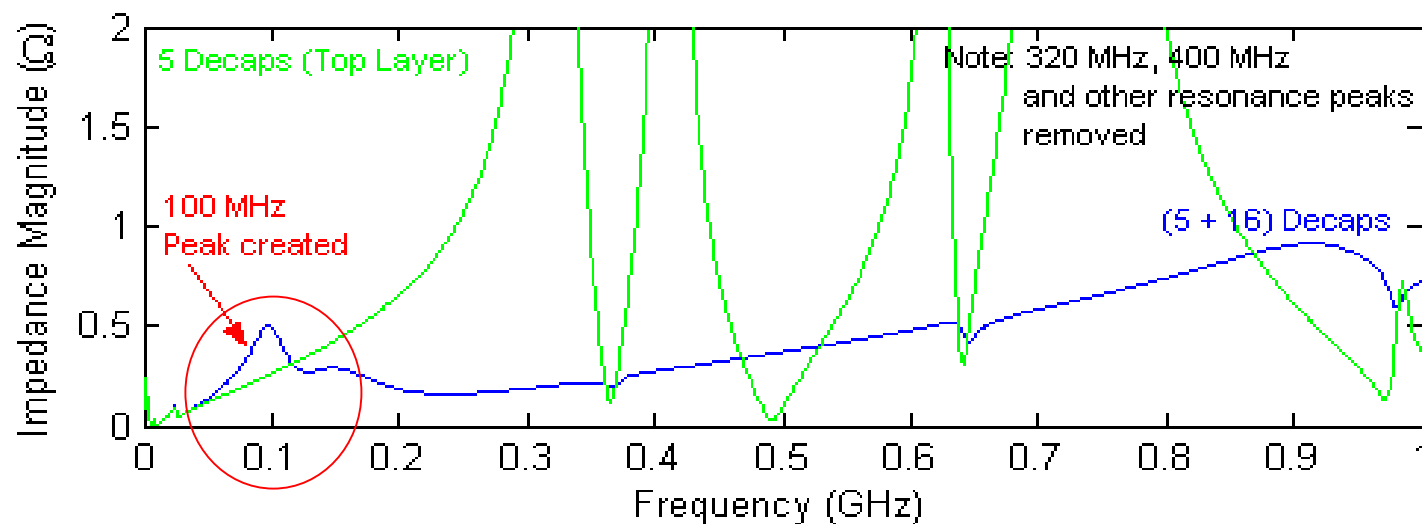
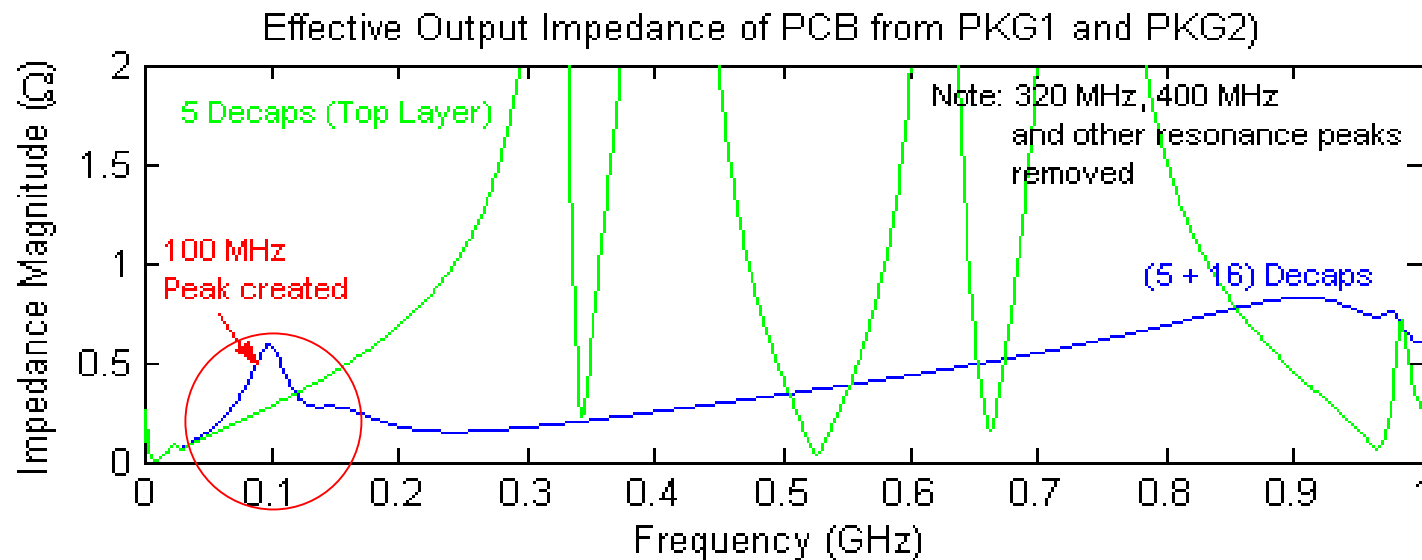
16 AVX's (0508) caps of 270 pF on the Bottom Layer:

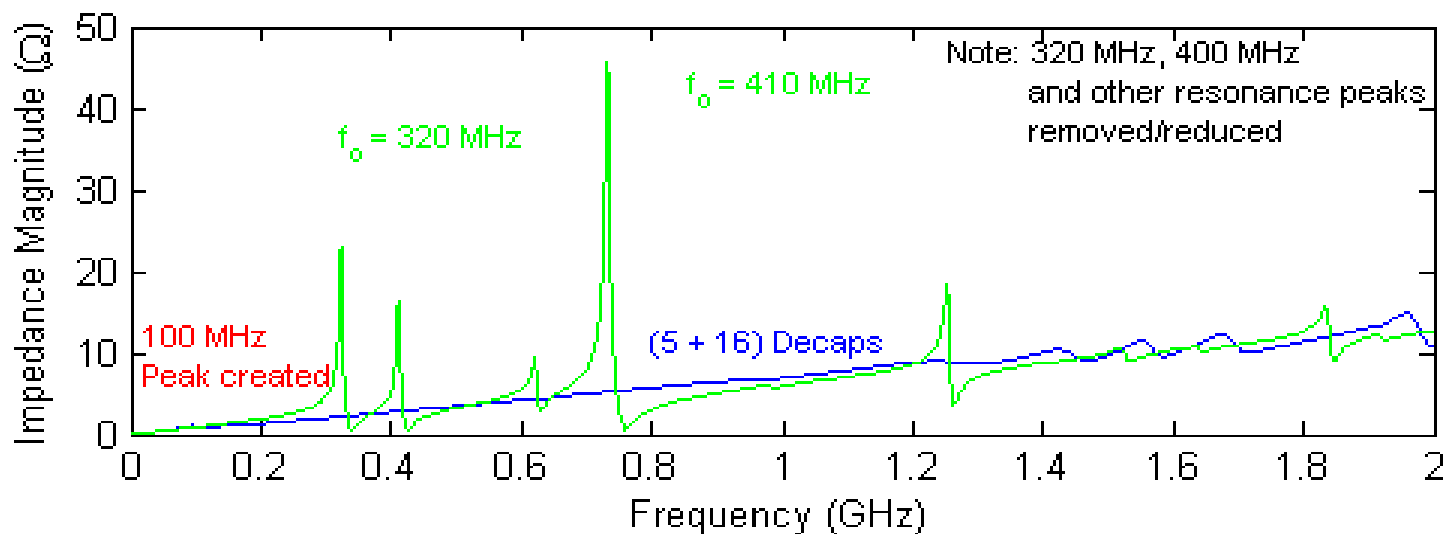
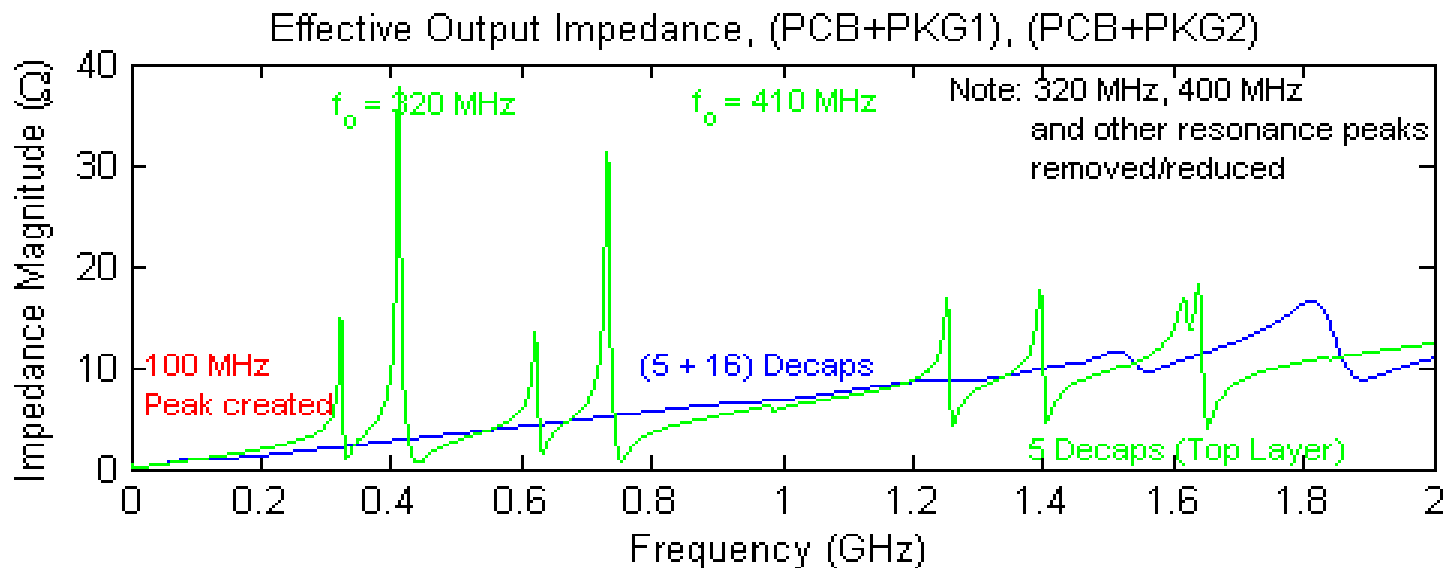
$C = 270 \text{ pF}$, $ESR = 1.49 \text{ Ohm}$, $ESL = 0.6 \text{ nH}$, $f_r = 395.51 \text{ MHz}$,

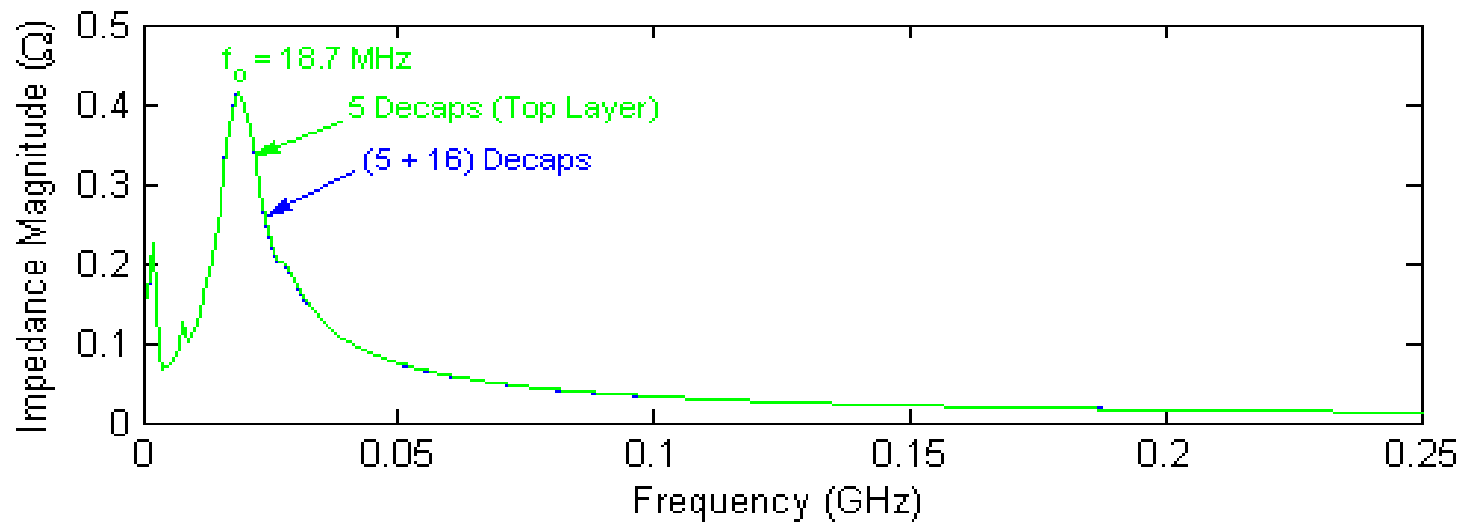
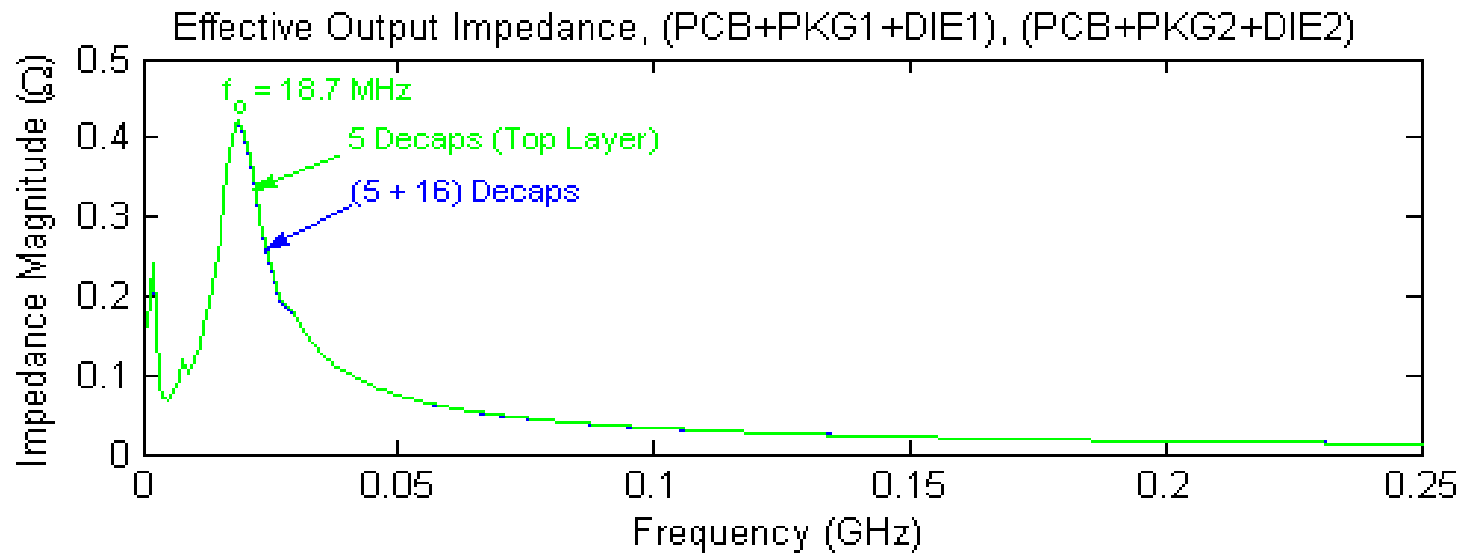
To reduce resonance peaks on the system board upto 400 MHz



Zoomed-in plots of previous slide:







5 Decaps on the Top-Layer:

Plus

16 Decaps on the Bottom-Layer:

- removes 60 MHz resonance peak,
- removes 310 MHz and 400 MHz resonance peaks
- introduces 100 MHz resonance peak,

Output Impedances with (5 + 16 + 16) DECAPS around MuP1 and MuP2

5 Decaps on the Top-Layer:

4 DECAPS : $C = 100 \text{ nF}$, $ESR = 10.2 \text{ m}\Omega$, $ESL = 195 \text{ pH}$

1 DECAP: $C = 10 \text{ nF}$, $ESR = 50 \text{ m}\Omega$, $ESL = 200 \text{ pH}$

16 AVX's (0508) caps of 270 pF on the Bottom Layer:

$C = 270 \text{ pF}$, $ESR = 1.49 \text{ }\Omega$, $ESL = 0.6 \text{ nH}$, $fr = 395.51 \text{ MHz}$,

To reduce resonance peaks on the System board upto 400 MHz

8 AVX's (0603) caps of 2.2 nF on the Bottom Layer:

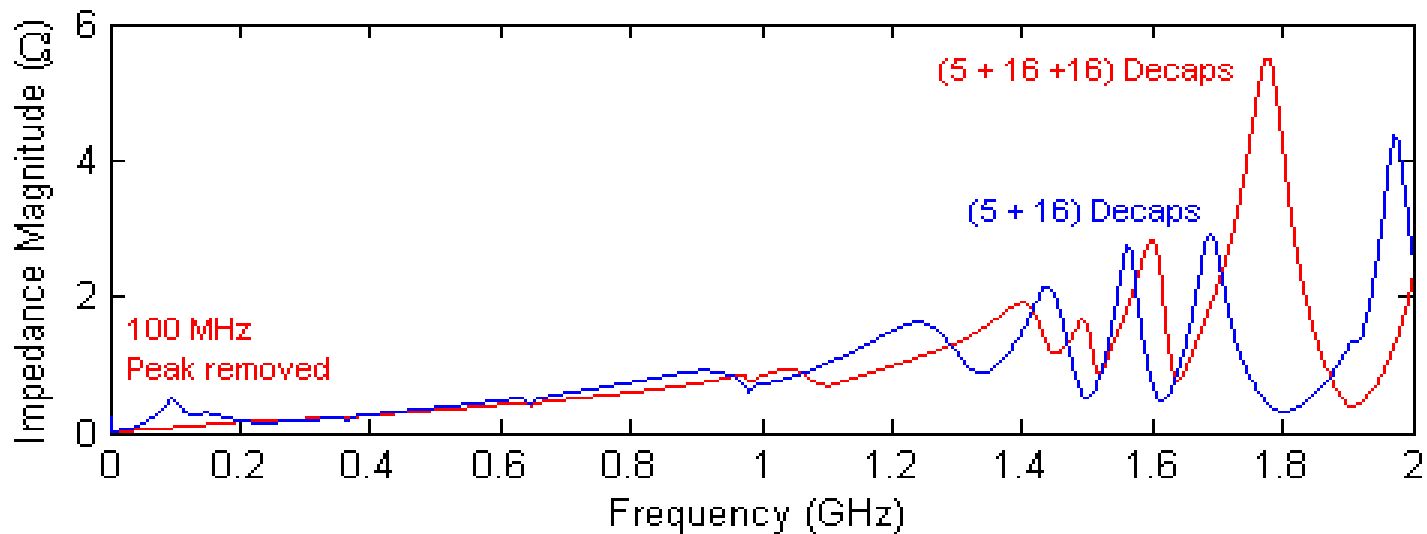
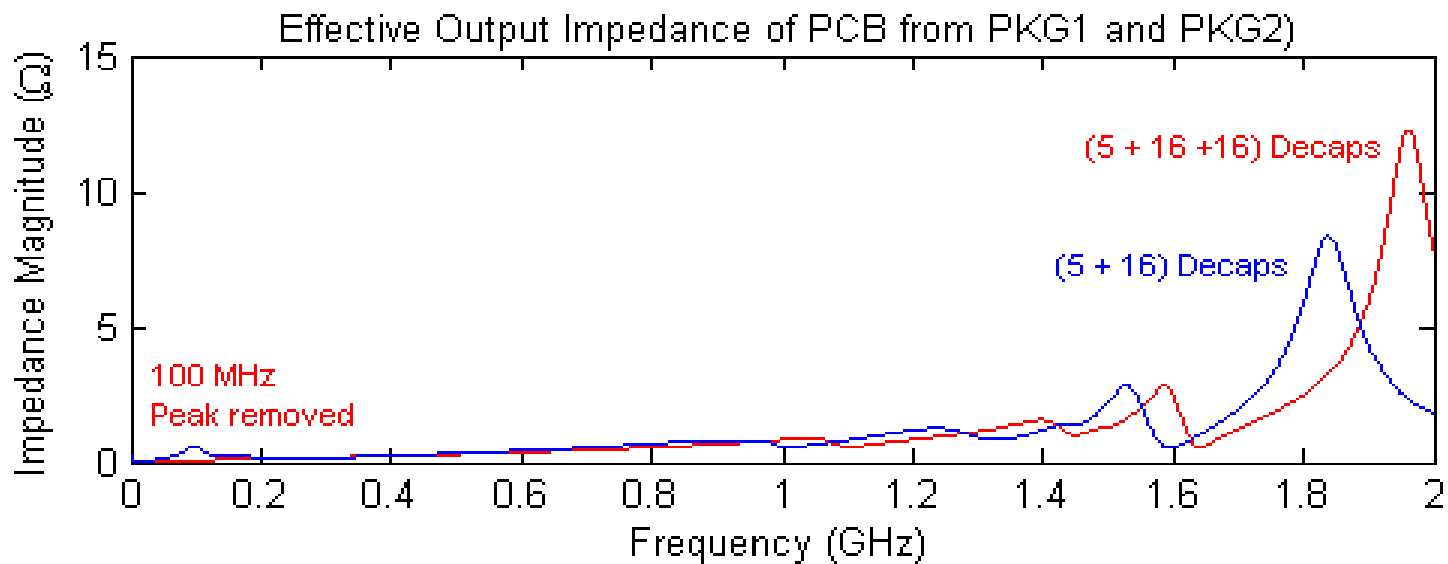
$C = 2.2 \text{ nF}$, $ESR = 0.58 \text{ }\Omega$, $ESL = 0.9 \text{ nH}$, $fr = 113.13 \text{ MHz}$

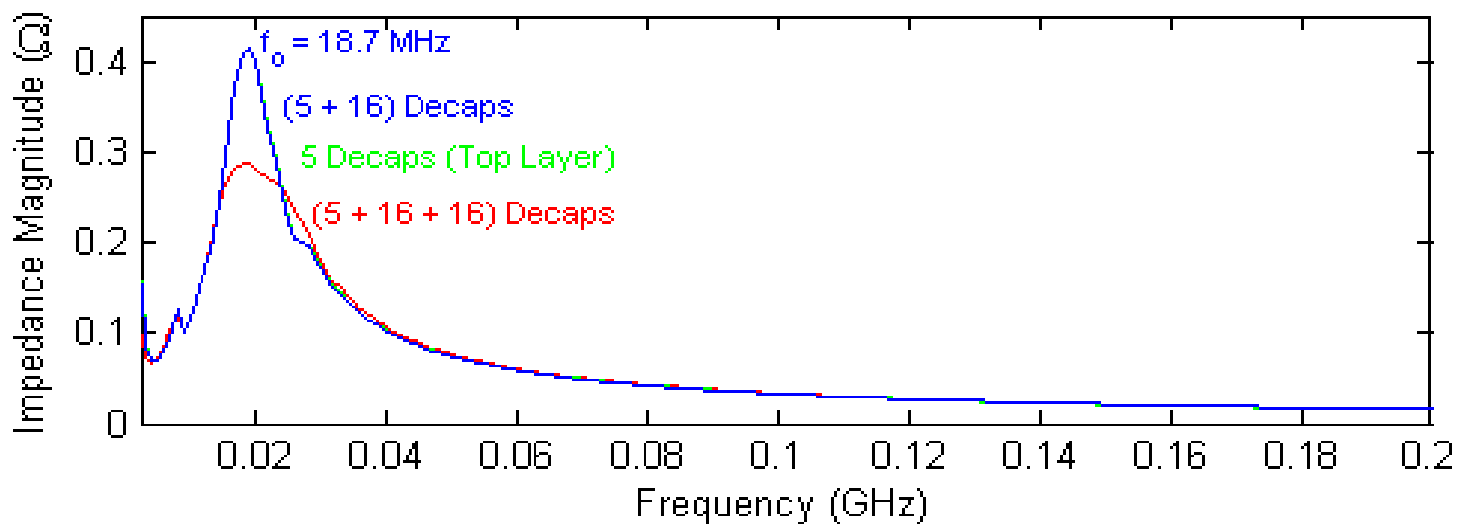
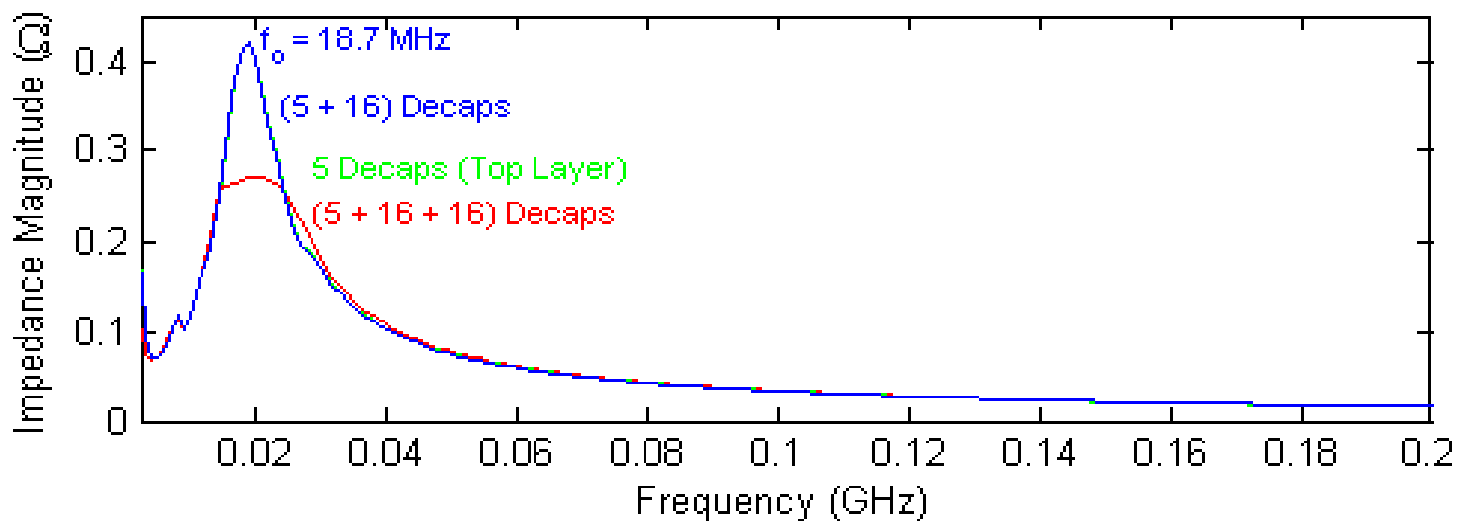
To reduce resonance peaks on the System board upto 100 MHz

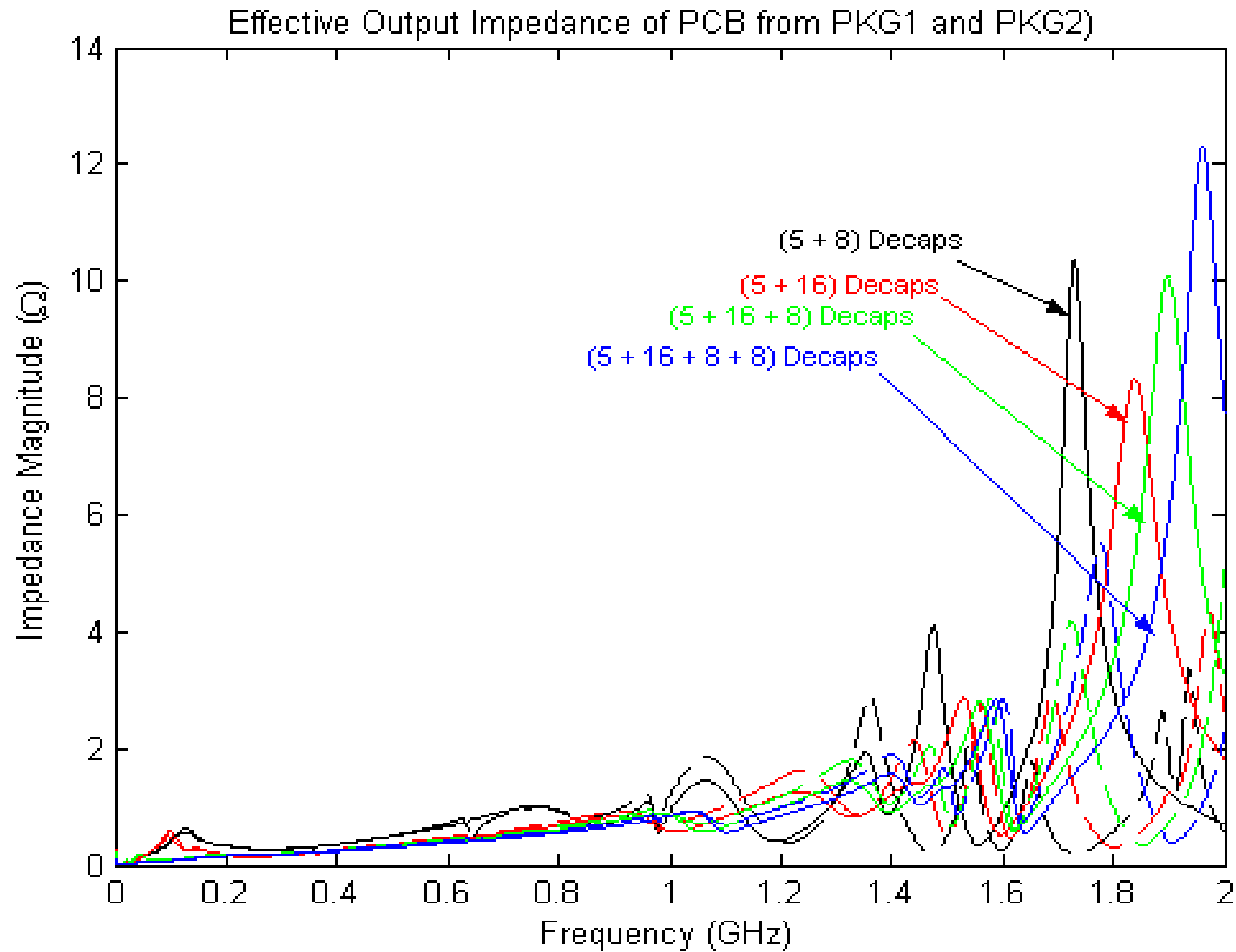
8 AVX's (0603) caps of 22 nF on the Bottom Layer:

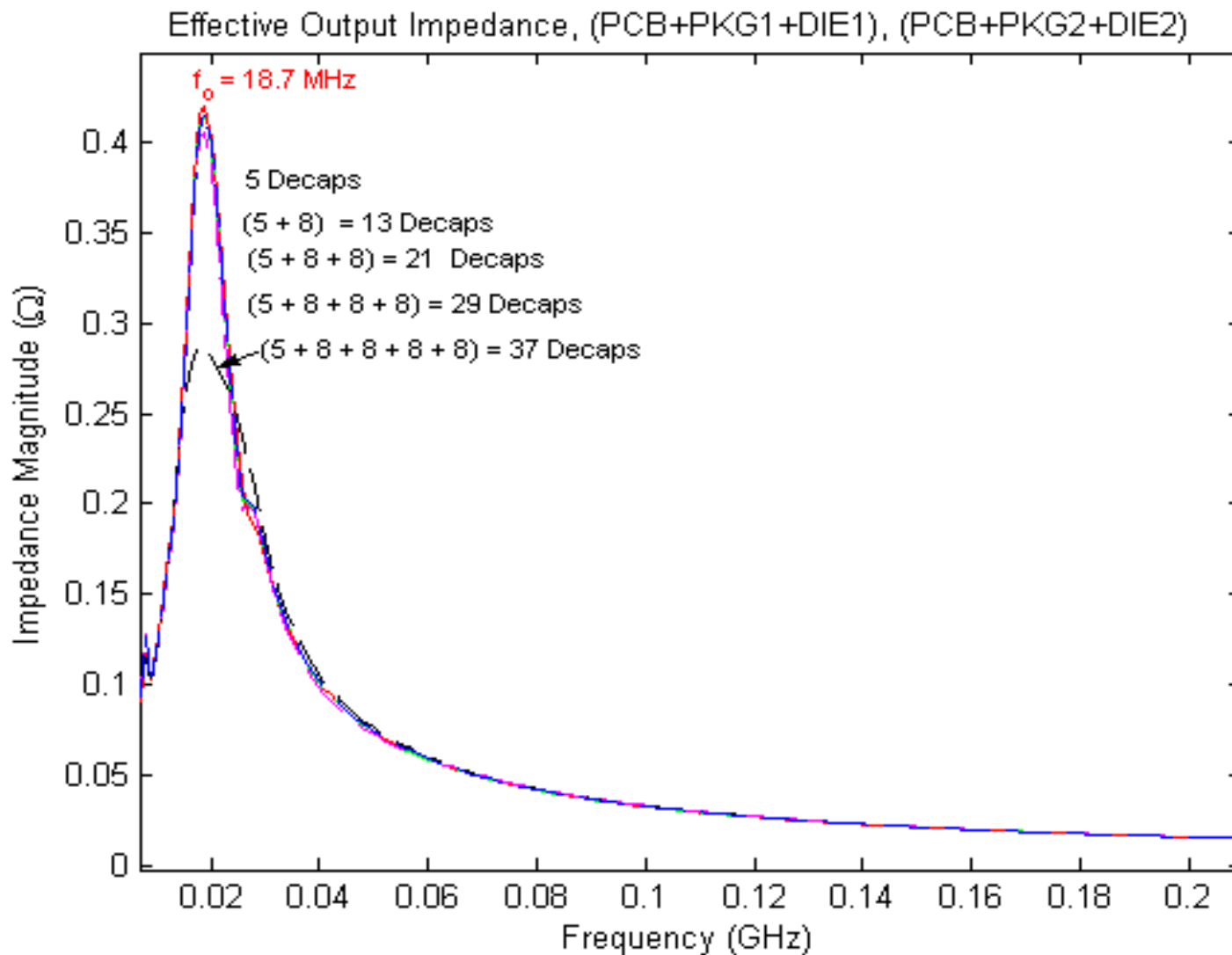
$C = 22 \text{ nF}$, $ESR = 0.2 \text{ }\Omega$, $ESL = 0.9 \text{ nH}$, $fr = 35.77 \text{ MHz}$

To target resonance peak at the Core/Die

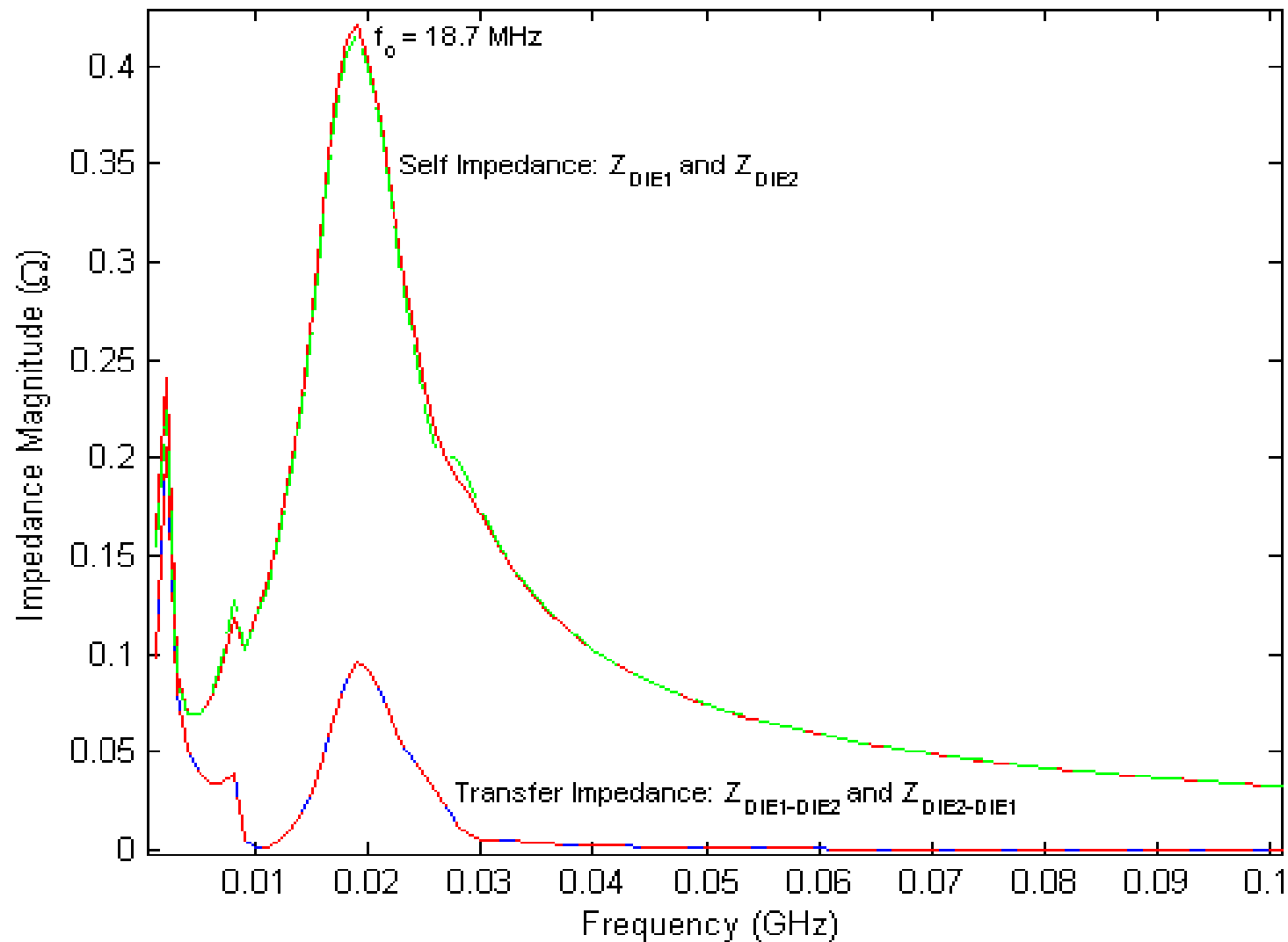






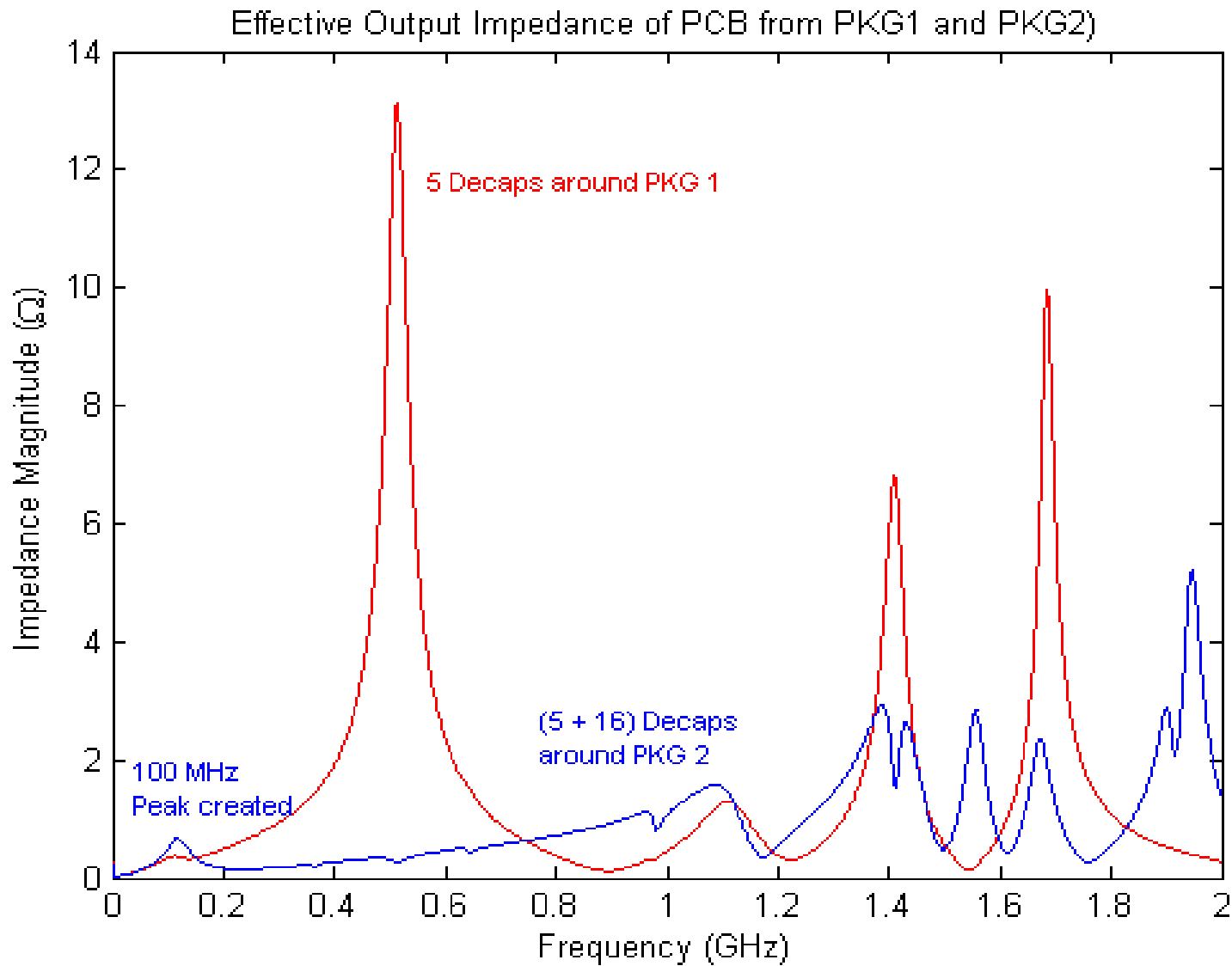


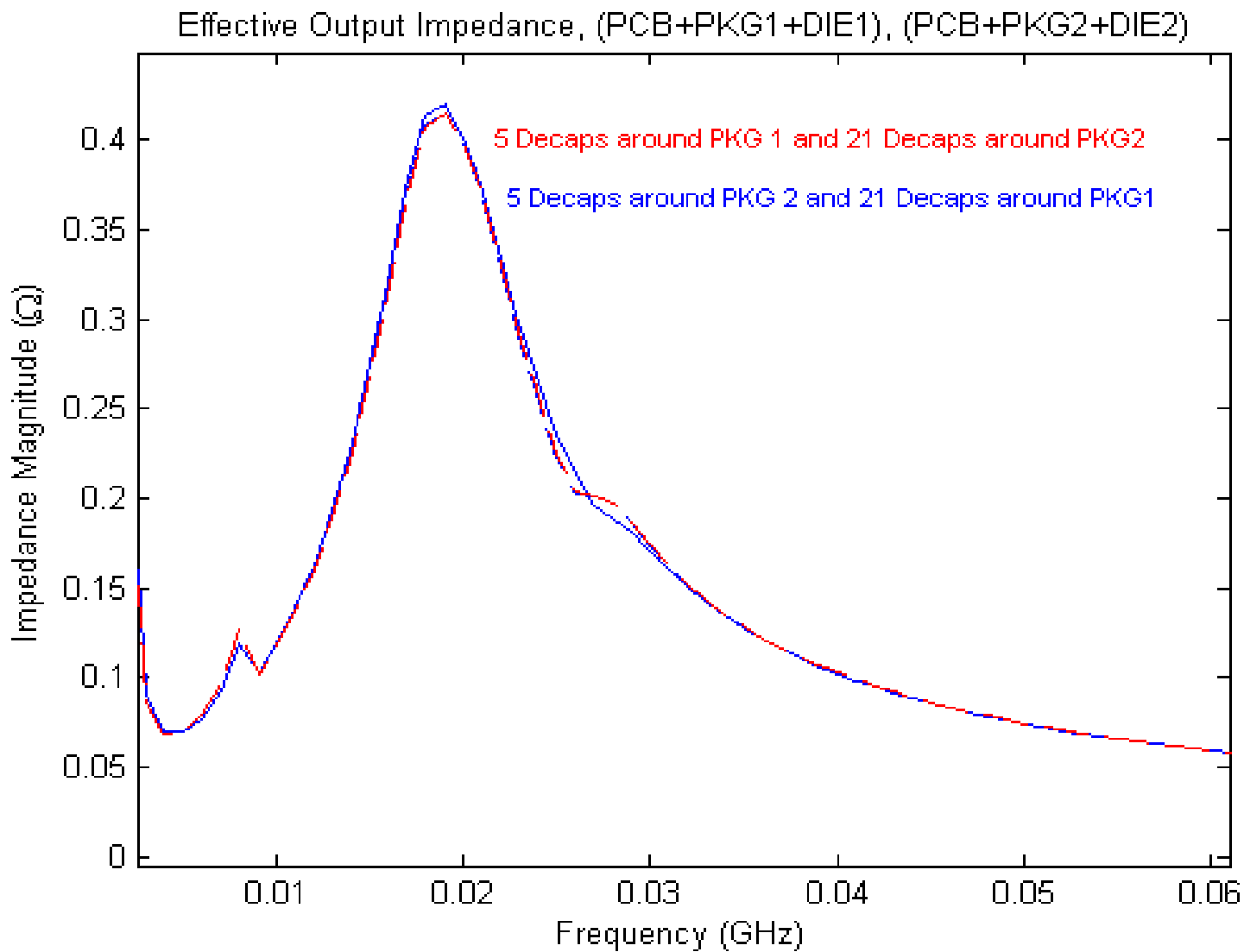
Effective Self and Transfer Impedance at DIE1 and DIE2 with 5 and 21 DECAPS



Output Impedances with

- ♦ 5 DECAPS around MuP1 and 21 DECAPS around MuP2
- ♦ 21 DECAPS around MuP1 and 5 DECAPS around MuP2



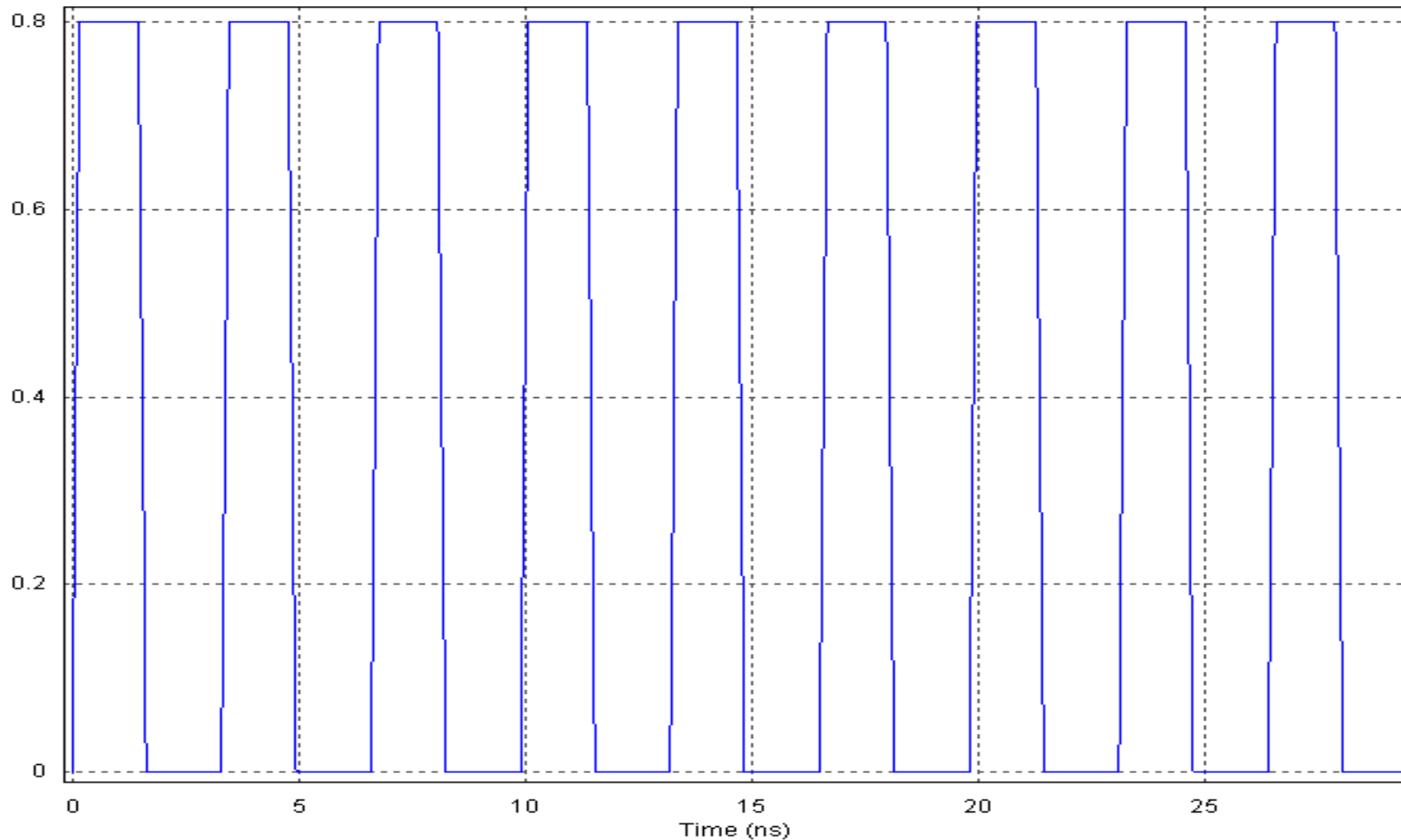


Time Domain-Simulation Results Using

Considered the Core current as a pulse train of frequency 300 MHz.

Current changes from 0 to 0.8 Amp with

$T_{\text{rise}} = T_{\text{fall}} = T/20$ where $T = 1/300 = 3.3$ nsec



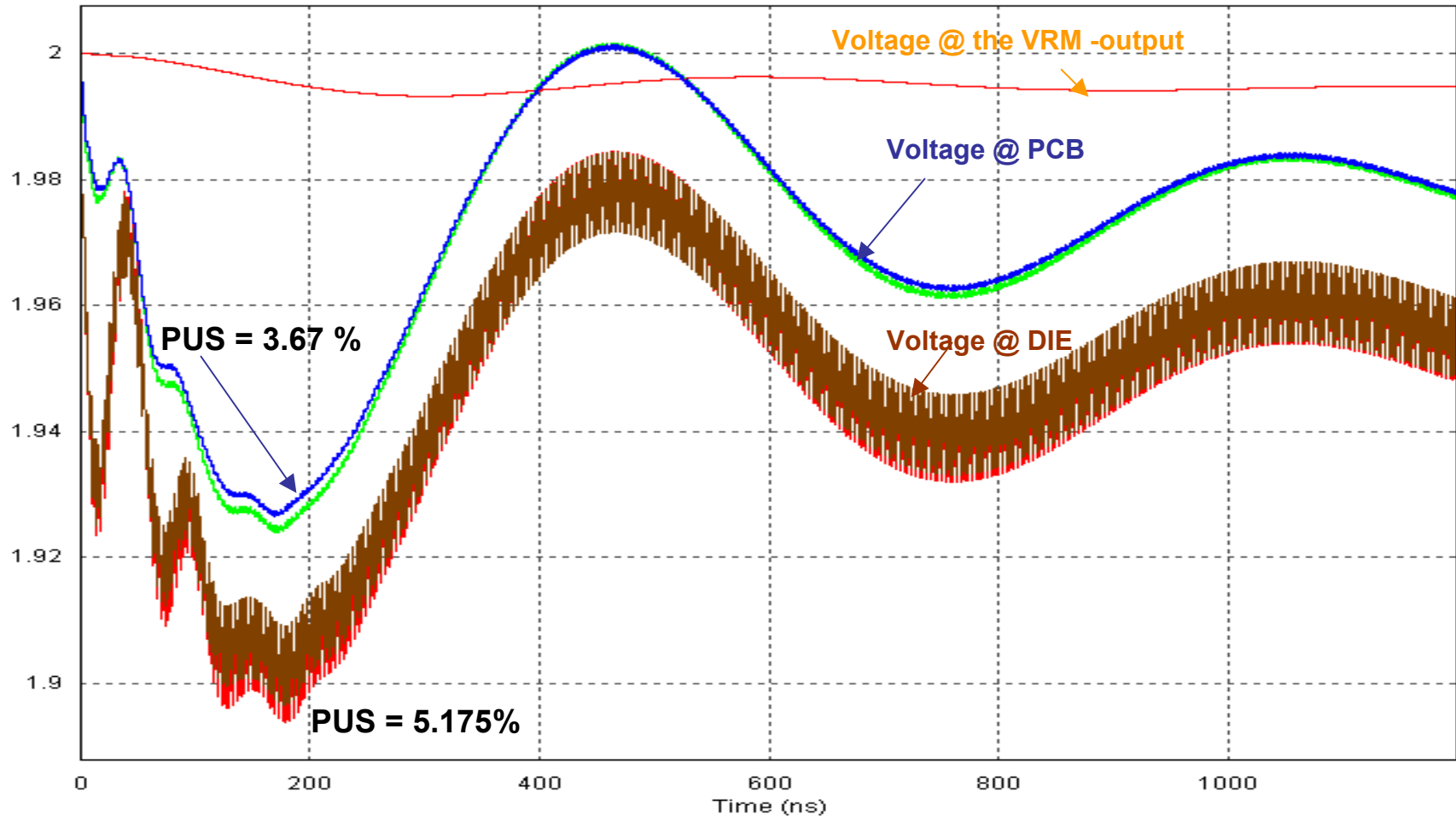
Voltage with 21 DECAPS(4, 100 nF + 1,10 nF on Top layer + 16, 270 pF on bottom layer)

on the PCB ($C_{die} = 50$ nF) with Icore shown on the previous slide

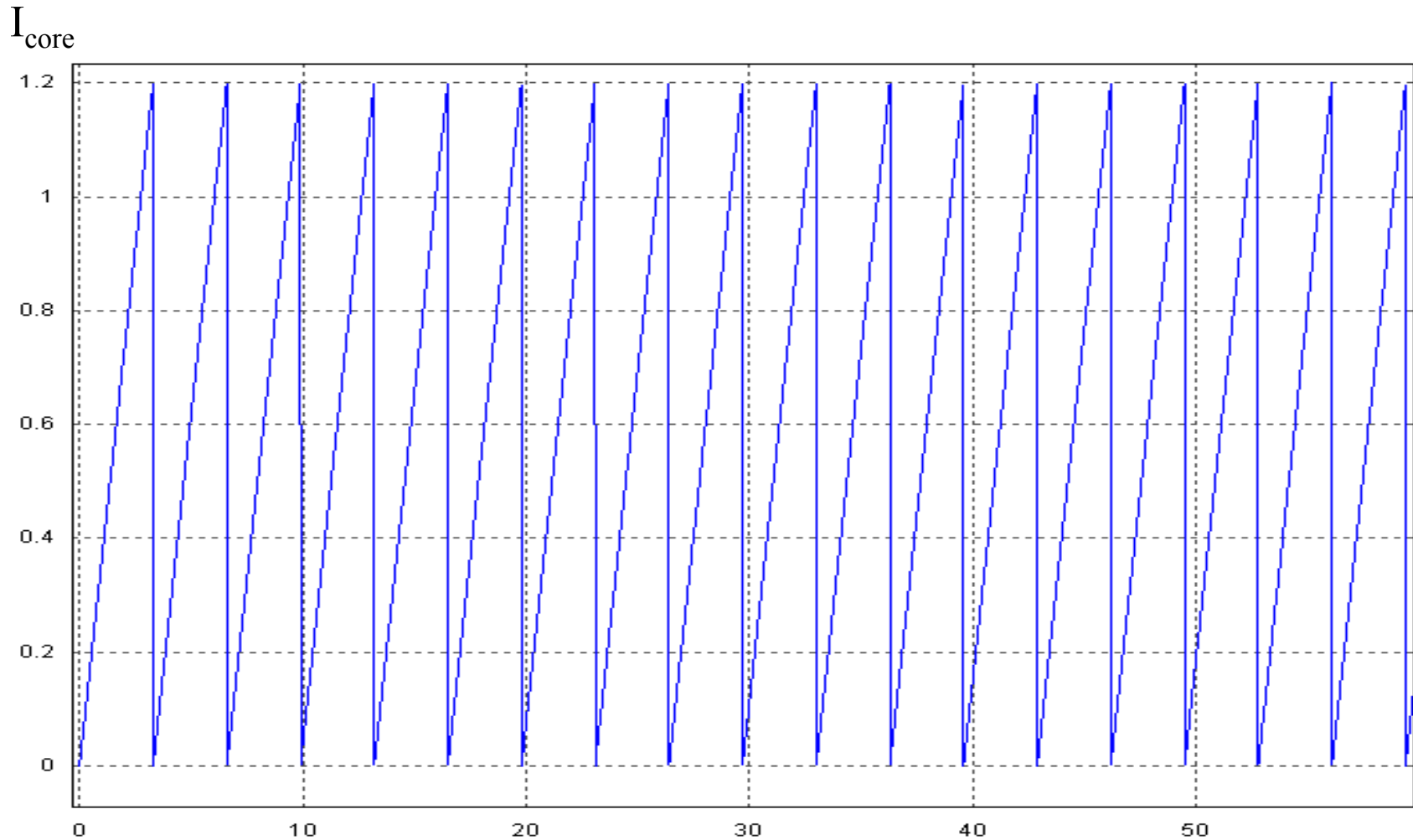
Green Plot → Voltage @ the PCB where Power-pins of Pkg1 is connected

Blue Plot → Voltage @ the PCB where Power-pins of Pkg2 is connected

Red Plot → Voltage @ the Die1; **Brown Plot** → Voltage @ the Die2,



Considered the Core current as a triangular pulse train of frequency 300 MHz. Current changes from 0 to 1.2 Amp in one cycle time, $T = 1/300 \text{ MHz} = 3.3 \text{ nsec}$ and 1.2 Amp to 0 instantaneously

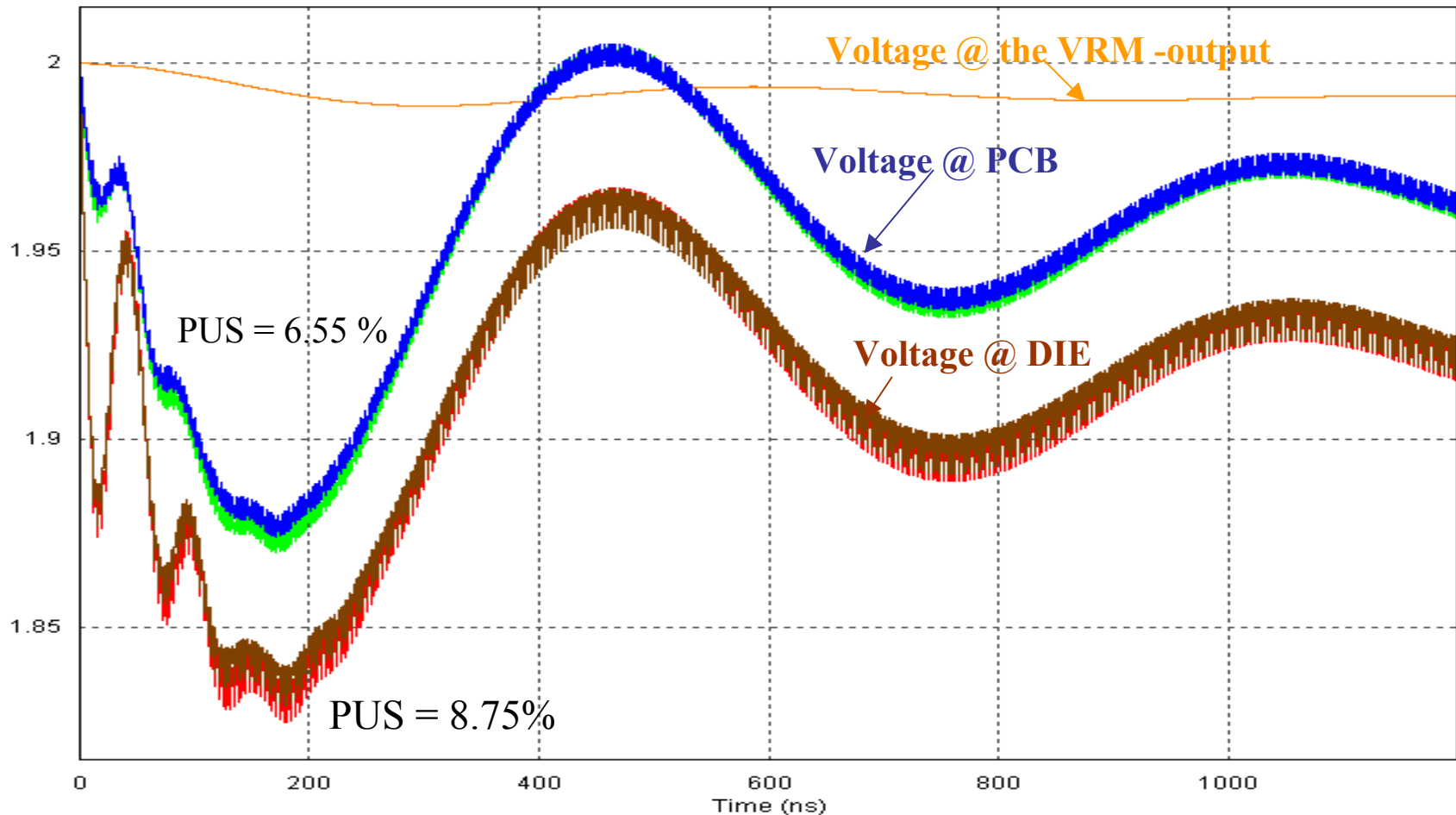


Voltage with 5 DECAPS on the PCB ($C_{die} = 50$ nF) with Icore shown on previous slide

Green Plot → Voltage @ the PCB where Power-pins of Pkg1 is connected

Blue Plot → Voltage @ the PCB where Power-pins of Pkg2 is connected

Red Plot → Voltage @ the Die1; Brown Plot → Voltage @ the Die2,



CONCLUSION:

- Modeling and Design oriented Analysis of a **System Board** is described considering - **two microprocessors** on the board, using 3D-field solver tools for

Frequency domain and **Time domain** simulation

- **Efficient Computational Algorithm** for extracting the **Output Impedance** from Simulation data is described in detail
- The methodology developed analyzes the complete PDS of a Microprocessor system
- The effect of using **DECAPS** to suppress the impedance peaks on the **System board** is described

CONCLUSION (Cont.)

- The board performance is improved significantly by adding 16 DECAPS on the bottom layer of the System board
- Simulation shows that adding 4 or 8 additional DECAPS also reduces 300-400 MHz resonance peaks significantly
- More DECAPS on PCB helps reducing the PCB impedance towards the Target impedance.
- The DIE Impedance peak reduces significantly after 18.7 MHz
==> A dominant sinusoid of 18.7 MHz, superimposed on the dc (Vdd)