Power Delivery Modeling and Design Methodology for A Programmable Logic Device Package

Anil Pannikkat[(1)], Jon Long[(1)] and Jin Zhao[(2)]

[(1)] Altera Corporation, San Jose, CA 95134
[(2)] Sigrity Inc., Santa Clara, CA 95051
Email: APANNIKK@altera.com, jzhao@sigrity.com

Abstract

A power delivery modeling and design methodology for a programmable logic device package is presented in this paper. Both the DC IR drop and high frequency power ground input impedance have been analyzed by commercial available power integrity software and calibrated with measurements. Design modifications have then been carried out for power delivery system improvement of the package for next generation products.

Introduction

In recent years, as the system operation speed increases, and more and more functions are integrated into a single device IC chip, the power consumption of the programmable logic device has increased dramatically although the operating power supply voltages have decreased. Due to these trends, the currents that are supplied to the device through the package power supply system have increased significantly. Meanwhile, the number of I/O in a device has also increased significantly. The large number of I/O buffers required in the device has also placed unusual constraints on the package power supply system design. Another challenge in the package power supply system design is that the mixture of analog and digital circuitry in side a chip with noise and signal integrity constraints requires separate power supplies even for different functional block circuits. Therefore, careful design of the power supply system inside a package and optimization of the ratio of I/O pins to power ground pins are required for both DC and high frequency band so that the simultaneous switching noise can be minimized.

In this paper, a power delivery modeling and design methodology for package power supply system design is introduced. The analysis contains two parts: DC IR drop analysis and high frequency power ground input impedance analysis. A commercial available power integrity analysis software is used to carry both the DC IR drop analysis and the high frequency power ground input impedance analysis. The analysis results are calibrated with measurement results and it shows good agreement between the two sources. Based on the analysis, design modifications are suggested and further analysis shows the improvement of the power supply performance of the package has been realized.

Methodology

A package power supply system can be divided into two parts based on the function such system carries on: to provide a high quality power supply to the device that mounted on the top of the package. The two parts are DC IR drop and high frequency power ground input impedance.

The DC IR drop analysis of the package power supply system has become a critical requirement in the design of high speed and high performance programmable logical device. The DC IR drop of a power supply system can be divided into three parts along it path from power supply source (the VRM module) to the IC circuits. They are on-die IR drop, on-package IR drop, and on-board IR drop. Usually, the on-board IR drop can be ignored since large plane structures are used for power supply systems on a printed circuit board. On the other hand, the on-die DC IR drop has been well studied, since the resistive loss is severe in the die environment. However, not much attention has been paid to the on-package IR drop analysis since with standard flip chip packages, DC IR drop was tolerable when chip power supply voltage was above 1.8 Volt on 0.13 μm technology. The switch to 90 nm technologies has resulted in greatly reduced power supply voltages (1.2 V and below), switching thresholds, and noise margins. As a result, the DC IR drop analysis in package substrate has becoming an important factor, and is no longer can be ignored by IC circuit design engineers.

The high frequency power ground input impedance is usually preferred to be low so that high frequency noise can be decoupled to the ground. An ideal power supply system can be thought as a two-port network system and such system has a low pass performance that only DC signal can be passed and all other high frequency signals will be blocked. Performing accurate analysis and improving the power supply system performance is becoming more and more important and a challenging task for a package designer.

For DC IR drop analysis, since there is no coupling between the power and the ground, the power and the ground structures can be separated and therefore, a dense mesh discretization can be applied so that the commercial software can recognize those details in the plane shapes. A voltage or current source is then connected to the top and the bottom of the package structure. Correspondingly the current or the voltage is "measured" in the simulation carried by the software. Such "measurement" can be made between each individual bump (on top of the package) and each individual ball (on bottom of the package); or between a group of bumps and a group of balls. Meanwhile, the current distribution on the power or the ground plane has been recorded after the "measurement". Based on the current distribution, certain modifications on the plane shape, via placement are made to improve the package power supply system DC performance.

Figure 1 shows the DC IR drop lab measurement setup. A HP 4338B m-ohmmeter and 4 probe measurement technique; high accurate DC resistance is measured between different specified bumps and balls. The results are then compared with simulation results.

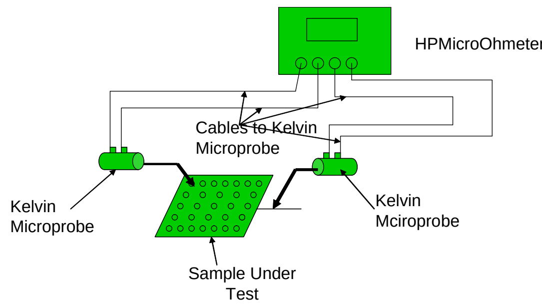

Figure 1. DC IR drop measurement setup

For high frequency power ground input impedance study, two kinds of power ground input impedance measurements were made at specific bump and ball locations by using Agilent 8753ES Vector Network Analyzer from 30 KHz to 2 GHz. The first kind measurement was made from a pair of bumps on top of the package and a pair of balls on bottom of the package with all other bumps and balls open; the second kind measurement was made by shorting all the balls on the bottom of the package and making a Kelvin type measurement at a power-ground bump pair on top of the package with both probes sitting on the same pair. Both measurement results are compared with simulation results, and an equivalent circuit model for power supply system of the package is then generated for time domain simultaneous switching noise analysis.

For high frequency power ground input impedance simulation, the package layout file is first translated into the format that can be read by the commercial power integrity analysis software. After making simulation setup, a two-port power ground network scatter parameters are obtained and then compared with the measurement results. Simple RLC equivalent circuit models are also generated for the power supply system and can be used in time domain simulations. As what has been done for DC IR drop analysis, based on the power ground input impedance profile, and carefully study of package layout, certain modifications on the plane shape, via placement are made to improve the package power supply system for high frequency applications.

Results

DC IR Drop Analysis

A layout of the plane inside the package is showing in Figure 2 with many vias coming from the bumps on top of the package and going down to the balls on bottom of the package. The package is a standard buildup with a core layer, which has larger via dimensions. Such feature has created a lot of voids under the die area and the quality of the plane continuity varies from left side to right side.

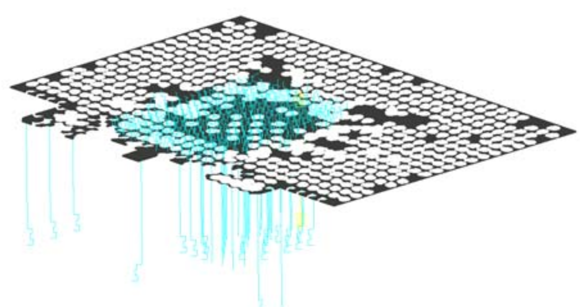
Figure 2. Package power structure

The measurement and simulation results from individual bump (on top of the package) to ball (on bottom of the package) are shown in Table 1. One can see that good correlation of the DC IR drop package resistance has been established with the lab measurement.

Figure 3 shows the current distributions on the plane with different excitation situations. The one on the left is one point excitation, which means only one bump is connected with a current source; the one on the right is lumped full excitation, which means all the bumps are lumped together and connected with a current source.

Table 1. Resistance comparison between measurement results and simulation results

Bump Name	Ball Name	Resistance Measured (mΩ)	Resistance Simulated (mΩ)
I23	AG10	32.7	40.0
I23	T19	26.7	28.0
Q12	AG10	32.5	31.0
Q12	T19	16.5	18.0
AG11	AG10	24.9	30.0
AG11	T19	18.9	18.0
AY0	AG10	31.8	37.0
AY0	T19	25.8	25.0

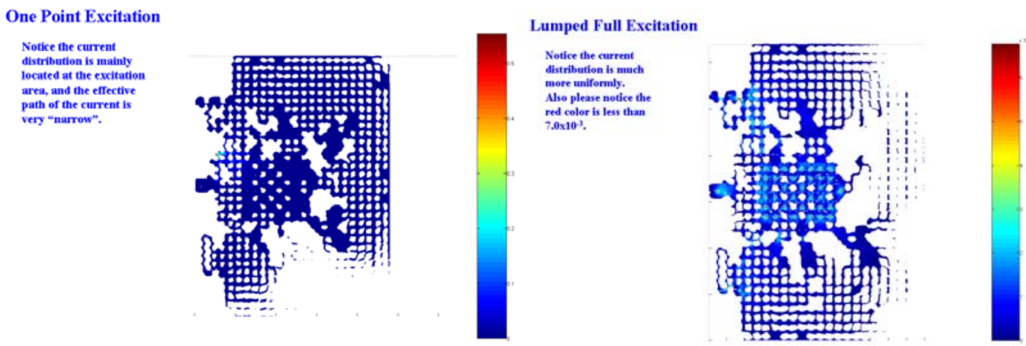

Figure 3. Current distribution on the plane with different excitation situations.

One can see that for one point excitation, the excitation location is very "hot"; and the current distribution for lumped full excitation is more uniform and the magnitude of the current density is much less than that for one point excitation. With both one point excitation at different locations and different lumped excitations, some hot spot on the plane can be identified and correspondingly the plane shape can be modified and more vias are placed at that location to provide a better current path.

High Frequency Power Ground Input Impedance Analysis

The package power ground input impedance has also been correlated between measurement and simulation for specific selected bumps and balls. Two port scattering parameters are obtained and compared with each other. Figure 4 shows such comparison. The left upper one is magnitude of S11 and the left lower one is phase of S11; the right upper one is magnitude of S21 and the right lower one is phase of S21. One can see that they are very close to each other.

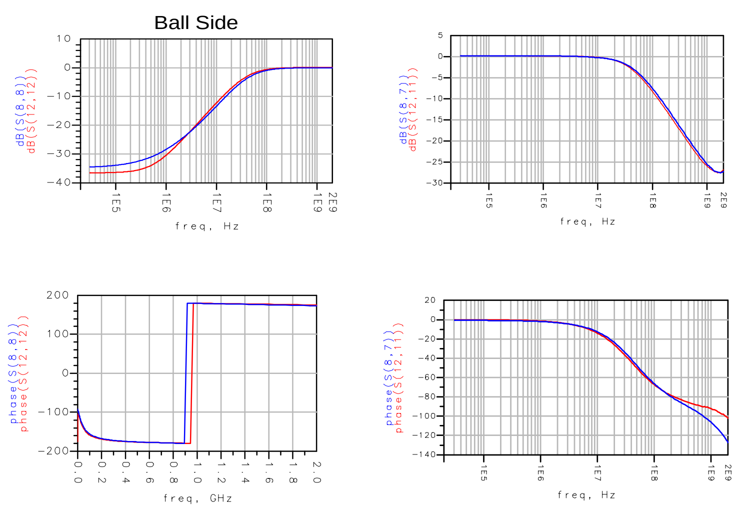

Figure 4. Comparison of scattering parameters from measurement (Blue) and simulation (Red).

There are some discrepancies in the phase that basically translates to a difference in the resonant frequencies. This is being investigated at the measurement and simulation levels.

The computed results, especially the current distribution on the planes inside the package were then used as an input for creating package design rules and guidelines for the next generation of high performance programmable logical device packages. The design rules and guidelines allow engineers to lay out power planes, optimize stackup, via connections and C4 bumps and pin balls placement to reduce both the DC IR resistance and high frequency power ground input impedance.

As an example, figure 5 shows a design improvement of the power ground input impedance for both core area power supply and I/O power supply. The original package has 6 layers and the I/O power plane has non-optimal performance. As an improvement, more layers are added to the package in addition to moving the layer and the location of the power plane. Such modification improves the input impedance significantly. Further improvements are also made to the next generation package by optimizing the power, ground, and signal pin balls arrangement.

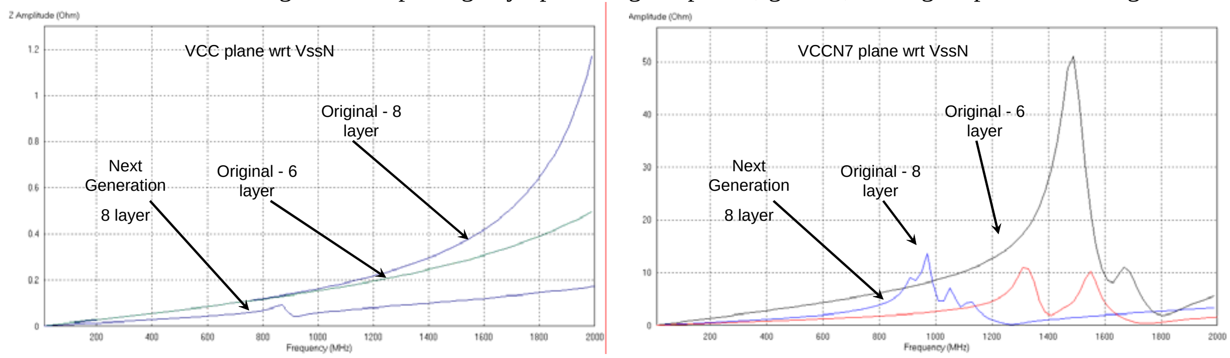

Figure 5. Design improvement has been made for both core area power supply and I/O power supply. Note the different scales on the 2 plots.

Table 2. Improvement in Input Impedance

Case (VCC plane)	Zin (Ω) (510 MHz)	Zin (Ω) (990 MHz)	L (nH) (510 MHz)
Original 6 layer	0.07	0.15	0.02
Modified 8 layer	0.07	0.16	0.02
Next generation 8 layer	0.04	0.06	0.01

Case (VCCN7 plane)	Zin (Ω) (510 MHz)	Zin (Ω) (990 MHz)	L (nH) (510 MHz)
Original 6 layer	3.67	8.45	1.14
Modified 8 layer	1.62	8.45	0.51
Next generation 8 layer	1.08	2.58	0.34

Conclusion

A methodology for modeling, analysis, and design for package power delivery system has been demonstrated. The analysis data are used for developing the design rules and guidelines for the next generation package design. Further work will be focus on time domain simulations on both the original package design and the improved package design.

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Reference

[1] High Bandwidth Measurement techniques for Low Inductance Structures, Dr. Eric Bogatin, 2003 Design Con Tech Forum on Power Distribution Design.
[2] Package_IRdrop_Resistance_Dist, Sigrity, Inc. Application Notes.