

Frequency Dependencies of Power Noise

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Abstract—In this paper, frequency dependencies of delta- I noise caused by variations of the on-chip switching activity have been analyzed by simulations for a complex computer system board with multi-chip module, especially the impact of coincidences with resonances of the power distribution system. The switching frequency and the noise source waveform have been varied in case of a single delta- I step. For repeated delta- I steps the power noise dependencies on the repetition frequency, the duty cycle and the damping of the resonant loop have been analyzed. Simulations using switching current sources for on-chip switching have been confirmed by simulations with switching resistors plus dc voltage source. Mid-frequency noise simulations using SPEED2000 and noise voltage measurements yield the same results within 6% for the first and second voltage droops and overshoots, if the real resistance of power/ground vias and module pins are included in the simulation.

Index Terms—Decoupling capacitor, delta- I noise, power distribution, power supply noise, resonances.

I. INTRODUCTION

THE SWITCHING activity and therefore the average current demand of microprocessor complimentary metal oxide semiconductor (CMOS) chips can change within a few nanoseconds causing power supply noise (delta- I noise). The power distribution system must have a low impedance over a wide frequency range which has to be achieved by placing power supply decoupling capacitors [1]–[5]. Decoupling capacitors sink and source extra charge after switching activity variations until the primary system power supply with the voltage regulator module responds. However, all capacitances on the chips and package, including the decoupling capacitors and module and card power/ground plane capacitances, and all parasitic inductances of capacitors and interconnections create also resonant RLC-loops, which cause delta- I power supply noise in the mid- and low-frequency range [1], [3], [6], [7].

In this study, frequency dependencies of delta- I noise caused by on-chip switching activity variations have been analyzed for an IBM zSeries 900 system board with multichip module (MCM). The software tool SPEED2000 from Sigrity, Inc. [8] has been used for the simulations, which is based on the FDTD (finite-difference time-domain) method. Time-domain simulations with an appropriate chip and package model directly yield noise voltage values which allow an early checking of specified noise margins. This work started before August 7, 2001, when SPEED2000 assumed zero via resistance during simulations

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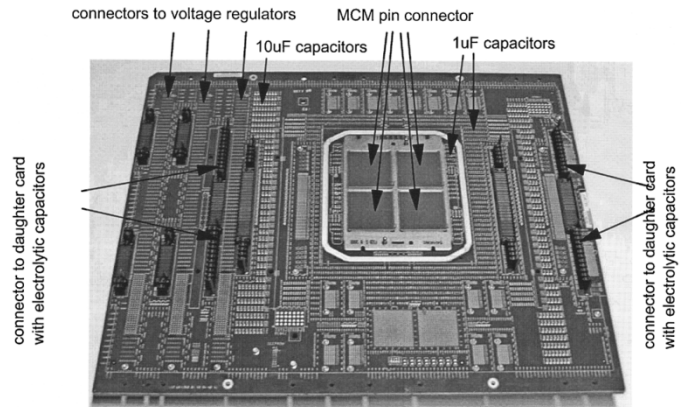


Fig. 1. Picture of the IBM zSeries 900 processor board. Courtesy of H. Pross, IBM Boeblingen.

TABLE I
NUMBER AND PARAMETERS OF DECOUPLING CAPACITORS AS USED
IN THE SIMULATIONS, IF NOT OTHERWISE STATED

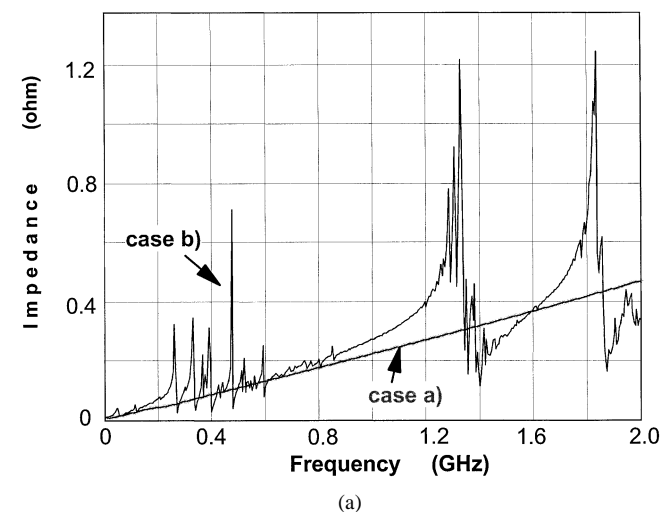
on-chip (total for 30 chips)	7.4uF (approx. 0nH, RC average 100ps)
on-module	275 x 150nF @-10C (30pH, 30mohm, AVX T60T)
on main board (board size: 55cm x 45cm)	2886 x 1uF (1nH, 7mohm, size 0805) 670 x 10uF (1nH, 1.5mohm, size 1210)
on voltage regulator cards and on daughter cards	464 x 1.2mF (7nH, 29mohm)

[8]. Additional simulations have been made with via resistance using a newer SPEED2000 version (build #1002174). The results are presented in Sections III-E and IV.

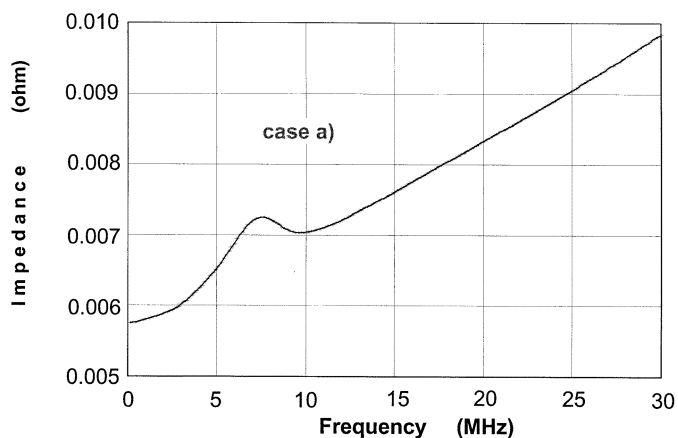
The impedance of the power distribution system as a function of frequency has also been determined with SPEED2000 using a single (10 GHz Gaussian) current pulse for excitation and taking the ratio of Fourier transforms of source voltage and via current as described in [5] and [9].

II. PACKAGE DESCRIPTION

The MCM has a size of 127 mm \times 127 mm and 30 chips with 700 A nominal average current at 1.6 V supply voltage. Fig. 1 shows a picture of the board which has a size of 55 cm by 45 cm. In Table I all decoupling capacitors are listed, which are located on the chips, on-module, on-board, on daughter cards and on the voltage regulators for high-frequency, mid-frequency, and low-frequency decoupling. These decoupling capacitors and the power distribution of the board and MCM, without on-chip



(a)



(b)

Fig. 2. Input impedance of the power and ground system observed from the MCM top surface at vias in the MCM center with on-chip, on-MCM and on-board decaps (case a), and without any decoupling capacitors (case b).

power distribution, are included in the simulation. In [10] and [11], the simulation methodology and simplifications are described in detail. A smaller capacitance value has been used for the module capacitors in Section III compared with the previous work in order to increase the oscillation frequency f_2 (see Section III-B) and to reduce the required simulation time.

III. SIMULATION RESULTS

A. Impedance as Function of Frequency

Fig. 2(a) shows the input impedance of the power and ground system observed from the MCM top surface at vias in the MCM center in two cases:

- with all on-chip, on-MCM and on-board decoupling capacitors as described in Table I;
- without any decoupling capacitors. The impedance curve shows several large peaks in case b).

However, it is a smooth function of frequency and below 0.25 GHz between 0 GHz and 1 GHz in case a). There only a small impedance peak of 0.007Ω is visible at 7.5 MHz [Fig. 2(b)] and a tiny “bump” at 175 MHz [Fig. 2(a)], which correspond to the oscillation frequencies f_2 and f_1 described in the next section.

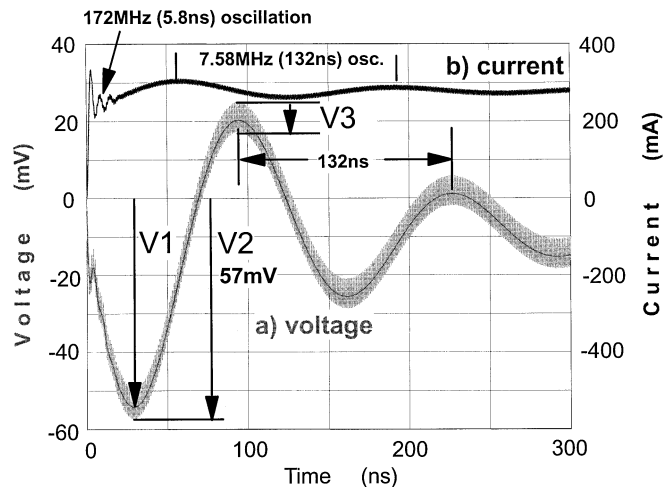


Fig. 3. Voltage at a source in the MCM center and current flowing from the source into one MCM via versus time, after all sources start continuously switching at time zero with 1 ns cycle. V_1 denotes the mid-frequency noise amplitude, V_2 the peak noise and V_3 the high-frequency peak-to-peak noise. The MCM decap capacitance equals 150 nF.

B. Power Noise Voltage and Current Oscillations and Definitions

At first the core on-chip switching of 30 chips has been represented by 504 current sources which are connected to power/ground vias at the MCM top surface as in [11]. The major assumptions and definitions are briefly repeated. Each current source has one RC element in parallel ($6.8 \text{ m}\Omega$, 14.6 nF , 100 ps RC time constant). These represent the on-chip decoupling capacitors which are assumed to have zero inductance. Fig. 3 shows the voltage at a source in the MCM center and the current flowing from the source into one MCM via, after all sources start switching at time zero with 1 ns cycle. Each current pulse has 200 ps rise- and 800 ps fall-time and 555.6 mA peak current (Fig. 9, curve a). In this section, the ΔI step is assumed to go from zero to 20% (140 A for the total MCM) of the nominal average (continuous) current.

The voltage and current curves in Fig. 3 show three oscillations.

- A high-frequency oscillation with the same frequency f_3 (1 GHz in Fig. 3) as the current sources. In the following sections the high-frequency peak-to-peak noise is taken over one switching cycle at the maximum of the voltage curve and denoted voltage “ V_3 .” A moving average calculation is used to eliminate the high-frequency oscillation and to determine the mid-frequency noise amplitude V_1 as shown in Fig. 3.
- A mid-frequency oscillation with a frequency $f_1 = 172 \text{ MHz}$ (5.8 ns period). The voltage curve shows this oscillation more clearly, if the source switching frequency is lower than f_1 , e.g., for a single switching event. As pointed out in [11], this oscillation is caused by the “horizontal” resonant loop formed by the on-chip decoupling capacitors, the adjacent on-MCM ceramic decoupling capacitors, and the effective loop inductance and resistance between these two sets of capacitors. This mechanism is supported by the linear dependency

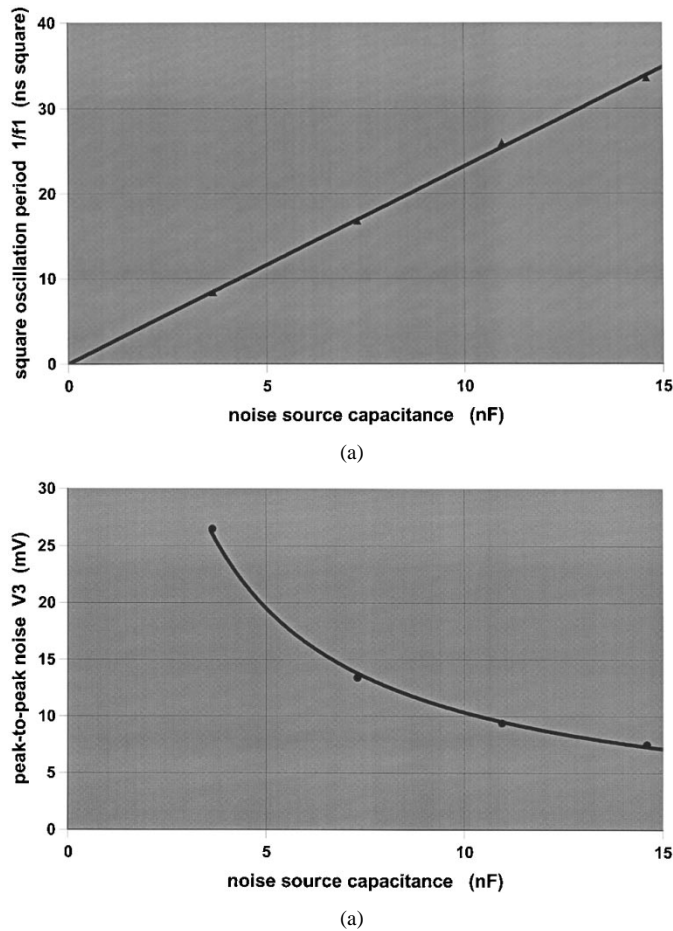


Fig. 4. (a) Square of the oscillation period $1/f_1$ and (b) high-frequency peak-to-peak noise V_3 versus source capacitance. The switching frequency is 1 GHz. The source capacitance is decreased from the 14.6 nF (normal value) to 75%, 50% and 25% of the normal value.

between the square of the oscillation period $1/f_1$ and the source capacitance [Fig. 4(a)], which is expected, if the on-chip capacitance is small compared to the capacitance of the adjacent on-module ceramic capacitors.

- 3) A second mid-frequency oscillation with a frequency $f_2 = 7.58$ MHz (132 ns period) and an amplitude denoted V_1 . This oscillation is caused by the “vertical” resonant loop formed by all capacitors (on-chip and on-module) connected to the module top surface, the board decoupling capacitors, and the effective loop inductance and resistance between the two sets of capacitors. The impact of variations of decoupling capacitances and loop inductance on the mid-frequency noise amplitude V_1 and on the resonant frequency f_2 has been studied in [11].

Finally the peak noise V_2 is defined in Fig. 3.

C. Variations of the Switching Frequency

Fig. 5 compares the noise voltage at a source in the MCM center for 1 GHz and 172 MHz switching frequency. The shape of the current pulses (peak current, rise- and falltime) is the same for both switching frequencies. The peak-to-peak voltage V_3 is larger and the mid-frequency noise amplitude V_1 is smaller

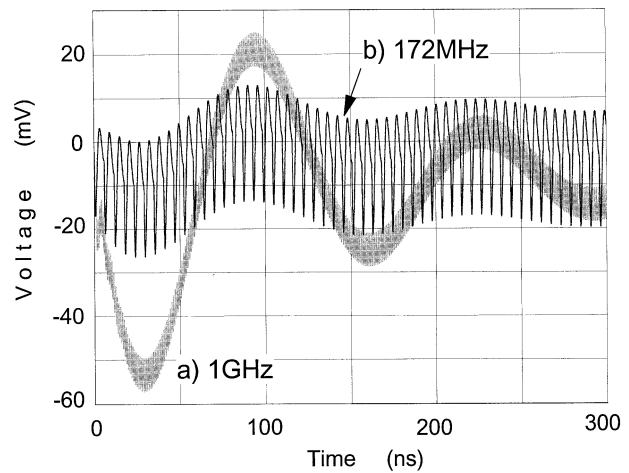


Fig. 5. Voltage at a source in the MCM center versus time, after all sources start continuously switching at time zero with (a) 1 GHz, 1 ns cycle and (b) 172.4 MHz, 5.8 ns cycle.

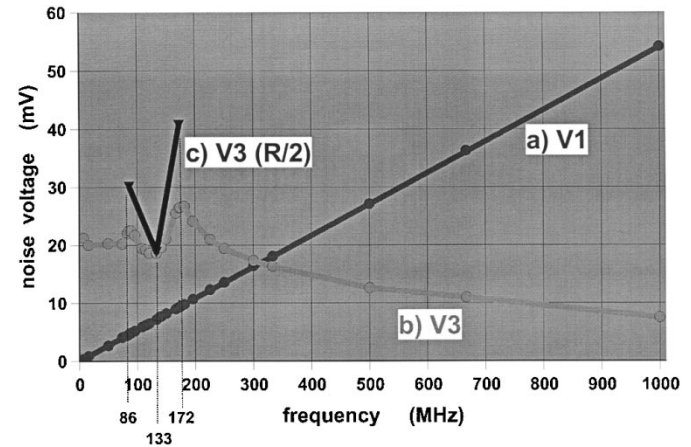


Fig. 6. (a) Mid-frequency noise amplitude V_1 , (b) peak-to-peak noise V_3 , and (c) versus switching frequency of the current sources. The peak-to-peak noise V_3 is always taken over one switching cycle. The triangles indicate simulations with doubled MCM power/ground plane conductivity, and source and module capacitor resistance cut to half.

for the smaller switching frequency. This is explained in the following paragraphs.

In Fig. 6 V_1 (curve a) and V_3 (curve b) are plotted versus the switching frequency of the current sources in the range from 7.58 MHz and 1 GHz. V_1 is proportional to the switching frequency, because V_1 is proportional to ΔI and ΔI is in these simulations proportional to the switching frequency, since the waveform of the current pulses has not been changed. This is normally true also in reality. V_1 shows no peak at the resonant frequency $f_2 = 7.58$ MHz, where ΔI is very small.

As expected, the high-frequency peak-to-peak noise V_3 has maximum values for the resonant frequency $f_1 = 172$ MHz and for 86 MHz (50% of f_1). V_3 increases further at these frequencies, if the damping of the resonant circuit is reduced, e.g., by doubling the conductivity of the MCM power/ground planes and by cutting the resistance of the source and module capacitors to half (Fig. 6, curve c). The resistance reduction has negligible impact on the mid-frequency noise amplitude V_1 at these

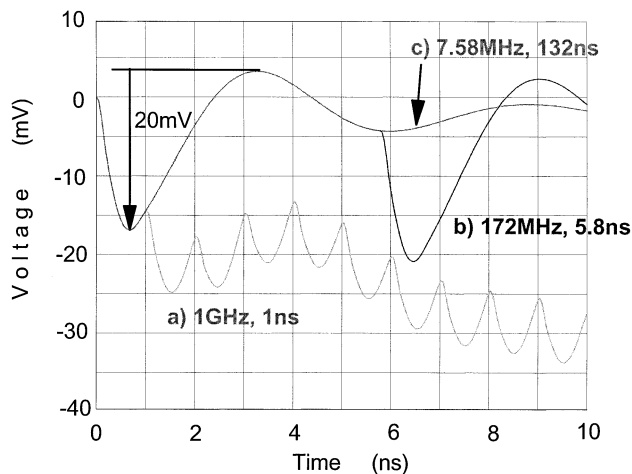


Fig. 7. Voltage at a source in the MCM center versus time, after all sources start continuously switching at time zero with (a) 1 ns, (b) 5.8 ns, and (c) 132 ns switching cycle.

frequencies, because $V1$ is determined by the “vertical” and not by the “horizontal” resonant loop.

A method has been described in [12] to avoid the coincidence of a package resonant frequency with the chip switching (clock) frequency by on-chip decoupling capacitance tuning. Thereby the peak-to-peak noise is reduced.

With decreasing switching frequency the voltage $V3$ approximates the $V3$ value of a single current pulse (20 mV), which is primarily determined by the first voltage drop (Fig. 7). This can be estimated with the current from each source (I_{source}), the current flowing into the package ($I_{package}$) and the voltage drop U_R across the RC element parallel to each source ($R = 6.8\text{ m}\Omega$, $C_{source} = 14.6\text{ nF}$) as follows:

$$U = \frac{1}{C_{source}} \cdot \int_0^{1\text{ ns}} (I_{source} - I_{package}) dt + U_R \quad (1a)$$

$$U \leq \frac{0.5\text{ ns}}{C_{source}} \cdot I_{peak} - I_{peak} \cdot R. \quad (1b)$$

Equation (1b) yields $U \leq 23\text{ mV}$ for $I_{peak} = 0.5556\text{ A}$ source peak current, in good agreement with the simulation.

The decrease of the peak-to-peak noise $V3$ with increasing switching frequency above the resonant frequency $f1$ is correlated with two assumptions.

- 1) The source (on-chip) decoupling capacitors have zero inductance and the effective loop inductance of the chip power distribution is negligible; the latter assumption is not adequate for small signal rise times [13], [14].
- 2) The time dependency (waveform) of the switching currents is independent of the switching frequency, which is true in reality in many cases.

However, if e.g., the current rise- and falltime are increased for longer switching periods so that there is no deadtime, and the peak current is assumed to be proportional to the switching frequency, then

- 1) the mid-frequency noise amplitude $V1$ still does not change as shown e.g., in Fig. 8, because the charge delivered by the sources in each cycle does not change;

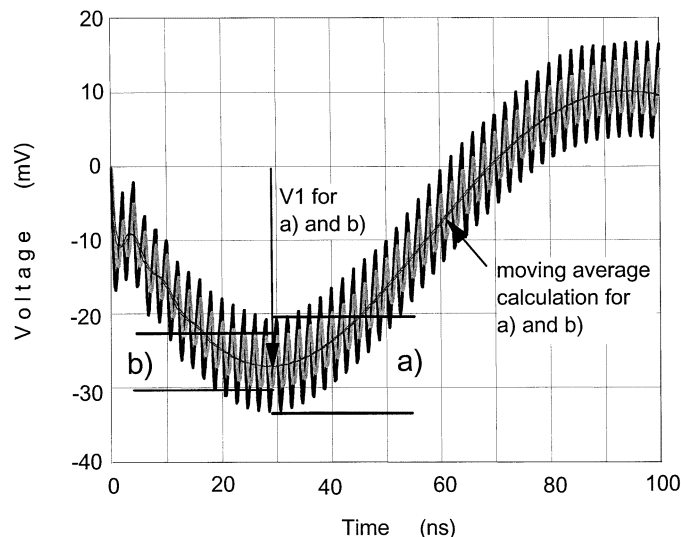


Fig. 8. Voltage at a source in the MCM center versus time, after all sources start continuously switching at time zero with 2 ns cycle. Each current pulse has 200 ps rise- and 800 ps falltime, 555.6 mA peak in case (a), and 400 ps rise- and 1600 ps falltime, 277.8 mA peak in case (b).

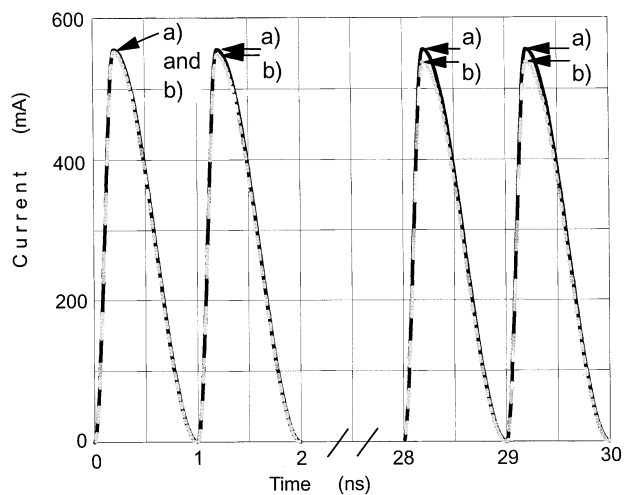


Fig. 9. (a) Source current in case of switching current sources and (b) current through a resistor in the MCM center in case of switching resistors. The continuous switching starts at time zero with 1 ns switching cycle.

- 2) $V3$ decreases with decreasing switching frequency, because more current flows into the package during each cycle and less through the RC parallel to each source. In this case $V3$ equals 1.5 mV at 15 MHz, which is only 8% of the $V3$ value for constant current pulses. In case b) in Fig. 8 $V3$ is 45% smaller than in case a).

The current waveform depends also on the delays between the various switching events in reality.

For 1 GHz the simulation can be compared with a simple calculation. It has been shown in [11], that for 1 GHz switching frequency and 200 ps rise- and 800 ps fall-time, the current flowing through each of the 6.8 mΩ resistors and the 14.6 nF capacitors (parallel to each source) oscillates almost symmetrical around zero after the 172 MHz oscillations has been damped away, which is the case 20 ns after the ΔI step occurred (Fig. 3). Then the peak-to-peak amplitude I_0 of this

capacitor current equals the peak current of each current source (555.6 mA). Therefore the peak to peak voltage V_o across one RC element can be calculated for 1 GHz by

$$V_o = I_o \sqrt{R^2 + \left(\frac{1}{\omega \cdot C}\right)^2}. \quad (2)$$

For $R = 6.8 \text{ m}\Omega$, $C = 14.6 \text{ nF}$, $\omega = 2\pi \cdot f$, $f = 1 \text{ GHz}$ and $I_o = 555.6 \text{ mA}$ equation (2) yields $V_o = 7.1 \text{ mV}$, which is very close to the 7.5 mV obtained for V_3 at 1 GHz by simulation.

It should be emphasized, that the on-chip (high-frequency) peak-to-peak noise V_3

- 1) is not effected by the package properties in the high frequency range above the resonant frequency f_1 ; there it is strongly effected by the on-chip decoupling capacitance—as indicated by the simulation results shown in Fig. 4(b) and also by equation (2)—and the on-chip power distribution properties;
- 2) is effected by the package properties (loop inductance and resistance, MCM decap capacitance), the on-chip capacitors and on-chip power distribution, if the switching frequency coincides with the frequency f_1 of the “horizontal” resonant loop;
- 3) is proportional to the current; therefore V_3 is five times larger for the nominal MCM current (700 A) compared with the 20% value in the simulation.

D. Reversal of Current Flow

The 504 current sources representing the core on-chip switching activity have been replaced by switching resistors and the shorting vias at the connector to voltage regulators have been replaced by dc voltage sources of 1.6 V. Then the direction of the simulated current flow is the same as in reality. The resistors switch with the core switching frequency between 2.88Ω and 6000Ω so that the waveform of the current flowing through each resistor during the first switching cycle is the same as in case of switching current sources and the delta- I step is again from zero to 20% of the nominal current [Fig. 9, curves a) and b)]. The switching resistors yield almost the same voltage oscillations (Fig. 10), but the simulation speed is 10 times smaller. The mid-frequency noise amplitude V_1 is 3% smaller than for switching current sources, because the peak current is 3% smaller in the time range from 28 ns to 30 ns (Fig. 9) due to the voltage reduction by approximately 3% at the switching resistors in this time range.

It is expected that switching resistors with more current load (e.g., 100%) provide more parallel damping of the mid-frequency oscillation than with 20% current load. This is further investigated in Section IV.

E. Delta- I Repetitions

So far the effects of one delta- I step (at time zero) have been studied, that means the delta- I repetition frequency was zero. In reality increase and decrease of the switching activity can alternate. Therefore the effect of repeated delta- I steps has been analyzed and the repetition frequency as well as the ratio between

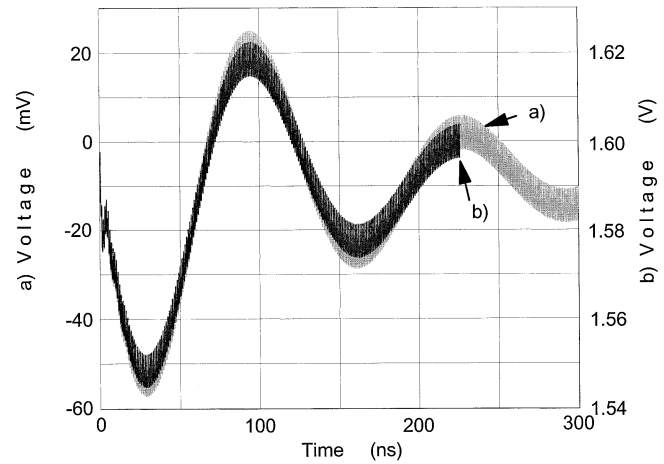


Fig. 10. (a) Voltage at a current source in case of switching current sources and (b) at a switching resistor in case of switching resistors in the MCM center. The continuous switching starts at time zero with 1 ns switching cycle.

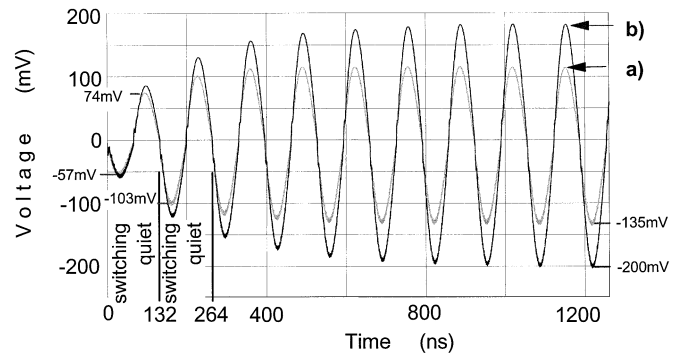


Fig. 11. Voltage at a switching current source in the MCM center for repeated delta- I steps. All vias are assumed to have zero resistance during the simulations. Case (a): normal plane conductivity and capacitor resistance, case (b): doubled conductivity of board power/ground planes and half resistance of source, module and board decaps.

active (switching) and quiet time periods (duty cycle) has been varied. Moreover, the effective loop resistance has been varied. Current sources are used with zero current during the quiet and with 20% of the nominal current during the switching (1 GHz) periods.

Fig. 11, curve a) shows the noise voltage curve for the coincidence of the delta- I repetition frequency with the resonant frequency f_2 (7.58 MHz, 132 ns period) and duty cycle 0.5. The first voltage droop (peak voltage V_2) equals 57 mV which is the same as in Fig. 3. The current sources stop switching after 66 ns. The first voltage overshoot amounts 74 mV compared with 25 mV in case of continuously switching sources (Fig. 3). After 132 ns the current sources start switching again and the second voltage droop peaks at 103 mV. Finally the 10th voltage droop peaks at 135 mV, which is $2.4 \times 57 \text{ mV}$.

Again the noise voltage in case of resonance depends on the damping of the resonant circuit. The curve b) in Fig. 11 has been obtained for doubled conductivity of the board power/ground planes and half resistance of the source, module and board decaps. There the 10th voltage droop peaks at 200 mV. The MCM and board vias and the MCM pins have zero resistance in case a) and b), because these simulations were done with an “old” SPEED2000 version before August 7, 2001. Additional

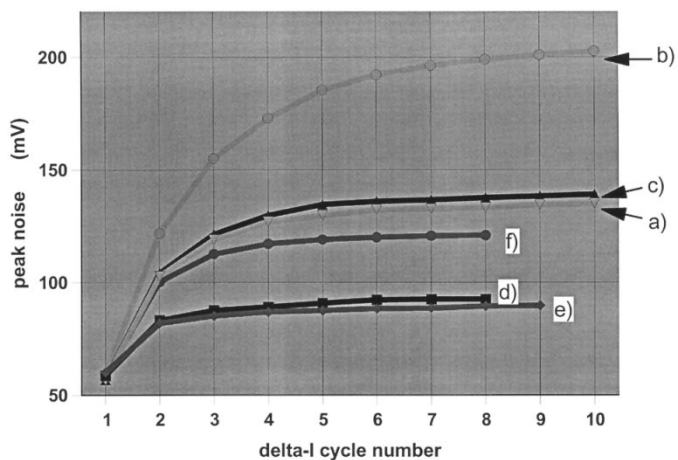


Fig. 12. Peak noise “ V_2 ” (definition in Fig. 3) at a current source in MCM center versus delta- I cycle number for various resonant loop damping: (a) normal board plane conductivity and decap resistance, zero via and pin resistance (corresponding to Fig. 11, curve a), (b) doubled conductivity of the board power/ground planes and half resistance of the source, module and board decaps, zero via and pin resistance (corresponding to Fig. 11 curve b), (c) doubled board plane conductivity, normal decap resistance, zero via and pin resistance, (d) normal plane conductivity and decap resistance as in case (a), but simulation with real via and MCM pin resistance. (e) Conditions as for case (d), but resistance of the $1 \mu\text{F}$ board decaps increased from 0.007Ω to 0.06Ω . (f) Conditions as for case (a), but resistance of the $1 \mu\text{F}$ board decaps increased from 0.007Ω to 0.06Ω . The delta- I repetition frequency equals 7.58 MHz (132 ns time period), the duty cycle 0.5 , and the switching frequency during the active periods 1 GHz .

simulations have been made with via resistance using a newer SPEED2000 version.

Fig. 12 shows the peak voltage “ V_2 ” (definition in Fig. 3) versus the delta- I cycle number for 7.58 MHz delta- I repetition frequency (resonant condition), 0.5 duty cycle and different damping of the resonant loop, which is described in Fig. 12.

These curves show only small differences for the first voltage droop, but large variations for delta- I repetitions. The following conclusions are drawn.

- 1) The effective board plane resistance of high performance boards with many power/ground planes is so small, that the impact on the resonant damping is negligible [cases a) and c) of Fig. 12].
- 2) It is important to include the via resistance in the simulations [cases a) and d) of Fig. 12]. The module power/ground pins, which are modeled as vias in SPEED, yield the major portion of the effective loop resistance for the vertical resonant loop. The damping is as small as for zero via and pin resistance, if the pin conductivity is increased by a factor 100.
- 3) The increase of the board decap resistance has only a negligible impact on the damping for this package, if the via resistance is included in the simulations [cases d) and e) of Fig. 12].

However, the module and board decap resistance has a large impact on the damping, if the via resistance is zero [cases a), b) and f) of Fig. 12]. Methods to optimize the power distribution impedance profile by optimization of the decap ESR have been reported in [15] and [16].

Fig. 13 shows the maximum peak noise V_2 during 10 delta- I cycles (seven cycles in case of 3.79 MHz) as a function of

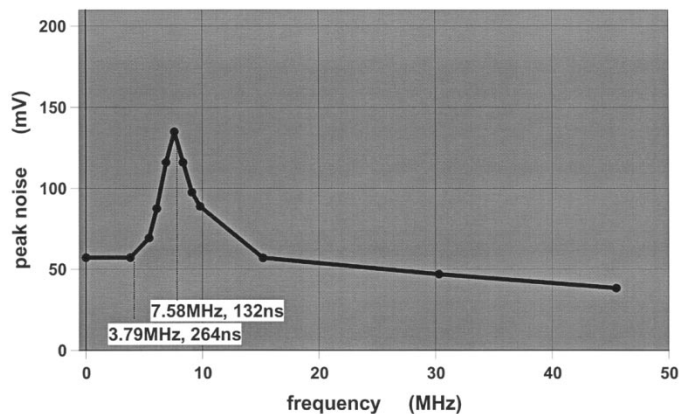


Fig. 13. Max peak noise V_2 at a current source in the MCM center during 10 delta- I cycles (7 cycles in case of 3.79 MHz) versus delta- I repetition frequency. Simulation conditions: 1 GHz source switching frequency, duty cycle 0.5 , zero via resistance, normal board plane conductivity and decap resistance.

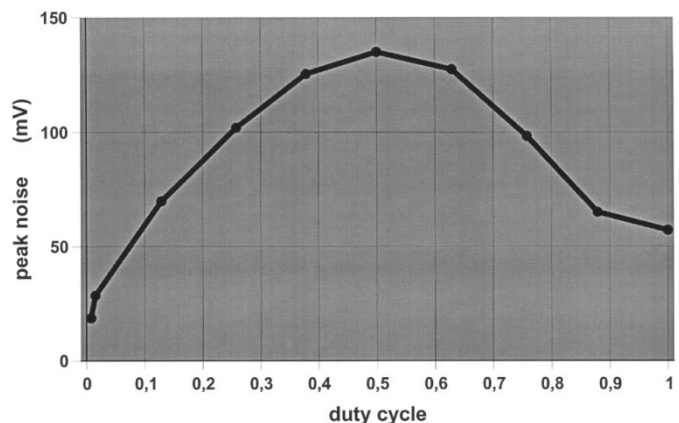


Fig. 14. Max peak noise V_2 at a current source in the MCM center during 10 delta- I cycles versus duty cycle. Simulation conditions: 1 GHz source switching frequency, 7.58 MHz delta- I repetition frequency, zero via resistance, normal board plane conductivity and decap resistance.

the delta- I repetition frequency. The duty cycle is 0.5 . The via resistance is zero and the damping is the same as for case a) in Fig. 12. V_2 equals 57 mV for zero repetition frequency (a single delta- I step) and reaches a maximum value of 135 mV for 7.58 MHz (coincidence with the resonant frequency f_2). For higher repetition frequencies V_2 approaches the peak noise of a single delta- I step with 500 MHz switching frequency due to the 0.5 duty cycle.

The duty cycle has been varied for a constant (7.58 MHz) delta- I repetition frequency and damping as for case a) in Fig. 12. V_2 reaches a maximum, if the duty cycle equals 0.5 (Fig. 14). As expected, V_2 decreases, as the duty cycle approximates zero, because the average current decreases. V_2 decreases down to 57 mV as the duty cycle approaches 1, which represents a single delta- I step.

IV. COMPARISON WITH MEASUREMENTS

In [11], the mid-frequency noise simulations using switching current sources have been compared with noise voltage measurements at the location of the center chip of the MCM for 2 ns switching cycle and a capacitance of the MCM capacitors in the range from 200 nF to 210 nF corresponding to a decap

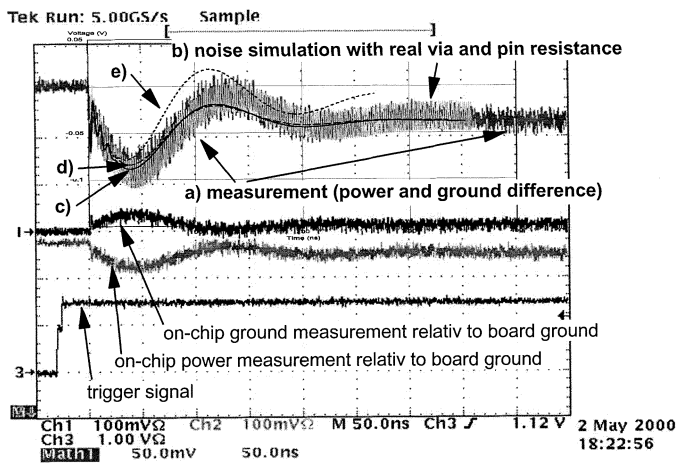


Fig. 15. Comparison between noise measurement (curve a) and simulations (curves b–e) for the chip in the MCM center with 2 ns switching cycle, 210 nF MCM decap capacitance, and 237 A ΔI . The curves c, d, and e are obtained by moving average calculations (2 ns averages). Simulation conditions: (b) real via and pin resistance, 0.5 mm grid, current sources; (c) solid curve: real via and pin resistance, 0.98 mm grid, current sources; (d) dashed curve: real via and pin resistance, 0.98 mm grid, switching resistors; (e) dotted curve: factor 1000 increased MCM pin conductivity, 0.98 mm grid, switching resistors.

TABLE II

MID-FREQUENCY NOISE VOLTAGE VALUES AND TIME VALUES OF THE FIRST AND SECOND VOLTAGE DROOPS AND OVERSHOOTS FOR THE CHIP IN MCM CENTER FOR 237 A ΔI . THE SIMULATIONS ARE DONE WITH 210 nF MCM DECAP CAPACITANCE AND WITH REAL VIA AND MCM PIN RESISTANCE

	first droop	first overshoot	second droop	second overshoot
mid-frequency voltage:				
measurement	91.8mV	12.4mV	44mV	33mV
simulation	93.3mV	11.7mV	42mV	33mV
difference	+2%	-6%	-4%	-0.1%
time:				
measurement	43.4ns	131ns	217ns	305ns
simulation	43.1ns	132ns	227ns	323ns
difference	-0.7%	+1%	+5%	+6%

temperature between 15C and 20C. The ΔI step was for the measurements from 47 A to 284 A and for the simulations from zero to 237 A. The agreement between measurement and simulation was excellent for the first voltage droop. However, the simulation which assumed zero MCM pin resistance exhibited much less damping of the mid-frequency noise oscillation. The simulation has been repeated now for 210 nF MCM decap resistance with real pin and via resistance using the new SPEED2000 version. The agreement between the measurement and the simulation is now excellent for the complete time range of 350 ns as shown in Fig. 15 by the curves a) and b). The mid-frequency voltage values as well as the time values agree within 6% for the first and second voltage droops and overshoots (Table II). The mid-frequency voltage values in Table II are the average of adjacent high-frequency peak voltages.

The curves c), d) and e) in Fig. 15 are moving average calculations obtained from simulations which were done to investigate further the damping of the mid-frequency noise oscillations. A larger grid was used for these simulations (0.98 mm instead of 0.5 mm) to increase the simulation speed. The larger grid changes the mid-frequency oscillation only slightly as shown by curve c) which has the same simulation

conditions as curve b) except of the different grid size. Also the simulation with switching resistors yield almost the same mid-frequency oscillation (dashed curve d). However, the simulation with switching resistors and a factor 1000 higher module pin conductivity (dotted curve e) yield a much smaller damping of the mid-frequency oscillation than the measurement (a) and the simulation with normal pin conductivity (d). This indicates that for the analyzed package and 237 A the module pin resistance dominates the damping compared with the resistive load of the switching resistors. This is reasonable, because all current of the 7.58 MHz mid-frequency oscillation flows through the module pins and most of this current flows through the module decaps and much less through the switching resistors and the on-chip decaps as indicated by the simulations. This is in agreement with the calculated impedance values at 7.58 MHz: 0.4 m Ω , 3 m Ω and 7 m Ω (average) for all module decaps, on-chip decaps and switching resistors, respectively. The module capacitors and module pins provide the largest ohmic resistance in the “vertical” resonant loop (both approximately 0.1 m Ω) and therefore both determine the damping of the 7.58 MHz oscillation.

V. CONCLUSIONS

Time domain simulations yield a significant increase of the ΔI power supply noise, if the on-chip switching frequency or the ΔI repetition frequency coincides with resonant frequencies of the power distribution system. The high-frequency on-chip noise is strongly effected by the package properties (especially the loop inductance and resistance), when the switching frequency coincides with a resonant frequency. In case of ΔI repetitions the mid-frequency noise is largest for duty cycle 0.5 and coincidence with a resonant frequency. The resistance of the module pins, which are modeled as vias in SPEED, must be included in the simulations, if they provide the major portion to the effective resistance of a resonant loop like for the analyzed package.

On-chip switching activity simulations with current sources yield the same mid-frequency noise within approximately 3% as simulations with switching resistors plus dc voltage sources for ΔI steps from zero to 20% of the nominal current, but the simulation speed is 10 times larger.

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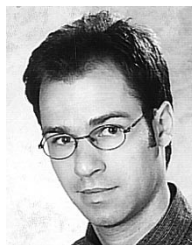


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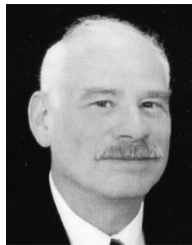
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