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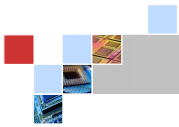
TSMC Selects Sigrity as a Reference Flow 11.0 Partner

Sigrity's XtractIM, OrbitIO Planner, and OptimizePI streamline IC, package and system co-design

CAMPBELL, Calif. – June 29, 2010 – Sigrity, Inc., the market leader in signal and power integrity solutions, today announced that TSMC has included three Sigrity chip, package and system co-design products – XtractIM, OrbitIO Planner and OptimizePI – in its new TSMC Reference Flow 11.0. Companies that rely on TSMC flow support now can benefit from streamlined IC package assessment, package model extraction, chip/system IO planning, and power delivery system optimization.

“Working closely with Sigrity, we are impressed by both the robust electromagnetic technology at the core of Sigrity tools, and by the company’s focus on making tools that can be readily used by designers,” said ST Juang, senior director of design infrastructure marketing, TSMC. “Incorporating Sigrity technology into the Reference Flow 11.0 enables designers to pinpoint potential reliability risks early and achieve faster time to market.”

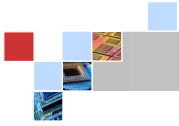
“TSMC long has been recognized for IC manufacturing leadership and for providing practical design flow guidance for complex semiconductor products,” said Raymond Y. Chen, senior VP of engineering at Sigrity.



“We are delighted to collaborate with TSMC to offer designers targeted solutions for rapid assessment of issues, and improved performance in chip, package and system-level designs.”

Sigrity’s XtractIM, OrbitIO Planner, and OptimizePI products included in TSMC Reference Flow 11.0 offer unique capabilities for customers.

- XtractIM provides an intuitive assessment of IC package performance that enables early identification of potential problems when changes can be made efficiently. It supports all package designs, including single die BGAs and multi-die SiP implementations. It accurately models wirebond and flip-chip interconnects and also supports leadframe designs. The package model extraction capability in XtractIM produces single-stage IBIS and SPICE models as well as package models that are reliable over broadband frequencies. The package models can be connected to chip and board models easily for further chip/system signal- and power-integrity analysis.
- OrbitIO Planner gives designers visibility into complex physical IO interactions. It simplifies chip-level IO pad ring design tasks and supports RDL routing. For designs with multiple chips and packages, including those with stacked implementations, OrbitIO Planner also supports IO trade-offs across multiple structures for rapid route feasibility studies and overall system improvement.
- OptimizePI offers targeted power delivery system improvement with a high degree of automation to support IC package and system-level decoupling capacitor optimization. Chip-level data can be incorporated with package and system data in OptimizePI for automatic performance and cost optimization of the total design across the chip, package and system to meet customer targets efficiently.



About Sigrity

Sigrity, Inc., a privately held U.S. company incorporated in 1998, delivers advanced software solutions for package physical design and for analyzing power and signal integrity in chips, packages and printed circuit boards. Sigrity's patented electrical analysis methodologies run orders of magnitude faster than general purpose electromagnetic tools, helping leading companies in the semiconductor, computer, graphics, communications and networking industries ensure high performance and reduce time to market. The company is headquartered in Campbell, Calif., with direct sales and global distribution through worldwide representatives. For more information about how to ensure operational designs by using Sigrity's package physical design and power and signal integrity analysis solutions, please visit: <http://www.sigrity.com>.

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