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**Sigrity Takes High-Speed Chip-to-Chip Analysis to the Next Level with SystemSI**

*Comprehensive new environment reduces design time, provides first parallel bus analysis solution to fully consider impact of SSN on timing closure*

**CAMPBELL, Calif. – June 1, 2011** – [Sigrity](http://www.sigrity.com), Inc., the market leader in signal and power integrity solutions, today announced the [SystemSI](http://www.sigrity.com)<sup>™</sup> family of signal integrity analysis solutions – the industry’s first comprehensive environment for end-to-end simulations of high-speed signal interfaces. Unlike previous approaches that analyze timing margin phenomena in an isolated, piecemeal manner to predict overall margins, Sigrity’s SystemSI family brings everything together within a single environment to streamline the development of high-speed products. It includes a block-based editor, support for standard modeling formats, automated model connections and highly accurate simulation, resulting in the most realistic assessment of actual system behavior. The SystemSI family of solutions can be used at the pre-layout stage, post-layout stage, or anywhere in-between. SystemSI will be featured in Sigrity’s booth (#2525) at this year’s Design Automation Conference in San Diego, Calif., June 5-10, 2011 and in a webcast scheduled for June 16, 2011.

SystemSI is available in two configurations: SystemSI – Serial Link Analysis, and SystemSI – Parallel Bus Analysis. SystemSI – Serial Link Analysis builds on Sigrity’s capabilities introduced in the company’s award-winning Channel Designer software to fully analyze high-speed SerDes designs. SystemSI – Parallel Bus Analysis brings the same level of automation and accuracy to the design of high-speed bus interfaces such as DDRx (Dual Data Rate) memory interfaces. It enables users to quickly and comprehensively analyze timing margins for DDRx memory interfaces. SystemSI – Parallel Bus Analysis considers multiple effects concurrently, including dielectric/conductor loss, reflections, crosstalk, inter-symbol interference (ISI) and simultaneous switching noise (SSN). End-to-end simulation that accounts for combined signal and power interactions results in a reliable, accurate assessment of system behavior.

“Brocade became an early adopter of Sigrity’s SystemSI – Parallel Bus Analysis software, which we use to perform rapid DDR3 simulations that accurately incorporate crucial power delivery system impacts to ensure we can meet our tight timing margins,” said Shahriar Mokhatarzad, a hardware engineering manager at Brocade. “We use a variety of models in our simulations. It has been very helpful to have a way to convert detailed transistor-level models to power-aware behavioral models. This enables us to efficiently complete simulations that would have been impossible otherwise.”



“With timing margins in the picosecond range, the traditional divide-and-conquer approach for phenomena such as reflections, crosstalk and non-ideal power effects such as SSN fails to support timing closure,” said Ken Willis, marketing manager at Sigrity. “Each effect impacts others in fairly unpredictable ways. Simulation of these effects together emulates actual hardware behavior to give a more realistic picture of timing margins.”

### **Comprehensive Environment, Flexible Use**

The SystemSI product family includes an intuitive block-based editor. For early stage designs, a TLine Editor and Via Wizard are available to facilitate creation of early approximations of system behavior. In this way, design begins at the concept phase with specific, detailed models being swapped in as design work progresses for various transmission line and via configurations. Interconnect models can come from a range of sources including supplier specifications, measured data and models extracted using tools such as Sigrity’s [PowerSI](#). Model connections are automated with Sigrity’s open Model Connection Protocol (MCP) format. Sigrity’s Broadband SPICE provides an efficient way to improve S-parameter models that may have problems such as the low-frequency issues that often exist when measured data is used, and it also improves the accuracy and efficiency of circuit simulation. Device IO modeling is supported in multiple formats, including SPICE sub-circuits, traditional IBIS format, and power-aware IBIS behavioral format.

“For more than 10 years, Sigrity has pioneered electromagnetic analysis solutions that provide the accuracy essential for high-speed designs, combined with efficient simulation runtimes to support rapid design improvement,” said Dr. Jiayuan Fang, president at Sigrity. “SystemSI builds on this expertise by providing a dedicated environment for comprehensive chip-to-chip signal integrity analysis.”

### **Pricing and Availability**

SystemSI – Parallel Bus Analysis is available on Windows and Linux platforms with annual prices starting at \$26,500. A Via Wizard for pre-layout studies, using 3D FEM techniques, is available at prices starting at \$8,000 per year. Sigrity customers who have purchased Channel Designer will receive an upgrade to SystemSI – Serial Link Analysis without charge. New users can purchase SystemSI – Serial Link Analysis with annual prices starting at \$26,500. Those with design needs that include both DDR and SerDes implementations can utilize the SystemSI environment configured to handle both.

### **About Sigrity**

Sigrity, Inc., a privately held U.S. company incorporated in 1998, delivers advanced software solutions for package physical design and for analyzing power and signal integrity in chips, packages and printed circuit boards. Sigrity’s



patented electrical analysis methodologies run orders of magnitude faster than general-purpose electromagnetic tools, helping leading companies in the semiconductor, computer, graphics, communications and networking industries ensure high performance and reduce time to market. The company is headquartered in Campbell, California with direct sales and global distribution through worldwide representatives. For more information about how to ensure operational designs by using Sigrity's package physical design and power and signal integrity analysis solutions, please visit: <http://www.sigrity.com>.

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Image #1: SystemSI – Parallel Bus Analysis. Eye diagrams from comprehensive simulations that include realistic power delivery system (PDS) behavior to accurately assess reflections, crosstalk, ISI and SSN effects.

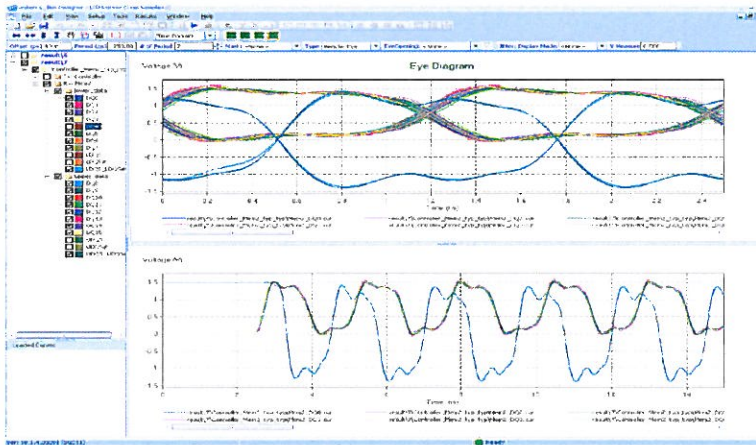


Image #2: SystemSI – Parallel Bus Analysis. Design Topology is synthesized by a wizard to model the complete die-to-die path of high-speed signals together with the PDS.





Image #3: SystemSI – Eye contours showing the impacts of power noise on system reliability.

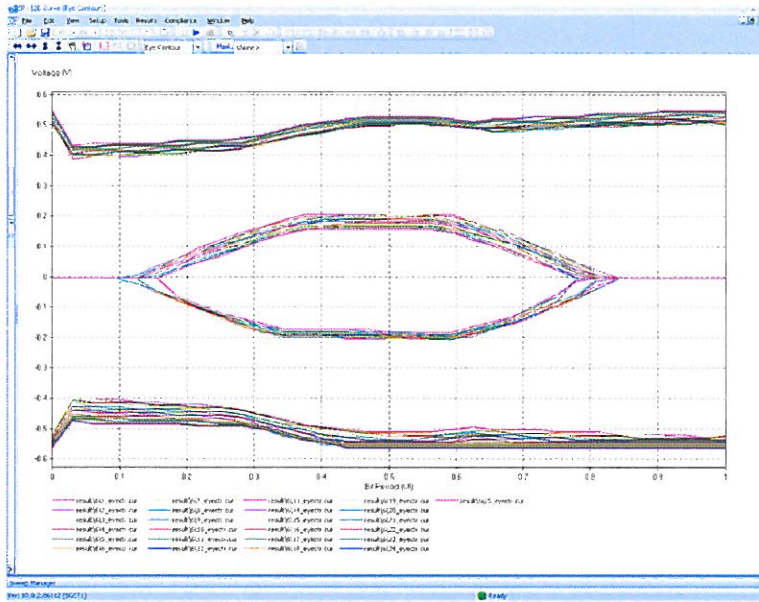


Image #4: SystemSI – Serial Link Analysis. 2D and 3D eye diagrams and bathtub curves enable quick identification of channel issues.

