

## Backgrounder

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### Sigrity and Synopsys Collaboration

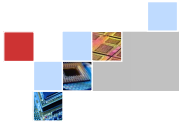
*Signal and Power Integrity Flows including Sigrity Solutions with HSPICE*

January 25, 2012 – Synopsys, inc. issued a press release today focused on the collaboration between Sigrity and Synopsys on flows including HSPICE and Sigrity signal integrity, power integrity and design stage EMI solutions. The companies have worked together for more than 10 years to deliver accurate results and streamlined design flows to address the challenges associated with high-speed designs. A typical design flow relies on Sigrity EM field solvers to generate system level interconnect models. These models along with semiconductor models (transistor level models or IBIS models) are used in a number of signal and power integrity flows that can incorporate HSPICE as an engine.

Sigrity's PowerSI, XtractIM and XcitePI are widely used to extract interconnect models from boards, packages and chip layout databases. Unique Sigrity technology assures that the resulting models include all signal and power integrity impacts. Sigrity generated interconnect models are produced in either Touchstone format or in Sigrity's Broadband Network Parameter Format (BNP) which contains more frequency domain data in a very small file. Synopsys announced support for Sigrity's BNP format with HSPICE 2011.09 using an API which provides for unique communication between the circuit simulator and the EM solver. The result is faster HSPICE simulation throughput, improved accuracy and convergence.

At times, design teams find the S-parameter models they want to simulate in HSPICE are of poor quality. This can be because the model was given to them by a supplier or the S-parameter data was obtained from lab measurements. In such cases, Sigrity's BroadbandSPICE utility checks the quality of S-parameter models and makes causality and passivity improvements paving the way for more efficient HSPICE simulations.

HSPICE can also be used to simulate multiple models that have been concatenated with Sigrity's Model Connection Protocol (MCP) to enable practical and efficient multi-structure simulations such as chip/package co-design projects and full chip-to-



chip channel analysis. Sigrity's SystemSI family provides a comprehensive environment for chip-to-chip analysis of high-speed DDR and SerDes interfaces that accurately incorporates essential power delivery system effects to enable designers to meet tight timing margins. SystemSI can be used both for early pre-layout studies as well as final system sign-off against industry specs. It includes a block based editor, support for standard device and interconnect model formats, automated model connections and highly accurate simulation, resulting in the most realistic assessment possible of actual system behavior. Users can select the either a Sigrity provided transient simulation engine or HSPICE at run time. A high degree of HSPICE specific automation is included and SystemSI accepts HSPICE encrypted subcircuits. This flow goes beyond basic signal integrity solutions that analyze timing margin phenomena in an isolated, piecemeal manner. With timing margins in the picosecond range, the traditional divide-and-conquer approach for phenomena such as reflections, crosstalk and non-ideal power effects such as SSN loses steam because each effect impacts the others in ways that are extremely difficult to predict. Simulation of the effects together emulates actual hardware behavior to predict timing margins in a realistic way.

Many Sigrity customers have made a major investment in HSPICE over the years and rely on it as a trusted gold-standard. Sigrity has pioneered electromagnetic analysis solutions that provide the accuracy essential for high-speed designs in an environment that supports rapid design improvement. The companies have worked together to develop design flows sharing these key technologies to ensure accurate results in an environment that is efficient and practical to use for complex, time-critical high-speed designs.

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