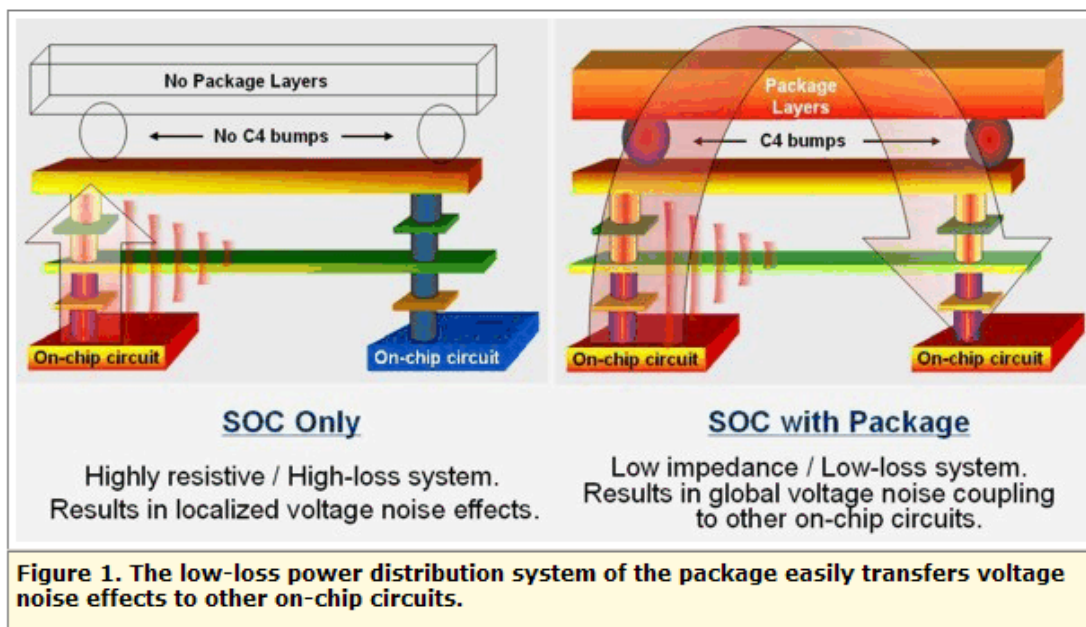


## ... But Will It Work?

September 2, 2008 -- After the arduous design tasks of formal verification, consideration of statistical process variations, optimization of yield, and eventually careful fabrication of an SOC with a device size smaller than the wavelength of light, a question still remains: "Will it perform as intended when placed in a package and applied in a higher-level system?" Off-chip system issues can result in failure of an otherwise successful SOC design that's incorporated into a larger system. The financial and schedule delay costs associated with post-fabrication failures are huge. Despite application of DFM techniques, significant issues are not observed during design for simulation of the SOC alone.

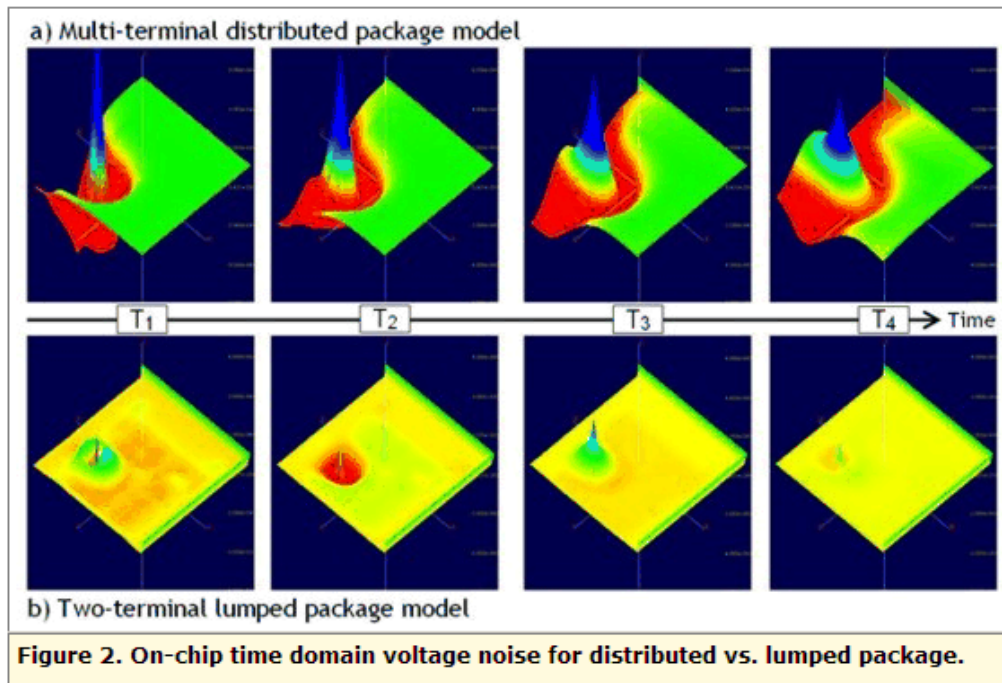
Without explicit design consideration of off-chip effects, it is difficult to assure a chip design will operate properly in a customer's system. High-speed chips, particularly those with flip-chip interconnect, are sensitive to noise that begins locally on-chip but propagates globally through package power planes, resulting in noise in remote regions of the chip (see Figure 1). When chips are analyzed in isolation, the assumption is made that noise will dissipate through the high-loss IC power grid. Unfortunately, this assumption fails to consider the effects of the low-loss package power planes on performance.



Traditional chip design approaches are based on the separate characterization of chip, package and board. These independent electrical models are combined via circuit simulation to form a system model. Often, these chip-centric analysis approaches rely on lumped or net-based models for the chip-package interface and fail to identify important distributed effects of the power-delivery system. It is these distributed effects that dominate voltage noise coupling from the power-delivery network to low- and high-speed signal nets.

### Successful approaches

Design approaches now are available for system-aware chip-centric design, and even for chip-package-board co-design. With a distributed electrical model applied for the chip-package interface, these approaches provide chip designers with an accurate view of critically interdependent chip and system structures. Evaluation of spatial variations in voltage noise in the time domain (see Figure 2) or across a broad range of frequencies enables a highly robust approach for considering issues such as simultaneous switching noise (SSN). A distributed chip-package interface model also supports exploration of various on- and off-chip decoupling capacitor options to address this noise.

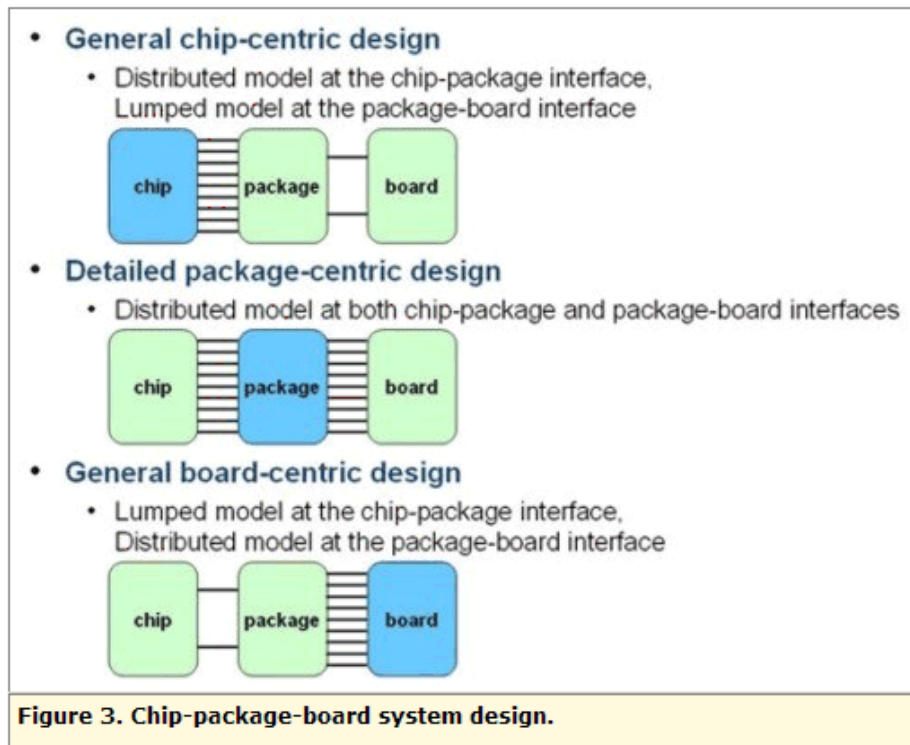


Successful co-design methodologies are available today. At their core are robust high-frequency electromagnetic analysis engines. A workable flow requires an automated approach to link the chip power grid to the package planes, and eventually link to the board. Chip and package CAD databases must be easily accessed to enable generation and linking of electrical models across the physical domain boundary. Further, the capacity to analyze this more complete system must also exist. With these elements in place, designers can step through issues in an organized way to understand design limitations and target improvements. Design adjustments among the chip, package and even board physical domains can yield power-integrity performance enhancement as well enable cost savings, while avoiding the risk of system failures.

### System modeling considerations

The early stages of chip design often begin with consideration of signal net and power grid loadings as two-terminal lumped loads. This is efficient for initial design but inadequate to assure SOC performance in higher-level systems. Figure 2 shows on-chip voltage noise in the power-delivery system due to a localized high-current switching event as a sequence of snapshots in time. The upper row of snapshots clearly demonstrates a global and non-uniform distribution of voltage noise across the entire chip. Accurate simulation of this package-induced distribution of noise through low-impedance power planes is enabled by applying a multi-terminal distributed package model. The lower row of snapshots in Figure 2 predicts a very localized and rapidly damped voltage noise response, which is not correct. Applying lumped package models as chip designs progress toward physical implementation may be convenient and support more simple system modeling, but it increases design failure risk by not properly considering off-chip effects.

For most chip designs, it is simply not possible to access detailed off-chip system information beyond the package. Typical board level loads for a packaged design must, therefore, be estimated. This is most commonly accomplished for chip-centric power-delivery design with a lumped two-terminal model of the package-board interface. Typical loads are assumed and their variations considered to represent broad system application of the packaged chip (see Figure 3).



As expected, board-centric design reverses the requirements for the two domain boundaries. Only a detail-oriented package-centric designer may be required to consider a fully distributed model throughout the chip-package-board system.

**By Brad Brim.**

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